Tackling Thermal Challenges in Power Semiconductors with Package and Silicon Advances
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Heat from hard-working power semiconductors represents wasted energy, and compromises system reliability. To overcome these challenges, equipment designers need new device technologies that not only minimise the amount of energy wasted per watt delivered, but also improve heat dissipation in order to safeguard reliability.

Introduction

Heat is the enemy of electronic designers, and also of equipment end users. To designers, high chip temperatures are a threat to reliability and promote early failure. Cooling electronics with fans, heatpipes, or heatsinks introduces unwanted engineering challenges, and forces the design to be larger and heavier than is ideal. Moreover, if a fan is needed, this adds to the overall system power demand, introduces an extra potential point of failure, and prevents sealing the enclosure to prevent ingress of dust or moisture.

Added to this, today’s tech-savvy end users understand that the hot casing of a smartphone or game console, laptop power supply or battery charger, is the result of wasted energy that equates to increased ownership costs, shorter battery life, greater loading on the supply grid, and higher CO₂ emissions from power stations.

Equipment designers, therefore, are under pressure to reduce the amount of energy converted into heat in equipment such as power supplies, and to manage heat more effectively so that smaller end products can handle higher power ratings and therefore support greater functionality.

The latest power semiconductors introduce improvements at the silicon level, which improve power-conversion efficiency leading to reduced heat generation, while improvements in package design not only contribute to reducing heat generation but also enhance heat dissipation to allow increased power handling without compromising reliability.

Prevention: Advancing Trench MOSFET Technology

As far as the efficiency of power MOSFETs is concerned, reducing on-state resistance ($R_{DS(ON)}$) to improve conduction performance has traditionally been achieved at the expense of poorer switching characteristics. On the other hand, optimising the device to reduce the gate charge ($Q_g$), which helps improve switching efficiency, tends to result in increased $R_{DS(ON)}$. The trade-off between these two parameters is expressed in the common figure of merit applied to power MOSFETs: $R_{DS(ON)} \times Q_g$.

The latest trench MOSFET technologies have overcome the traditional limitations on these two parameters, allowing lower conduction losses and better switching performance to be achieved at the same time.

Trench MOSFETs have evolved through several generations. One of the most important targets, with each successive process generation, has been to improve trench filling and so achieve closer spacing between trenches resulting in lower $R_{DS(ON)}$ per die area. At the same time, device capacitances and therefore gate charge can be kept low, which is essential to maintain switching performance and minimise the load placed on gate-driver circuitry. Figure 1 shows how improvements in trench fabrication have enabled both and $Q_g$ to be reduced in successive technology generations.
Figure 1. Advances in trench MOSFET technology have enhanced conduction and switching performance.

Devices based on Toshiba’s UMOS VIII-H process offer excellent switching ripple suppression capability and can help designers reduce overall EMI noise. This can be seen in the latest products such as the TK160F10N1L MOSFET for automotive applications.

Featuring a maximum RDS(ON) of just 2.4mΩ, this 100V, 160A power MOSFET delivers a much tighter threshold voltage (Vth) specification – a very important consideration for switching applications - than previous devices. A comparison of the specification of the new device with its predecessor is shown in the table below.

<table>
<thead>
<tr>
<th>Product Name</th>
<th>Package</th>
<th>VDSS (V)</th>
<th>ID (A)</th>
<th>RDS(ON) max(mΩ)</th>
<th>Vth min(V) / max(V)</th>
<th>Ciss typ(pF)</th>
<th>Crss typ(pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TK160F10N1 (Reference)</td>
<td>TO-220SM(W)</td>
<td>100</td>
<td>160</td>
<td>2.4</td>
<td>2V / 4V</td>
<td>8510</td>
<td>500</td>
</tr>
<tr>
<td>TK160F10N1L (New)</td>
<td></td>
<td></td>
<td></td>
<td>2.4</td>
<td>3.9</td>
<td>10100</td>
<td>610</td>
</tr>
</tbody>
</table>

The new MOSFET is ideal for automotive power switching applications. In these designs its tighter Vth specification could contribute to a dead time reduction in half-/H-/B6-bridge schemes. This is because the max Vth difference between low-side MOSFET and high-side MOSFET is smaller.

In applications where MOSFETs are connected in parallel, a tighter Vth spec leads to improved synchronous switching among paralleled MOSFETs. As a result, the switching loss will be distributed more evenly among the MOSFETs. If a single MOSFET turns on earlier or turns off later than other MOSFETs in parallel, the switching loss concentrates on this single MOSFET.
Toshiba’s latest UMOS VIII-H semiconductor process has been used in the TK160F10N1L. U-MOS VIII-H has an excellent switching ripple suppression capability and can contribute to EMI noise reduction. Target applications for the new MOSFET include automotive motors in 48V systems, DC-DC converters and load switches.

Toshiba’s latest-generation UMOS IX-H MOSFETs improve transistor figures of merit such as \( R_{\text{DS(ON)}} \times A \) (on resistance x die area) and \( R_{\text{DS(ON)}} \times C_{\text{iss}} \) (on resistance x input capacitance), resulting in better conduction performance and lower gate-drive losses. In addition, reduced output capacitance (COSS) reduces output charge (QOSS) leading to better switching efficiency.

Toshiba has reduced die resistance by 42% in its latest UMOS IX-H silicon, compared to the UMOS VIII generation, leveraging advances such as improved trench filling. 30V and 60V N-channel UMOS IX-H MOSFETs are now in the market. The 30V devices have ultra-low \( R_{\text{DS(ON)}} \) of 0.6mΩ (max.) at \( V_{GS} = 10V \), and 2160pF typical \( C_{\text{oss}} \). For the 60V MOSFET, \( R_{\text{DS(ON)}} \) is 1.3mΩ and typical \( C_{\text{oss}} \) is 960pF.

**Cure: Package Technology Minimising DFPR and More**

As the \( R_{\text{DS(ON)}} \) of successive device generations has fallen continuously from one generation to the next, the impact of package parasitic effects on overall device performance has become more significant. Increasing the cross-sectional area of the package leadframe and terminations, together with more efficient ohmic connections to the die metallisation, helps to reduce the die-free package resistance (DFPR), leading to lower overall MOSFET on-state resistance.

A new DPAK+ power package has been developed, which has the same dimensions and outline as the conventional DPAK but uses copper clips to connect the gate and source pins directly to the metallised electrodes on the die. These copper clips replace the aluminium bondwires, and benefit from a large cross-section and increased contact area at the die. This has yielded a 73% improvement in DFPR. This significantly reduces I2R losses due to the package, and also allows higher maximum current. Figure 2 compares the more efficient and robust copper-clip gate and source connections with traditional wirebonds.
Figure 2. Copper-clip technology replaces bondwires with electrically and thermally efficient gate and source connections.

The TO-220SM(W) power package shown in figure 3 also features copper-clip technology, has an outline comparable to that of the conventional D2PAK (TO-263), but in addition has a source pin more than three times wider. These enhancements boost maximum current rating to 200A, while reducing the total board footprint by more than 13% to just 13mm x 10mm.

<table>
<thead>
<tr>
<th>Package</th>
<th>Conventional D2PAK (TO-263)</th>
<th>Toshiba TO-220SM(W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Size</td>
<td>15mm x 10mm</td>
<td>13mm x 10mm</td>
</tr>
<tr>
<td>Source pin width</td>
<td>~0.75mm</td>
<td>2.35mm</td>
</tr>
<tr>
<td>Bonding</td>
<td>Al wire</td>
<td>Cu clip</td>
</tr>
<tr>
<td>Picture</td>
<td><img src="image1" alt="DPAK" /></td>
<td>![TO-220SM(W)]</td>
</tr>
</tbody>
</table>
Figure 3. TO-220SM(W) with copper-clip technology, D2PAK-size outline, and low-resistance source pin.

The enhanced electrical conductivity of the connections in packages such as Copper-clip lowers overall energy loss within the device and therefore contributes to reducing heat generation. The larger conductors also increase the package-limited current-carrying capability. Although this can help equipment designers increase the power density of new designs, increased current obviously increases power dissipation due to $I^2R$. The imperative to remove heat effectively from the package becomes even more urgent.

To this end, Toshiba is taking advantage of new and advanced package technologies designed to utilise the package surface as fully as possible to promote heat dissipation. The first UMOS IX-H trench MOSFETs were introduced in the latest DSOP Advance package, which is engineered for highly efficient heat dissipation through the top-side as well as via the underside into a thermal pad on the PCB. Figure 4 illustrates the package and cooling principle.

Figure 4. DSOP Advance maximises heat dissipation within the 5mm x 6mm footprint made popular by the industry-standard SOP.

DSOP Advance connects the source metallisation on the upper surface of the die directly to a large electrode on the top side of the package. This not only utilises the upper package surface to dissipate heat, but allows the drain electrode on the underside to be much larger than is possible in the conventional SOP. DSOP devices can be used with an ordinary FR4 substrate and can help to significantly reduce system temperatures, giving designers extra freedom to specify smaller.

Testing the DSOP Advance alongside the conventional SOP has shown a 26% improvement in dynamic thermal resistance ($R_{th}$). Figure 5 compares the dynamic $R_{th}$ of both packages when test currents of varying pulse widths are passed through the device.
Figure 5. DSOP Advance significantly improves dynamic thermal resistance.

DSOP Advance has the same footprint as the standard 5mm x 6mm SOP designed for single-sided cooling. Figure 6 compares the cross section of DSOP Advance with the SOP as well as a competing dual-side package. Unlike DSOP Advance, the construction of the competing package utilises a stacked connector to expose the pad on the upper surface. This type of construction introduces interfacial thermal resistances between the elements of the stack, as shown. DSOP Advance, with its one-piece integrated connector, achieves greater thermal efficiency.

Figure 6. Comparison of single-side and dual-side cooled packages.
Figure 7 helps to appreciate the improvements in electrical performance brought about by the recent advances in device and package technology. As Toshiba MOSFETs in the 5x6mm footprint have evolved from UMOS VIII to UMOS IX-H technology, the new silicon has reduced $R_{\text{DS(ON)}}$ by 42%, while the lower DFPR of the DSOP Advance is responsible for an additional 25% reduction. This diagram, of course, is concerned only with electrical performance and does not express the increased thermal capability of the DSOP Advance package. Figure 8 provides a longer-term view of the trend in device on resistance resulting from the combined effects of silicon and package improvements.

Figure 7. Combined effects of package and silicon improvements.
Figure 8. Reduction in trench MOSFET $R_{DS(ON)}$ with silicon and package technology advances.

Other thermally enhanced packages such as SOP Advance, TSON Advance and PS-8 maximise heat dissipation through the underside of the device only, and are suited to cost-sensitive applications at lower power levels. TSON Advance achieves comparable power dissipation to the conventional 5mm x 6mm SOP-8, but within a 64% smaller footprint of just 3.3mm x 3.3mm.

Summary

Improvements at the silicon and package levels in power devise both contribute towards lowering unwanted resistances that cause energy losses and internal heating. By combating these effects, the latest UMOS IX-H MOSFETs in the DSOP Advance package help designers deliver more attractive products offering better performance and environmental credentials than their competitors. Similar package technologies that offer enhanced electrical and thermal performance, such as DPAK+ and TO-220SM(W) with Copper-clip technology or TSON Advance optimised for single-side cooling, give designers even more options in the battle to minimise avoidable energy losses, boost current/power capability per device, and maximise reliability.

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