

Stable cascode GaN HEMT operation by direct gate drive

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Abstract— We describe a proposed cascode GaN device configuration that allows stable operation during zero voltage switching (ZVS) turn-on transition and suppresses non-ZVS losses. We verified that application of our proposed device to an LLC resonant converter resulted in stable operation. In our device configuration, a GaN high-electron-mobility transistor (HEMT) gate is directly driven by a commercial Si MOSFET driver via a charge pump circuit. This allows the slew rate (dv/dt) to be controlled by an external gate resistance. In addition, we demonstrate that the 650-V normally-on GaN HEMT used in our proposed device configuration has highly reliable characteristics. The predicted lifetime for a 0.1% failure rate under actual bias conditions ($V_{ds} = 500$ V at 150°C) exceeds 1000 years (8.76×10^6 hr).

Keywords—GaN power device; cascode GaN HEMT; zero volt switching; stable operation; LLC resonant converter

I. INTRODUCTION

GaN power devices are promising candidates for achieving high efficiency and/or downsizing systems. The GaN transistors used in practice for power conversion can be classified into cascode GaN high-electron-mobility transistors (HEMTs) and normally-off GaN HEMTs with a p-GaN gate. GaN MOS FETs are promising devices, but more time is required before they will be ready for mass production [1]. Cascode GaN devices, combining a normally-on GaN HEMT and a normally-off Si MOSFET, are less susceptible to gate-loop noise leading to malfunctions because they have a higher threshold voltage (> 2.5 V) than p-GaN gate normally-off HEMT devices, which have a threshold voltage of around 1.5 V. The conventional cascode GaN device shown in Fig. 1 a) has issues in terms of self turn-on during zero voltage switching (ZVS) [2], poor controllability of switching slew rates (dv/dt) by an external gate resistor [3], [4] and reverse recovery losses attributable to the body diode of the Si MOSFET. In high-frequency switching applications used in downsizing systems, ZVS systems such as the LLC resonant converter provide effective control topology to suppress the increase in switching losses [5], [6]. A stable internode voltage (INV) as shown in Fig. 1 a) is important to keep the GaN HEMT from being "OFF" during the turn-on transition of ZVS. In this paper, we demonstrate that the proposed cascode

GaN device configuration [7] shown in Fig. 1 b) can overcome the issues described above, especially the INV instability.

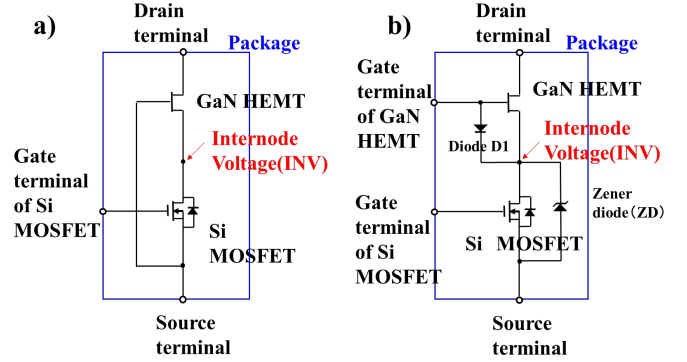


Fig. 1. a) Conventional cascode GaN device; b) Proposed cascode GaN device.

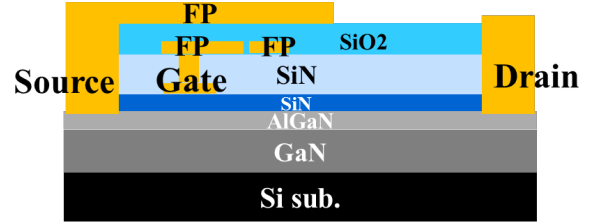


Fig. 2. Schematic view of normally-on GaN HEMT.

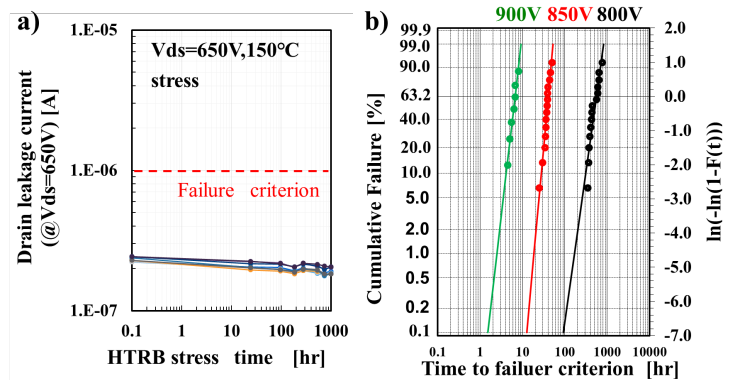


Fig. 3. a) Time dependence of off-state drain leakage current in GaN HEMT during HTRB test ($V_{ds} = 650$ V, $V_{gs} = -15$ V, 150°C); b) Weibull distribution of failure time of GaN HEMT in voltage acceleration test.

II. STRUCTURE AND DEVICE CHARACTERISTICS OF NORMALLY-ON GaN HEMT

Fig. 2 shows a schematic view of the 650-V normally-on GaN HEMT used in our proposed cascode GaN device. The optimized FP structure makes it possible to reduce $R_{on} \cdot Q_{gd}$ to $0.148 \text{ } \Omega \cdot \text{nC}$ while enhancing the reliability at the same time. Total R_{on} is $110 \text{ m}\Omega$. Fig. 3 a) shows the timeline for the drain leakage current during high-temperature reverse bias (HTRB) tests at 650 V. The failure criterion is $1 \text{ } \mu\text{A}$. Fig. 3 b) shows the Weibull distribution of the failure time for HTRB measurement settings V_{ds} of 800 V, 850 V and 900 V at 150°C . The voltage acceleration coefficient β is 0.044, derived from the mean time to failure (MTTF). Fig. 4 shows that the predicted lifetime for a 0.1% failure rate under the condition of $V_{ds} = 500 \text{ V}$ at 150°C exceeds 1000 years ($8.76 \times 10^6 \text{ hr}$). Even under a rated drain voltage of 650 V, the MTTF exceeds 10 years. Fig. 5 shows the R_{on} and V_{th} stability of the GaN HEMT during HTRB tests. Our proposed cascode GaN device is composed the highly reliable normally-on GaN HEMT.

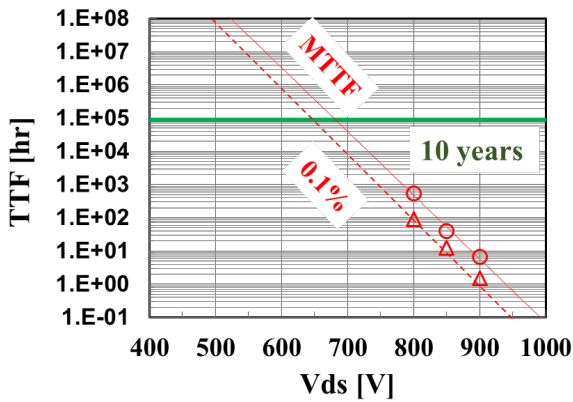


Fig. 4. Dependence of predicted lifetime on voltage acceleration factor.

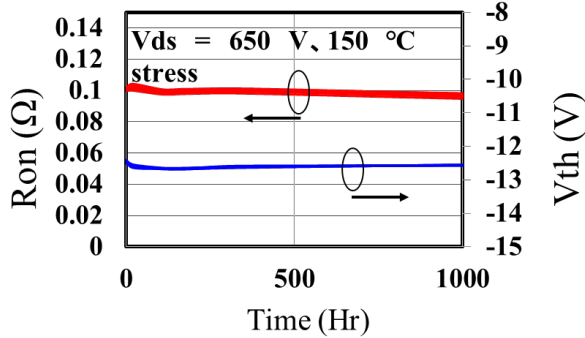


Fig. 5. Time dependence of R_{on} and V_{th} of GaN HEMT during HTRB test ($V_{ds} = 650 \text{ V}$, $V_g = -15 \text{ V}$, 150°C).

III. PROPOSED CASCODE GaN DEVICE

Fig. 6 shows the proposed cascode GaN device in a package and the proposed gate driving circuit. Although the proposed cascode GaN device functions as a normally-off GaN HEMT in the off state, as shown in Fig. 7 a), the gate terminals of the GaN HEMT and Si MOSFET can be controlled independently. The charge-pump circuit converts

the input voltage swinging between 0 V and 15 V to a range between -14.1 V and 0.9 V at the normally-on GaN gate (Fig. 7 b-1), b-3)). The resistor R_{LG} and the C_{iss} of the Si MOSFET make the CR time constant of the input circuit sufficiently large to keep the Si MOSFET stably “ON” during the switching operation, as shown in Fig. 7 b-2). As a result, INV in Fig. 6 is stably grounded during switching operations. Fig. 8 shows the double pulse switching behavior of our proposed cascode GaN device for various external R_{gex} values using a half bridge test circuit. The slew rate (dv_{ds}/dt), the drain current (I_d) overshoot and the turn-on loss (E_{on}) are controlled by changing R_{gex} from $20 \text{ } \Omega$ to $62 \text{ } \Omega$. Our proposed device has the advantage of being operated under optimal conditions in terms of both switching losses and electromagnetic interference (EMI).

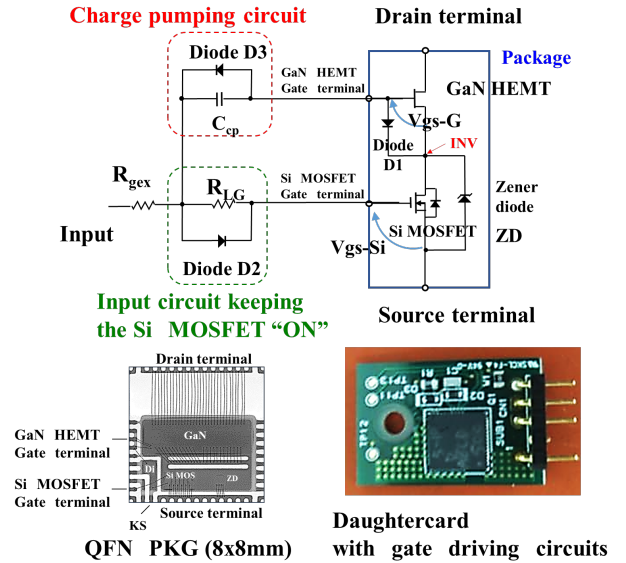


Fig. 6. Proposed cascode GaN device and gate driving circuit.

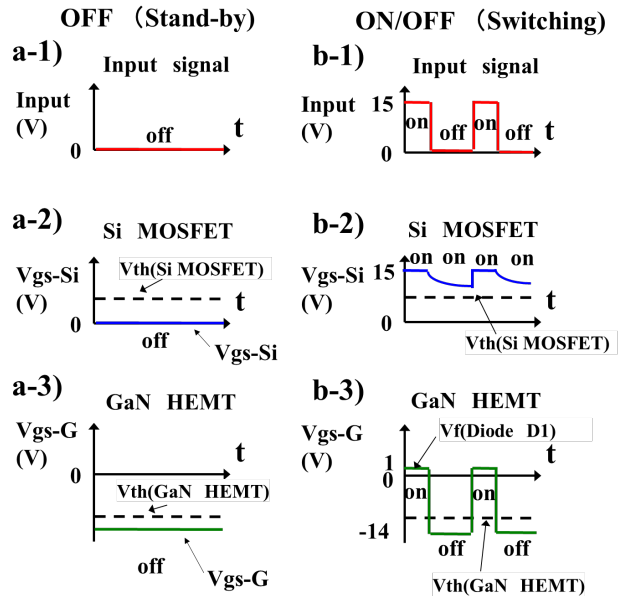


Fig. 7. Voltage of each point in the off state and switching state.

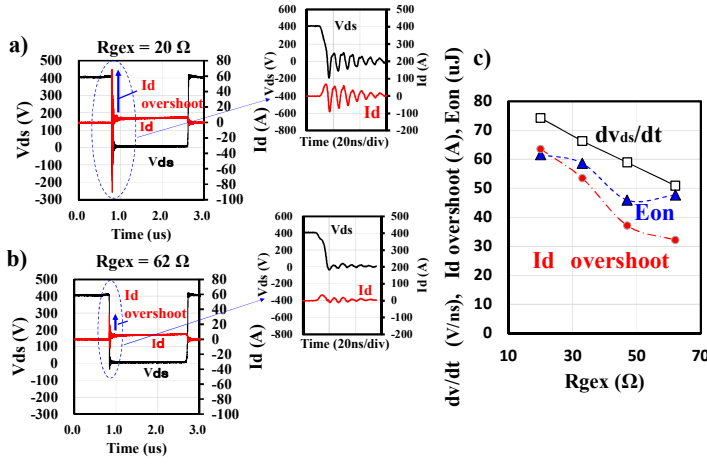


Fig. 8. Double pulse switching behavior; a) Waveform with $R_{gex} = 20 \Omega$; b) Waveform with $R_{gex} = 62 \Omega$; c) Slew rate (dv_{ds}/dt), I_d overshoot and turn-on loss (E_{on}) dependence on R_{gex} .

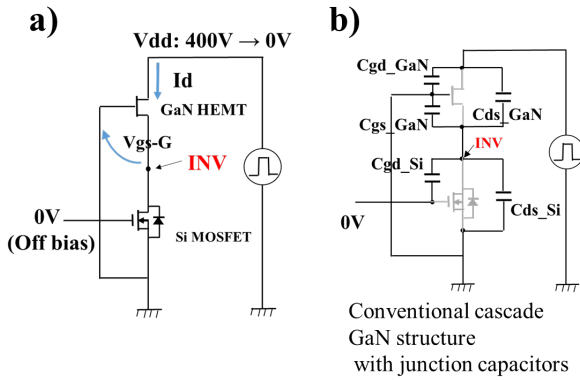


Fig. 9. Evaluation circuit of conventional cascode GaN device.

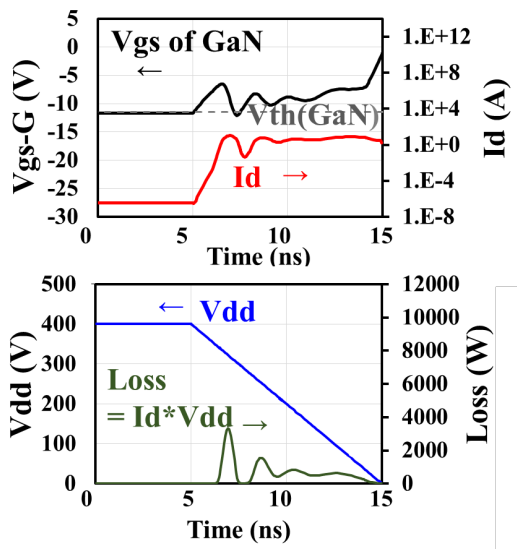


Fig. 10. Results of the INV stability simulation of conventional cascode device.

IV. UNSTABLE BEHAVIOR OF CONVENTIONAL CASCODE GaN HEMT

During the off-to-on transition period in ZVS mode, there is a risk that self turn-on will occur because of INV fluctuations

with the conventional cascode GaN device. The circuits shown in Fig. 9 were used to simulate the self turn-on phenomenon because of the instability of INV. INV was evaluated when the output voltage V_{dd} was forcibly changed from 400 V to 0 V to simulate the turn-on transition period in soft-switching. V_{gs-G} and V_{th} are the gate-source voltage and threshold voltage of the conventional GaN HEMT respectively. When the output voltage (V_{dd}) decreases, the INV of the conventional cascode GaN device also decreases because it depends on the junction capacitance ratio of the Si MOSFET and the GaN HEMT as shown in Fig. 9 b). If the V_{ds} of the Si MOSFET decreases below the absolute value of threshold voltage of the GaN HEMT, turning on of the GaN HEMT makes the Si MOSFET reach avalanche and self-turn-on and non-ZVS loss will occur as shown in Fig. 10. When the junction capacitance of the Si MOSFET is much smaller than that of the GaN HEMT, this mismatch causes the GaN HEMT to turn itself on [2]. In this case, self turn-on causes non-ZVS losses to occur in every switching cycle.

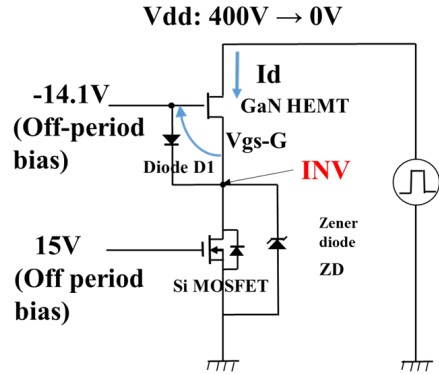


Fig. 11. Evaluation circuit of proposed cascode GaN device.

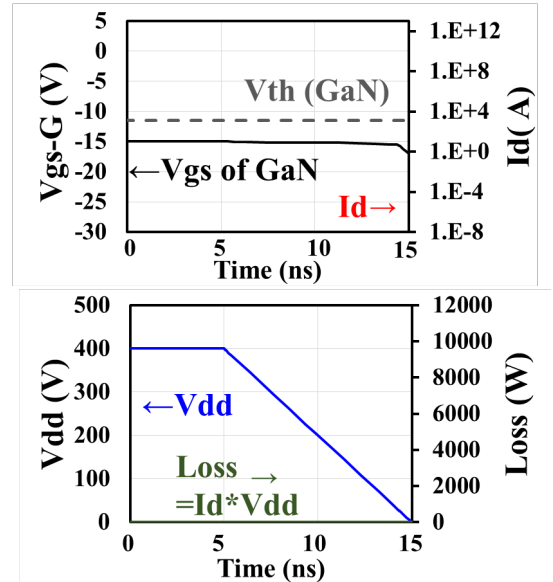


Fig. 12. Results of the INV stability simulation of proposed cascode device.

V. STABLE OPERATION OF PROPOSED CASCODE GaN HEMT

The INV stability of the proposed cascode GaN device was evaluated using the circuits shown in Fig. 11. In our proposed cascode device, the INV is stably grounded because the Si MOSFET is “ON” during switching, as shown in Fig. 7. Both the GaN HEMT and Si MOSFET gates are simply set to -15 V and 15 V as the off-period bias of the switching operation during the simulation. The GaN HEMT is kept “OFF” even when the output voltage (V_{dd}) drops, because the GaN HEMT gate is controlled independently. As illustrated in Fig. 12, self turn-on does not occur and non-ZVS losses are suppressed. We applied the proposed device and circuit configuration to the LLC resonant converter shown in Fig. 13. The normally-on GaN HEMT was modified to the middle voltage application. The input voltage was 120 V, the output voltage was 20 V and the switching frequency was 1 MHz. We verified that the LLC resonant converter operated without any observable self turn-on problems as shown in Fig. 14. The Si MOSFET is always “ON” since the gate voltage (V_{gSi}) of the Si MOSFET is sustained above the threshold voltage during switching as shown in Fig. 7 b-2). The gate voltage (V_{gGaN}) of the GaN HEMT is controlled independently of the Si MOSFET as shown in Fig. 7 b-3).

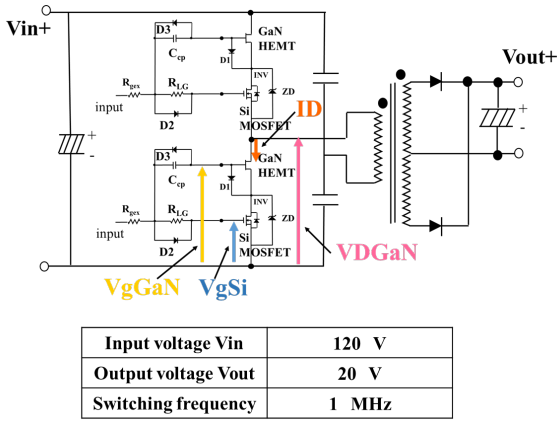


Fig. 13. Circuit diagram of the LLC resonant converter.

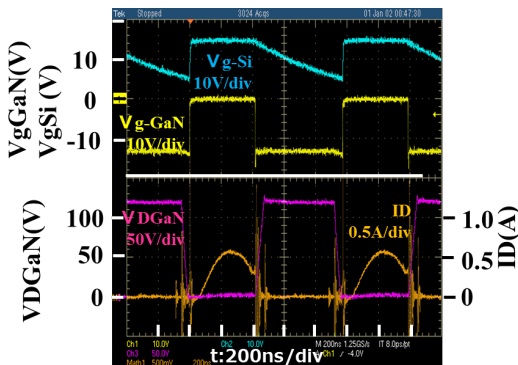


Fig. 14. Operation waveforms of the LLC resonant converter.

VI. CONCLUSION

We demonstrated the operation of a controllable slew-rate cascode GaN power device that was configured with a highly reliable normally-on GaN HEMT. By optimizing the FP design of the GaN HEMT, a predicted lifetime of more than 1000 years ($V_{ds} = 500$ V at 150°C) was achieved. The stably grounded INV allowed stable operation during the ZVS turn-on transition and suppression of the non-ZVS losses. Moreover, there was no loss of the reverse recovery charge Q_{rr} , because the Si MOSFET was always “ON” during switching. The proposed cascode device thus made full use of the normally-on GaN HEMT characteristics, such as high speed switching and absence of a reverse recovery charge Q_{rr} . These characteristics make our proposed cascode GaN device suitable for application to LLC resonant DC-DC converters and in other ZVS applications.

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REFERENCES

- [1] T. Yonehara, Y. Kajiura, D. Kato, K. Uesugi, T. Shimizu, Y. Nishida, H. Ono, A. Shindome, A. Mukai, A. Yoahioaka and M. Kuraguchi, "Improvement of Positive Bias Temperature Instability Characteristics in GaN MOSFETs by Control of Impurity Density in SiO_2 Gate Dielectric," in IEEE IEDM Tech., Dig., pp.745-748, 2017
- [2] X. Huang, W. Du, F. C. Lee, Q. Li and Z. Liu, "Avoiding Si MOSFET Avalanche and Achieving Zero-Voltage Switching for Cascode GaN Devices" IEEE Transactions on power electronics, Vol. 31, no.1, pp.593-600, 2016
- [3] A. Endruschat, T. Heckel, R. Reiner, P. Waltereit, R. Quay, O. Ambacher, M. Marz, B. Eckardt and L. Frey, "Slew Rate Control of a 600 V 55 mΩ GaN Cascode" in Proc. IEEE 4th Workshop Wide Bandgap Power Devices and Application, Fayetteville, AR, USA, pp.334-339, Nov. 2016
- [4] D. Aggeler, F. Canles, J. Biela and J. W. Kolar, "Dv/Dt-Control Methods for the SiC JFET/Si MOSFET Cascode" IEEE Transactions on power electronics, Vol. 28, no.8, pp.4074-4082, 2013
- [5] W. Zhang, F. Wang, D. J. Costinett, L. M. Tolbert and B. J. Blalock, "Investigation of Gallium Nitride Devices in High-Frequency LLC Resonant Converters," IEEE Transactions on power electronics, Vol. 32, no.1, pp.571-583, 2017
- [6] M. Mu, and F. C. Lee, "Design and Optimization of a 380-12 V High-Frequency, High-Current LLC Converter With GaN Devices and Planar Matrix Transformers," IEEE Journal of emerging and selected topics in poer electronics, Vol. 4, no.3, pp.854-862, 2016
- [7] M. Koyama, K. Ikeda and K. Takao, "Novel cascode GaN module integrated a single gate driver IC with high switching speed controllability," in European Conference Power Electronics and Applications (EPE) Tech., Dig., 2018

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