SiC Snacks Bite Sized Benefits

Optimal $R_{DS(ON)} * Q_{gd}$

What does it mean?

 $R_{DS(ON)}$, which is known as the on-resistance, is an intrinsic property of the MOSFET that will contribute to the power losses witnessed. This is influenced by the architecture and the semiconductor material used.

Basically, $R_{DS(ON)}$ signifies the resistance between the MOSFET's drain and source elements when a specific gate-tosource voltage (V_{GS}) is applied. As the V_{GS} increases, the $R_{DS(ON)}$ generally decreases. For this reason, datasheets will state the typical $R_{DS(ON)}$ at particular V_{GS} values.

While $R_{DS(ON)}$ is concerned with static (or conduction) losses, the gate charge (Q_{gd}) relates to dynamic power losses (which are the ones associated with switching operation). The Q_{gd} consists of several component elements and defines the amount of charge needed to activate the MOSFET.

VGS

The combination of $R_{DS(ON)}$ with the Q_{gd} results in a figure of merit (FoM) that proves invaluable for assessing MOSFET performance - with information on both types of power loss covered.

What's the benefit?

The lower that the $R_{DS(ON)} * Q_{gd}$ FoM is, the smaller the power losses of the MOSFET will be. It will thereby mean that higher degrees of system efficiency can be attained. In addition, less heat will be generated, so thermal management will not be as problematic.

Improvements in the $R_{DS(ON)}$ and Q_{gd} values of Toshiba's 3rd generation silicon carbide (SiC) MOSFETs (with a 80% reduction on the previous generation) are helping engineers to keep pushing the performance envelope of their power system designs. With less heat needing to be dissipated, these systems can also be simpler and more compact - with board space and component cost savings.

Product specifications are all subject to change without notice. Product design specifications and colours are subject to change without notice and may vary from those shown. Errors and omissions excepted.





Prescribed current

monitor

Constant

current, In



Drain (D)

М

Gate (G)

Source (S)

SiC Snacks Bite Sized Benefits

Suppressing Body Diode Conduction Effects

What does it mean?

A MOSFET's body diode is an inherent parasitic element found in all such devices. Reducing the effects of body diode conduction during the switching process is something that needs addressing - otherwise it will cause an increase in the switching losses experienced and add to the on-resistance ($R_{DS(ON)}$) too. Normally this is done by putting an external Schottky Barrier Diode (SBD) in parallel with the MOSFET.

What's the benefit?

Research has shown the contribution that a MOSFET's body diode makes to turn-on losses will rise substantially as the junction temperature is increased. Likewise, its R_{DS(ON)} will be very susceptible to heat variations and also get worse over its working lifetime. This is why SBD inclusion within the MOSFET is so important - as current will then pass through this rather than the parasitic body diode. It must be noted that the conventional external SBD arrangement takes up board real estate and adds to the component count.

In contrast to the SiC MOSFETs produced by other vendors, the 3rd generation of Toshiba SiC MOSFETs each feature a built-in SBD. These fast operating SBDs are able to take care of $R_{DS(ON)}$ fluctuation suppression and curb power losses, while simultaneously presenting engineers with a compact streamlined solution that is easy to implement. Their forward voltage (V_F) of just -1.35V (typical) means reverse conduction losses or minimal. The favourable V_F and $R_{DS(ON)}$ temperature characteristics are thanks to the advanced doping methods used.

Product specifications are all subject to change without notice. Product design specifications and colours are subject to change without notice and may vary from those shown. Errors and omissions excepted.





Body Diode





SIC MOSFET

SiC Snacks Bite Sized Benefits

Wide V_{GSS} and high V_{th} ratings

What does it mean?

V_{GS} is the voltage that is applied between the gate and the source of a switching device in order to drive it, with V_{GSS} denoting the maximum acceptable values for this. If the V_{GSS} figures are exceeded, then the MOSFET could be damaged. As silicon carbide (SiC) MOSFETs have higher power densities than their silicon counterparts, heightened V_{GSS} characteristics are important, so that the possibility of unwanted short circuits and other functional problems are safeguarded against. Alongside this, a high gate-threshold voltage (V_{th}) will help to ensure against false turn-ons (due to high levels of noise) occurring.

What's the benefit?

The ability to specify MOSFETs that have expanded V_{GSS} figures is certain to be of value to engineers. This will mean that greater tolerances can be accommodated within their power system designs. Consequently, noise issues, acceleration in switching speeds and variations in environmental conditions (such as ambient temperature) are less likely to impact on overall operational performance.



V _{DSS} : 650V			V _{DSS} : 1200V		
R _{DS(ON)} (typ)	TO-247	TO-247-4L	R _{DS(ON)} (typ)	TO-247	TO-247-4L
	*			*	
15mΩ	TW015N65C	TW015Z65C*	15mΩ	TW015N120C	TW015Z120C*
27mΩ	TW027N65C	TW027Z65C*	30mΩ	TW030N120C	TW030Z120C*
48mΩ	TW048N65C	TW048Z65C*	45mΩ	TW045N120C	TW045Z120C*
83mΩ	TW083N65C	TW083Z65C*	60mΩ	TW060N120C	TW060Z120C*
107mΩ	TW107N65C	TW107Z65C*	140mΩ	TW140N120C	TW140Z120C*

SiC MOSFET 3rd generation line-up

* Under development

© 2023 Toshiba Electronic Devices & Storage Corporation

Product specifications are all subject to change without notice. Product design specifications and colours are subject to change without notice and may vary from those shown. Errors and omissions excepted.



Sic Snacks Bite Sized Benefits

Kelvin Source Pin for Precise Control

What does it mean?

As silicon carbide (SiC) MOSFETs deal with large currents being switched at elevated speeds, the effect of parasitic inductances situated between the gate and the source can become problematic. The resulting voltage drop means that such MOSFETs will experience a slowing of their switching speed. It will also cause power losses which will lower conversion efficiency. Inclusion of a Kelvin source pin within the MOSFET design makes a real difference. It provides a low current connection to the source which is separate from the power source pin. Complementing the 3-pin version, Toshiba also offers 4-pin SiC MOSFETs, which each feature a Kelvin source pin. This arrangement allows a significant boost in performance parameters.

What's the benefit?

Inclusion of a Kelvin source pin (as shown on the right of the diagram directly below) means there is a dedicated connection for the driving signal, rather than having to rely on the power source pin to deliver both power and the driving loop. It means that the parasitic inductances found between the gate and source no longer impact on the current driving the MOSFET or the speed at which switching is conducted. MOSFET turn-on is not slowed down by a voltage drop across such inductances and unwanted turn-on losses are avoided.





eeds, ne problematic.



 $\ensuremath{\mathbb{C}}$ 2023 Toshiba Electronic Devices & Storage Corporation

Product specifications are all subject to change without notice. Product design specifications and colours are subject to change without notice and may vary from those shown. Errors and omissions excepted.

SiC Snacks Bite Sized Benefits

Switching Capabilities

What does it mean?

One of the stand-out characteristics that SiC MOSFETs offer over silicon-based IGBTs is their far superior switching capabilities coming as close as the industry has been able to, so far, to an ideal switch arrangement. Reaching MHz frequencies, these wide bandgap devices are orders of magnitude faster in this respect. They are able to rapidly respond to changes in current (di/dt) or voltage (dv/dt), transitioning from the off to the on state in a short timeframe. Switching occurs once their defined V_{th} has been reached, but they can successfully block voltages below this (making them invaluable in high-power switching applications). Since their switching periods are very short, they exhibit minimum switching losses during that time. Because of the enhanced switching capabilities associated with them, Toshiba's SiC MOSFETs are addressing opportunities in electric vehicle charging hardware, telecommunications network infrastructure, renewable energy generation equipment and high-power industrial systems.

What's the benefit?

The elevated switching speeds of SiC MOSFETs are advantageous for numerous reasons. With switching losses being reduced, the amount of accompanying thermal management is substantially less. In addition, the associated passive components (inductors and capacitors) being incorporated into the design can be smaller and will also be less expensive to procure. Consequently, SiC-based switching implementations will not only save valuable space, but also keep the overall bill-of-material (BoM) costs involved down.

Product specifications are all subject to change without notice. Product design specifications and colours are subject to change without notice and may vary from those shown. Errors and omissions excepted.





SIC MOSFET





- High switching frequencies
- Reduced size of passive components and cooling system
- EMC needs to be handled
- BOM cost reduction

^{© 2023} Toshiba Electronic Devices & Storage Corporation