

TB6560AFG Usage Considerations

The TB6560AFG drives a two-phase bipolar stepping motor.

It drives at a constant current by PWM control. The TB6560AFG can be used in applications that require 2-phase, 1-2-phase, 2W1-2-phase and 4W1-2-phase excitation modes. It is capable of forward and reverse driving of a two-phase bipolar stepping motor using only a clock signal.

1. Power Supply Voltage

(1) Operating Range of Power Supply Voltage

Characteristic	Symbol	Operating Voltage Range	Absolute Maximum Ratings	Unit
Control power supply voltage	V_{DD}	4.5 to 5.5	6	V
Motor power supply voltage	V_{MA}, V_{MB}	4.5 to 34	40	V

The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.

If a voltage outside the operating range as follows; $4.5 \le V_{DD} \le 5.5$, $4.5 \le V_{MA/B} \le 34$, $V_{DD} \le V_{MA/B}$ is applied, the IC may not operate properly or the IC and peripheral parts may be permanently damaged. Ensure that the voltage range does not exceed the upper and lower limits of the specified range.

(2) Power-on Sequence with Control Input Signals

Turn on VDD. Then, when the VDD voltage has stabilized, turn on VMA/B.

Hold the control input pins Low while turning on V_{DD} and $V_{MA/B}$.

(All the control input pins are internally pulled down.)

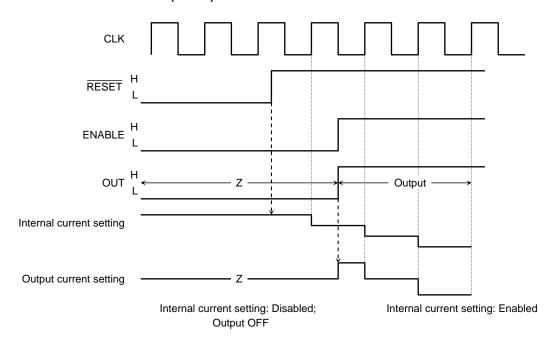
After V_{DD} and $V_{MA/B}$ completely stabilizes at the rated voltages, the \overline{RESET} and ENABLE pins can be set High. If this sequence is not properly followed, the IC may not operate correctly, or the IC and the peripheral parts may be damaged.

When RESET is released High, the CLK signal is applied and excitation is started. Only after ENABLE is also set High, outputs are enabled. When only \overline{RESET} is set High, outputs are disabled and only the internal counter advances. Likewise, when only ENABLE is set High, the excitation will not be performed even if the CLK signal is applied and the outputs will remain in the initial state.

An example of a control input sequence is shown below.

A power-off sequence should be the reverse of this sequence.

Recommended Control Input Sequence is indicated below.



2. Output Current

The absolute maximum rating is 2.5 A per phase, and the upper limit of operating current is 1.5 A per phase. The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.

The average permissible current is restricted by total power dissipation. Please use the IC within the range of the power dissipation.

3. Output ON-Resistance

Output ON-resistances for H-bridge: 0.7 Ω typical and 1.0 Ω maximum (upper and lower sum) with a test condition of the I_{out} = 1.5 A

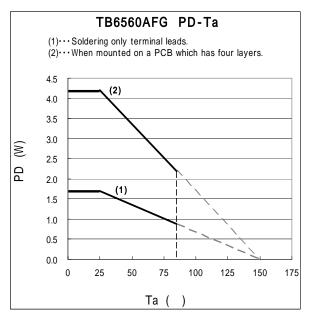
4. Output Residual Voltage

The residual voltages of the M_O and Protect output pins are up to 0.5 V each where Io = 1 mA.

5. Power Dissipation

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Pp-Ta curve of the TB6560AFG in each mounted condition are shown below.



Power consumption in each excitation mode is calculated at a rough estimate as follows:

2-phase excitation

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P = V_{DD} \times I_{DD} + (Ron(U + L) \times I_{O} \times I_{O}) \times 2
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1-2 phase excitation

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P = V_{DD} \times I_{DD} + \{(Ron(U + L) \times I_0 \times 100\% \times I_0 \times 100\% \times (2/8)) + (Ron(U + L) \times I_0 \times 71\% \times I_0 \times 71\% \times (4/8)) + (Ron(U + L) \times I_0 \times 0\% \times I_0 \times 0\% \times (2/8))\} \times 2
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• 2W1-2 phase excitation

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P = V_{DD} \times I_{DD} + \{ (Ron(U+L) \times Io \times 100\% \times Io \times 100\% \times (2/32)) + (Ron(U+L) \times Io \times 98\% \times Io \times 98\% \times (4/32)) + (Ron(U+L) \times Io \times 98\% \times Io \times 98\% \times (4/32)) + (Ron(U+L) \times Io \times 98\% \times 100\% \times Io \times 98\% \times Io \times 98\% \times 100\% \times Io \times 98\% \times 100\% \times 100\%
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+ (Ron(U + L) \times Io \times 92\% \times Io \times 92\% \times (4/32)) + (Ron(U + L) \times Io \times 83\% \times Io \times 83\% \times (4/32))
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$$+ (Ron(U + L) \times Io \times 71\% \times Io \times 71\% \times (4/32)) + (Ron(U + L) \times Io \times 56\% \times Io \times 56\% \times (4/32))$$

$$+ \left(Ron(U+L) \times Io \times 38\% \times Io \times 38\% \times (4/32) \right) + \left(Ron(U+L) \times Io \times 20\% \times Io \times 20\% \times (4/32) \right) + \left(Ron(U+L) \times Io \times 20\% \times Io \times 20\% \times (4/32) \right) + \left(Ron(U+L) \times Io \times 20\% \times Io \times 20\% \times (4/32) \right) + \left(Ron(U+L) \times Io \times 20\% \times Io \times 20\% \times (4/32) \right) + \left(Ron(U+L) \times Io \times 20\% \times Io \times 20\% \times (4/32) \right) + \left(Ron(U+L) \times Io \times 20\% \times Io \times 20\% \times (4/32) \right) + \left(Ron(U+L) \times Io \times 20\% \times Io \times 20\% \times (4/32) \right) + \left(Ron(U+L) \times Io \times 20\% \times Io \times 20\% \times (4/32) \right) + \left(Ron(U+L) \times Io \times 20\% \times Io \times 20\% \times (4/32) \right) + \left(Ron(U+L) \times Io \times 20\% \times Io \times 20\% \times (4/32) \right) + \left(Ron(U+L) \times Io \times 20\% \times Io \times 20\% \times (4/32) \right) + \left(Ron(U+L) \times Io \times 20\% \times Io \times 20\% \times (4/32) \right) + \left(Ron(U+L) \times Io \times 20\% \times Io \times 20\% \times (4/32) \right) + \left(Ron(U+L) \times Io \times 20\% \times Io \times 20\% \times (4/32) \right) + \left(Ron(U+L) \times Io \times 20\% \times Io \times 20\% \times (4/32) \right) + \left(Ron(U+L) \times Io \times 20\% \times Io \times 20\% \times (4/32) \right) + \left(Ron(U+L) \times Io \times 20\% \times Io \times 20\% \times (4/32) \right) + \left(Ron(U+L) \times Io \times 20\% \times Io \times 20\% \times (4/32) \right) + \left(Ron(U+L) \times Io \times 20\% \times Io \times 20\% \times (4/32) \right) + \left(Ron(U+L) \times Io \times 20\% \times Io \times 20\% \times (4/32) \right) + \left(Ron(U+L) \times Io \times 20\% \times Io \times 20\% \times (4/32) \right) + \left(Ron(U+L) \times Io \times 20\% \times 1o \times 20\% \times (4/32) \right) + \left(Ron(U+L) \times Io \times 20\% \times 1o \times 20\% \times (4/32) \right) + \left(Ron(U+L) \times Io \times 20\% \times 1o \times 20\% \times (4/32) \right) + \left(Ron(U+L) \times Io \times 20\% \times 1o \times 20\% \times (4/32) \right) + \left(Ron(U+L) \times 1o \times 20\% \times (4/32) \right) + \left(Ron(U+L) \times 1o \times 20\% \times (4/32) \times (4/32) \right) + \left(Ron(U+L) \times 1o \times 20\% \times (4/32) \times (4$$

+
$$(Ron(U + L) \times Io \times 0\% \times Io \times 0\% \times (2/32)) \times 2$$

• 4W1-2 phase excitation

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P = V_{DD} \times I_{DD} + \{ (Ron(U + L) \times I_0 \times 100\% \times I_0 \times 100\% \times (2/64)) + (Ron(U + L) \times I_0 \times 98\% \times I_0 \times 98\% \times (4/64)) \}
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+ (Ron(U + L) \times Io \times 96\% \times Io \times 96\% \times (4/64)) + (Ron(U + L) \times Io \times 92\% \times Io \times 92\% \times (4/64))
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$$+ (Ron(U + L) \times Io \times 88\% \times Io \times 88\% \times (4/64)) + (Ron(U + L) \times Io \times 83\% \times Io \times 83\% \times (4/64))$$

$$+ (Ron(U + L) \times Io \times 77\% \times Io \times 77\% \times 4/64)) + (Ron U + L) \times Io \times 71\% \times Io \times 71\% \times (4/64))$$

$$+ (Ron(U + L) \times Io \times 63\% \times Io \times 63\% \times (4/64)) + (Ron(U + L) \times Io \times 56\% \times Io \times 56\% \times (4/64))$$

$$+ \left(Ron(U+L) \times Io \times 47\% \times Io \times 47\% \times (4/64) \right) + \left(Ron(U+L) \times Io \times 38\% \times Io \times 38\% \times (4/64) \right)$$

$$+ \; (Ron(U+L) \times Io \times 29\% \times Io \times 29\% \times (4/64)) \; + \; (Ron(U+L) \times Io \times 20\% \times Io \times 20\% \times (4/64))$$

$$+ \left(Ron(U+L) \times Io \times 10\% \times Io \times 10\% \times (4/64) \right) + \left(Ron(U+L) \times Io \times 10\% \times Io \times 10\% \times (2/64) \right) \} \times 2$$

(Notes)

V_{DD} = Power supply pin for control block

IDD = Supply current for control block

Ron(U + L) = Output on-resistance (Upper + lower)

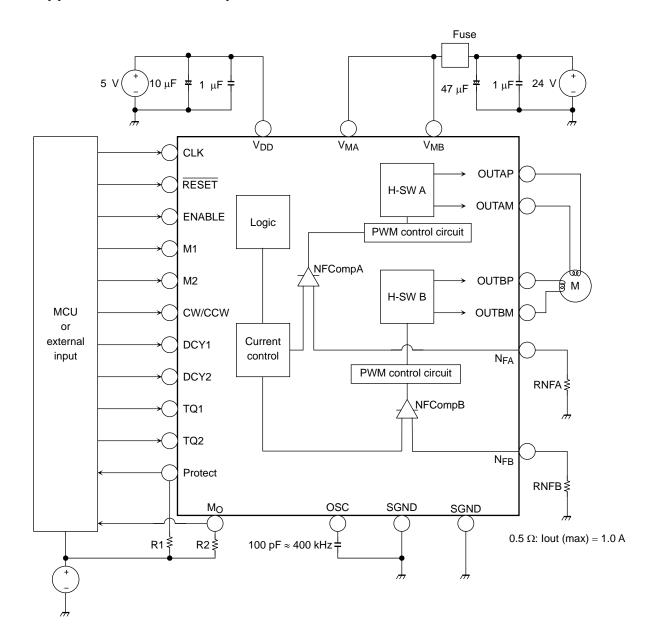
Io = Output current (Peak value of 100%)

Please confirm the operation in the actual operation conditions because thermal characteristics changes widely depending on the discharge characteristics of the board and the transient characteristics in the mounted state.

Heat loss can be promoted by taking the GND pattern of the print board widely. Usage of a heat sink is recommended to promote more heat loss.



6. Application Circuit Example



Note: Capacitors for the power supply lines should be connected as close to the IC as possible.

Usage Considerations

- A large current might abruptly flow through the IC in case of a short-circuit across its outputs, a
 short-circuit to power supply or a short-circuit to ground, leading to a damage of the IC. Also, the IC
 or peripheral parts may be permanently damaged or emit smoke or fire resulting in injury especially
 if a power supply pin (VDD, VMA and VMB) or an output pin (OUTAP, OUTAM, OUTBP and OUTBM)
 is short-circuited to adjacent or any other pins. These possibilities should be fully considered in the
 design of the output, VDD, VM, and ground lines.
- A fuse should be connected to the power supply line. The rated maximum current of the TB6560AFG is 2.5 A/phase. Considering those maximum ratings, an appropriate fuse must be selected depending on operating conditions of a motor to be used. Toshiba recommends that a fast-blow fuse be used.
- The power-on sequence described on page 2 must be properly followed.
- If a voltage outside the operating range specified on page 1 $(4.5 \le V_{DD} \le 5.5, 4.5 \le V_{MA/B} \le 34, V_{DD} \le V_{MA/B})$ is applied, the IC may not operate properly or the IC and peripheral parts may be permanently damaged. Ensure that the voltage range does not exceed the upper and lower limits of the specified range.

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(1) Capacitors for the Power Supply Lines

Capacitors for the power supply lines between VDD and GND should be connected as close to the IC as possible.

Recommended Value

Characteristic	Recommended Value	Remarks
V _{DD} – GND	10 μF to 100 μF	Electrolytic capacitor
	0.1 μF to 1 μF	Ceramic capacitor

(2) Capacitors for V_M Terminal

Capacitors for V_M terminal between V_M and GND should be connected as close to the IC as possible.

Recommended Value

Characteristic	Recommended Value	Remarks
V _M – GND	10 μF to 100 μF	Electrolytic capacitor
	0.1 μF to 1 μF	Ceramic capacitor

(3) Resistances for NFA and NFB Terminals

The resistance of NFA terminal (RNFA) and that of NFB terminal (RNFB) determine the maximum current of phase A and B.

The reference current for the constant current operation should be set by the external resistance. When voltage for NFA and NFB terminals become 0.5~V or more (in case torque is 100~%.), it stops charging and the current which is over the reference value does not flow.

Iout (A) = 0.5 V/RNF (Ω)

Example: When the maximum current is 1 A, external resistance is 0.5 Ω .

(4) Adjusting the External Capacitor Value (C_{OSC}) and Minimum Clock Pulse Width ($t_{w (CLK)}$)

A triangular-wave is generated internally by CR oscillation. The capacitor is externally connected to the OSC pin. The recommended capacitor value is between 100 pF and 1000 pF.

Approximate equation: $f_{OSC} = 1/\{C_{OSC} \times 1.5 \times (10/C_{OSC} + 1)/66\} + 1000 \text{ kHz}$ (Since this is an approximation formula, the calculation result may not be exactly equal to the actual value.)

The approximate values are shown below.

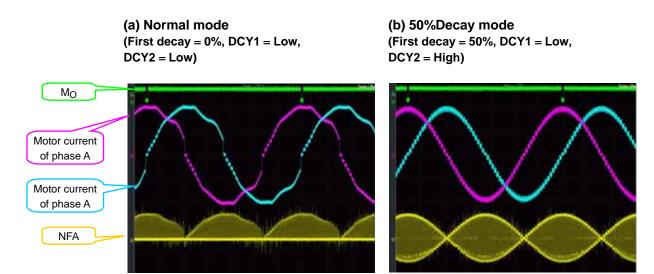
The minimum clock pulse width $(t_{W(CLK)})$ corresponds to the external capacitor (C_{OSC}) as follows:

Capacitor	Oscillating Frequency	Minimum Clock Pulse Width t _{w (CLK)}) (Note)
1000 pF	44 kHz	90 μs
330 pF	130 kHz	30 μs
100 pF	400 kHz	10 μs

Note: When the frequency of an input clock signal is high, the C_{OSC} value should be small so that the duty cycle of an input clock pulse does not become extremely high (should be around 50% or lower).

(5) To set decay mode (current decay by DCY1 and DCY2 terminals), set the appropriate mode by monitoring the waveform of motor coil current. The appropriate mode depends on the conditions (usage motor, power supply voltage, CLK frequency, and so on).

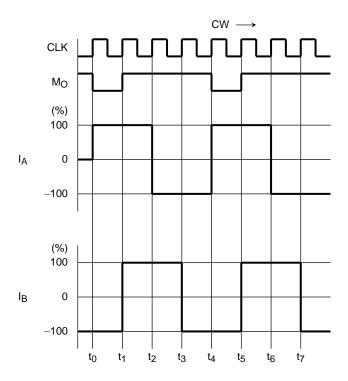
Example: Set current decay



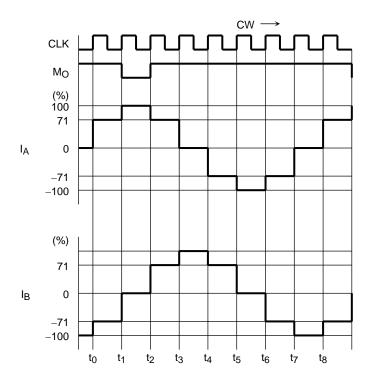
7. Excitation Mode Setting

The excitation mode can be selected from 2 phase, 1-2 phase, 2W1-2 phase, and 4W1-2 phase modes using the M1 and M2 inputs. It is capable of forward and reverse driving of a two-phase bipolar stepping motor with CW and CCW terminals using only a clock signal.

2-Phase Excitation (M1: L, M2: L, CW mode)

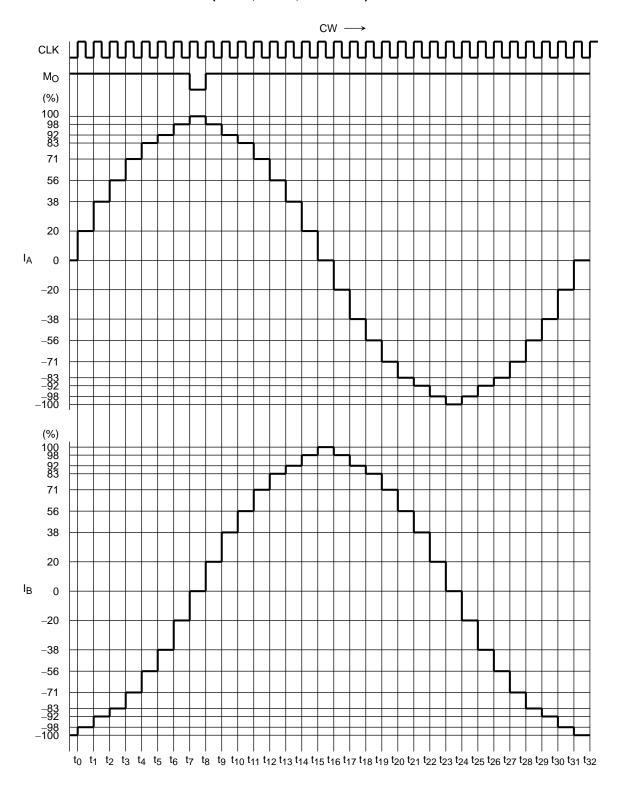


1-2 Phase Excitation (M1: H, M2: L, CW mode)

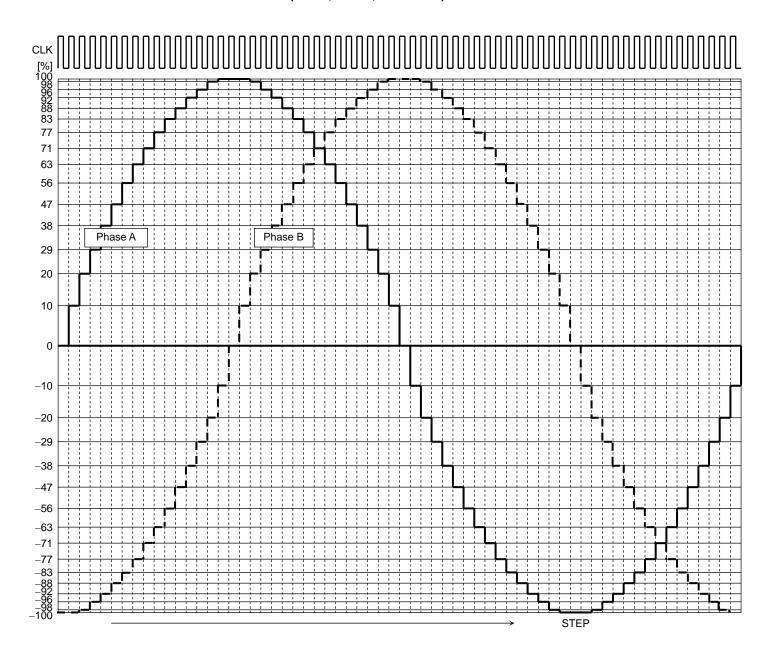


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2W1-2 Phase Excitation (M1: H, M2: H, CW mode)

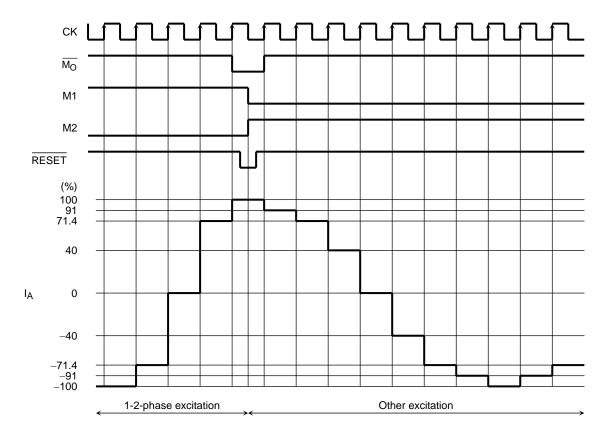


4W1-2 Phase Excitation (M1: L, M2: H, CW mode)



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Input Signal Example



It is recommended that the state of the M1 and M2 pins be changed after setting the \overline{RESET} signal Low during the Initial state ($\overline{M_O}$ = Low). Even when the $\overline{M_O}$ signal is Low, changing the M1 and M2 signals without setting the \overline{RESET} signal Low may cause a discontinuity in the current waveform.



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