TB6643KQ Usage Considerations

The TB6643KQ is a full-bridge driver IC for a DC motor with output transistors that employ a MOS structure.
Low ON-resistance MOSFETs and a PWM control help the TB6643KQ exhibit lower heat generation thus efficient motor drive.
Furthermore, the TB6643KQ has two inputs, IN1 and IN2, which allow for selection of the four operation modes: forward (clockwise), reverse (counter-clockwise), short brake and stop modes.

1. Power Supply Voltage

(1) Operating Power Supply Voltage Range

The absolute maximum voltage rating of the TB6643KQ is 50 V. However, when it is actually used, the operating supply voltage must fall within the range between 10 V and 45 V.

(2) Power-ON/Power-OFF

Having a single VM as its power supply and the undervoltage lockout circuit, the TB6643KQ has no special procedures for turning on and off itself. However, unstable power supplies result in abnormal IC operations. Therefore, it is recommended to run the motor after ensuring both the IN1 and IN2 are in Low states, and subsequently turn the IC on with the stable VM. Then the motor rotational direction should be controlled by switching the inputs.
It is likewise recommended to turn off the TB6643KQ after the motor movement is completely stopped.

2. Output Current

Note that the absolute maximum output current rating of the TB6643KQ varies with the VM. OUT1 and OUT2 must be kept under 4.5 A when VM = 36 V; they must be kept under 4.0 A when VM < 36 V.
Also, the usage conditions such as the ambient temperature, presence or absence of a heatsink, board layout and IC mount technique have effect on increase and decrease of the available average output current. The TB6643KQ must be used with the absolute maximum output current rating of 4.0 A when T_j = 150°C or with the average output current of less than 4.5 A.

3. Control Inputs

IN1, IN2 Inputs
Even thought there are pulse inputs to IN1 and IN2, they never seep into VM as long as the VM power supply is turned off; thus the TB6643KQ will never be turned on.

Before releasing the TSD and ISD circuits, keep driving the IN1 and IN2 Low for more than 1 μs.

4. PWM Frequency

Switching input through either one of IN1 and IN2 pins allows for the PWM control of the motor rotation speed.

The motor controlled by the PWM frequency runs alternately in Normal mode and Short brake mode.

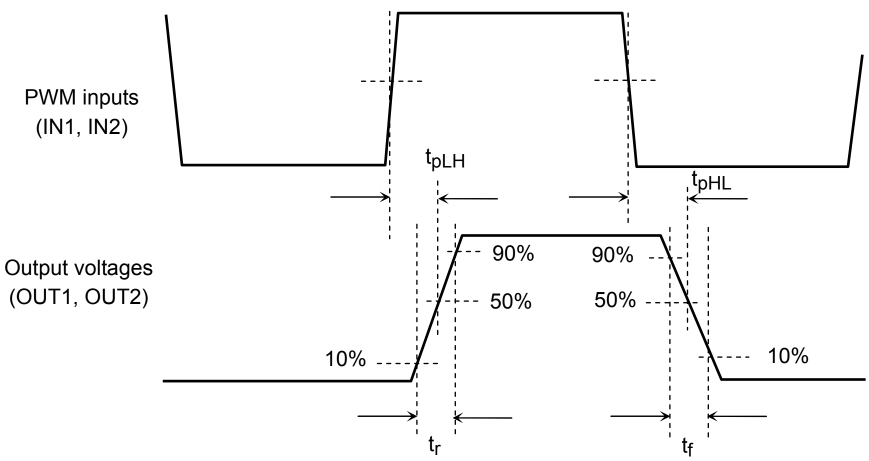
The TB6643KQ internally generates the blank times of 200 ns and 500 ns (typ.) on the ON-OFF switching time of the upper and lower power transistors for preventing the shoot-through current that occurs otherwise on overlap of the ON states of the upper and lower power transistors. Therefore, the PWM control with the synchronous rectification is available without external off time input.

In this document, the operational range of the PWM frequency is stated as 100 kHz. However, in actual operations, the output voltage will be distorted with respect to the input current even the TB6643KQ runs within the stated operating range as shown in the switching characteristics below.

The TB6643KQ can support the frequency of even over 100 kHz only as far as its output distortions with respect to the inputs and the duty gaps are taken into account when it is used.

Note that the values of the following switching characteristics are given as typical values. The TB6643KQ must be used with a sufficient safety margin because they vary with power supply voltages, temperatures and IC variation.

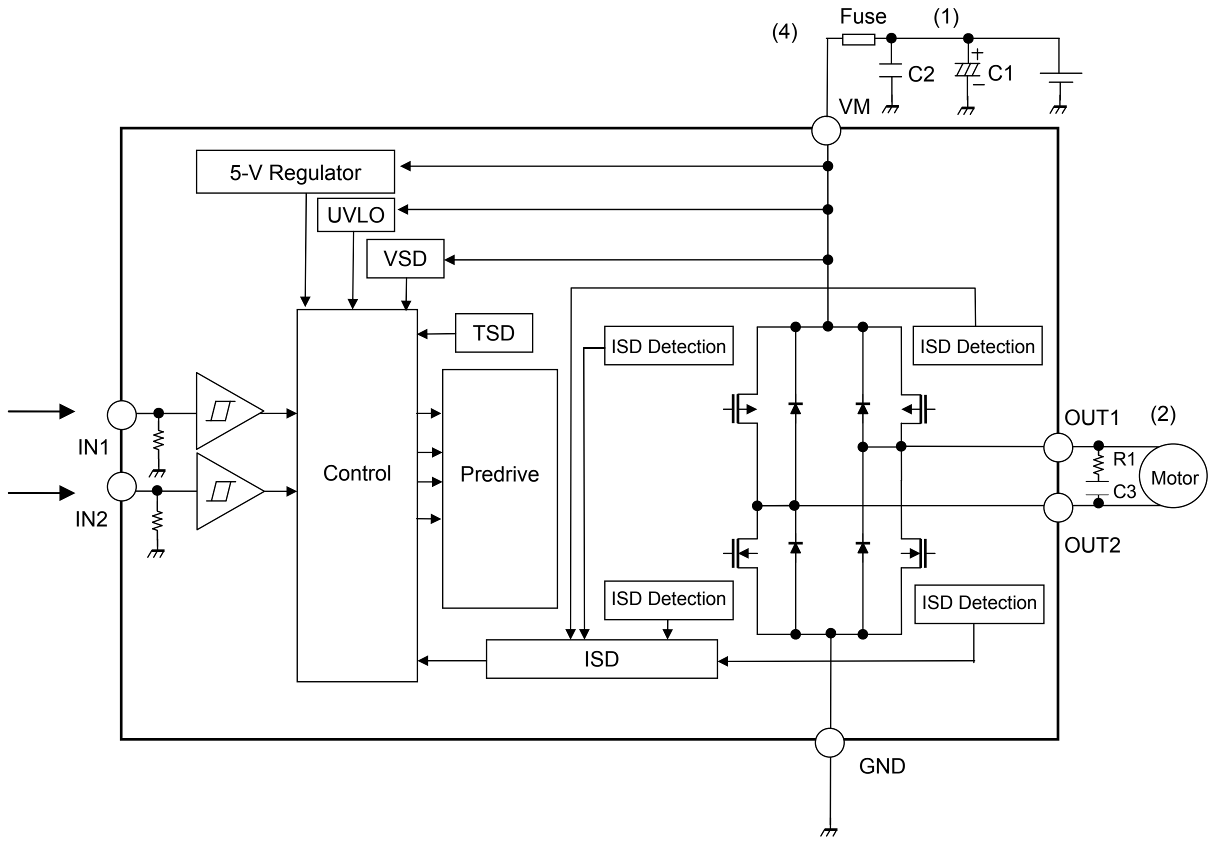
Switching Characteristics



VM = 24 V   Ta = 25°C

Characteristics	Value	Unit
t_{pLH}	650 (typ.)	ns
t_{pHL}	450 (typ.)	
t_r	90 (typ.)	
t_f	130 (typ.)	

5. Application Circuit



(1) Capacitors Connected to the Power Supply Pin

Connect the capacitors between VM and GND as near the IC as possible.

Recommended Values

Characteristics	Symbol	Recommended Value	Remarks
VM – GND	C1	10 μF to 100 μF	Electrolytic capacitor
	C2	0.001 μF to 1 μF	Ceramic capacitor

(2) Capacitor and Resistor Between the Outputs

Connect the R1 resistor and the C3 capacitor only for removing the brush noise of the motor. If so, limit the current by using R1 because the outputs momentarily move to the short circuit mode in conduction if C3 is not charged.

(3) VM, OUT1, OUT2 and GND

Sufficient space must be kept to design the wiring pattern of these pins; particularly for GND, a space large enough must be secured.

(4) Fuse

For preventing a continuous flow of a large current due to overcurrent or IC damages, an appropriate fuse must be placed in the power supply of the TB6643KQ.

The TB6643KQ is may fail because of illegal use such as exceeding the absolute maximum ratings, incorrect wirings and abnormal pulse noise induced by wirings and loads. As a result, a large current continuously flows into the TB6643KQ leads to smoking and ignition. To make these negative impacts as small as possible, appropriate control of the capacitance and weld time of the fuse as well as positioning of the fuse in the circuit is required.

The TB6643KQ incorporates an overcurrent detection circuit (ISD). However, it does not necessarily protect the TB6643KQ in any case. On activation of the ISD circuit, overcurrent conditions must be removed immediately. Depending on the usage and the use environment of the TB6643KQ, like using it with the absolute maximum ratings being exceeded, the ISD circuit may not operate correctly; or the TB6643KQ may be broken before the ISD circuit is activated. Even after the activation of the ISD circuit, the TB6643KQ may be destroyed due to the IC heating if overcurrent continues flowing too long.

There is a concern that a secondary destruction of the IC due to continuous overcurrent may occur. Another concern is that the ISD circuit may not run due to its blank time, interacting with the output load conditions. Toshiba, therefore, describes in the specification that the ISD circuit does not necessarily run in any case as one of the usage considerations.

For instance, if a current that neither reaches the absolute maximum output current rating nor infringes the lower limit of the operating voltage of the ISD circuit continues flowing, the DMOS transistors in the output stage will be degraded. On the other hand, if once a current exceeding the absolute maximum output current rating flows through the DMOS transistors in the output stage, they are degraded as well. Therefore, even though the TB6643KQ is not broken after a single overcurrent detection, it may be broken after two or three times of overcurrent detection because repeated detections will deepen the DMOS degradation.

Toshiba recommends the use of a fuse in the power supply to cope with such a secondary destruction.

(5) Metal Parts

The metal parts on the rear surface of the TB6643KQ help release the IC heat. Attaching a heatsink to these metal parts can lower the power dissipation of the TB6643KQ. Therefore, the heat protection must be considered when designing the board layout.

Also, these metals are electrically connected to the rear surface of the TB6643KQ; thus they must be insulated or shorted to GND.

6. Power Dissipation

The power loss of the TB6643KQ can be roughly estimated by the following equations.

(1) When PWM Duty = 100%

$P = VM \times I_{CC} + I_O^2 \times R_{ON}$ (U + L)

For example, when VM = 24 V and the output current, I_O = 0.5 A (For I_{CC} and R_{ON} (U + L), refer to the electrical characteristics on the datasheet.)

P (typ.) = 24 V × 2.5 mA (typ.) + (0.5 A)^2 × 0.55 Ω (typ.) = 0.1975 W
P (max) = 24 V × 8 mA (max) + (0.5 A)^2 × 0.9 Ω (max) = 0.417 W

(2) When Using the PWM Control

The power dissipation when using the PWM control can be roughly calculated as follows:
(Switching loss occurring actually is not considered.)

$P = VM \times I_{CC} + I_O^2 \times R_{ON}$ (U + L) × PWM duty

Mutual relationship of the ambient temperature, Ta, and the junction temperature, T_j, are roughly estimated by the following equation:

$T_j = P \times R_{th\ (j\text{-}a)} + Ta$

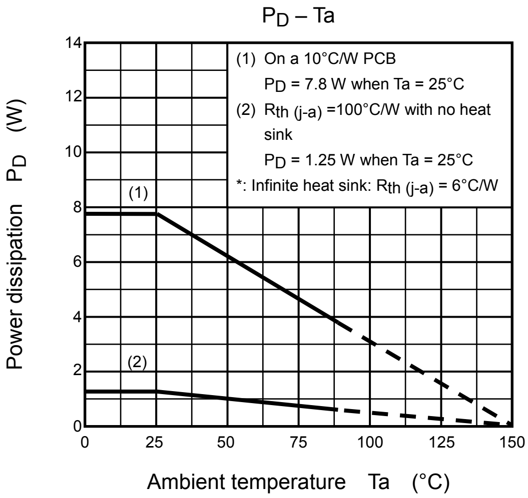
*: $R_{th\ (j\text{-}a)}$: Heat resistance between the junction and ambient temperatures

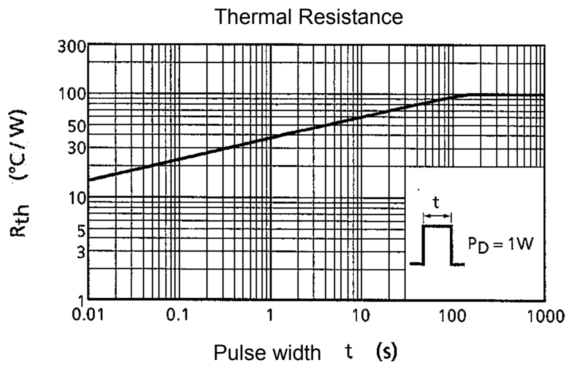
*: Ta: Ambient temperature (Stable ambient temperature avoiding the affect of any heat radiation)

For example, when $R_{th\ (j\text{-}a)}$ = 100°C/W, Ta = 85°C, P (max) = 0.417 W, then

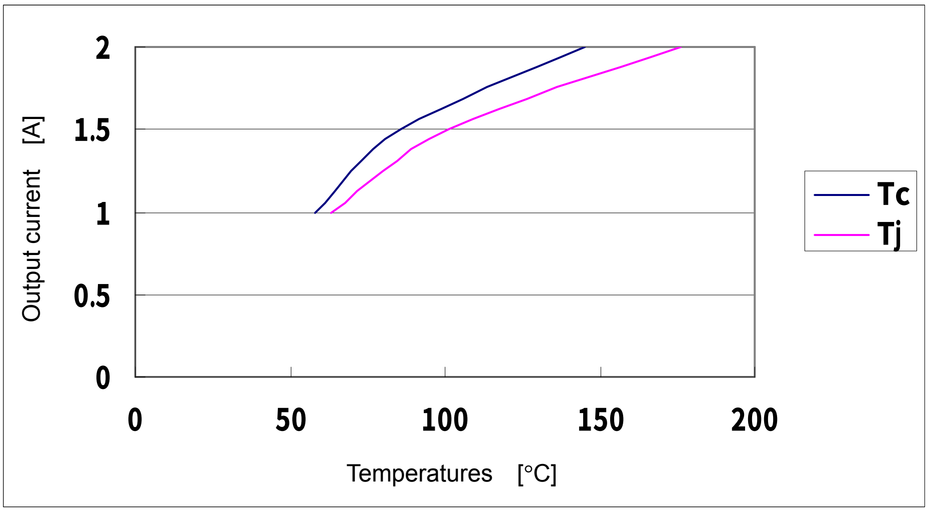
T_j = 0.417 W × 100°C/W + 85°C = 126.7°C

Care must be taken for $R_{th\ (j\text{-}a)}$ which is dependent on use conditions such as a board mount method.
Higher the ambient temperature is, smaller will be the power dissipation.
Note that the equations described in this document are only the ways to find out rough estimation. A sufficient evaluation of the TB6643KQ with the junction temperature less than 150°C is required for using the TB6643KQ with a full safety margin.





The test curves of the package surface temperature, T_C [°C], and the junction temperature, T_j [°C], when Ta = 25°C and current flows between the OUT1 and OUT2 outputs on a PCB are shown below:



Conditions: Ta = 25°C VM = 24 V IN2 = 5 V, IN1 = −100 μA (Diode voltage monitor circuit), on a PCB with no heat sink

Used PCB: Glass epoxy board 70 × 50 × 1.6 (mm), a double-sided PCB, Cu 67%, Cu thickness 50 μm

Top View

Bottom View

The test curves shown above are only typical ones. They fluctuate depending on power supply voltages, temperatures and IC variation.

Also, the conditions such as board mount method and running motors affect the results; therefore the TB6643KQ must be used after a sufficient evaluation and provided with a safety margin before used.

Care must be taken for the junction temperature to be kept less than 150°C.

7. Pin Shorting

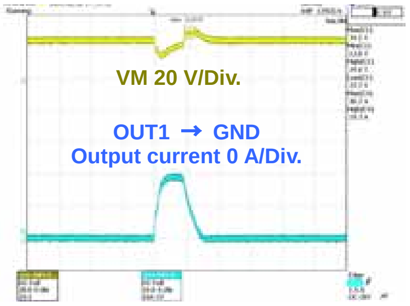
The results of evaluations performed by Toshiba are listed below.
The TB6643KQ has never been destroyed even when the following pairs of the pins are shorted together. However, amount of current flow on short depends on power supply impedance and shorted wiring impedance.
Furthermore, whether or not the TB6643KQ is destroyed depends on the power supply voltage, temperature and the IC variation. Therefore, a sufficient evaluation of the TB6643KQ in your application and providing a safety margin are required.
For your information and guidance, the TB6643KQ was destroyed when tested under the Load Short 2 condition with VM = 36 V.

Shorting Condition	Shorted Pin Names	IC Condition
OUT1 to GND	OUT1 – GND	Not destroyed
OUT1 to supply	OUT1 – VM	Not destroyed
OUT2 to GND	OUT2 – GND	Not destroyed
OUT2 to supply	OUT2 – VM	Not destroyed
Load short 1	OUT1: High – OUT2: Low	Not destroyed
Load short 2	OUT1: Low – OUT2: High	Not destroyed

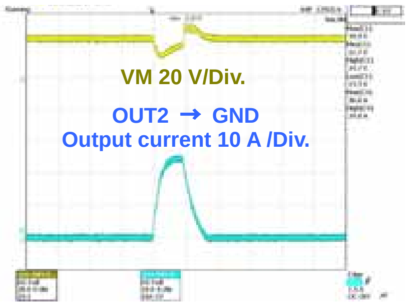
Shorting Condition	Shorted Pin Names	IC Condition
1 – 2	IN1 – IN2	Not destroyed
2 – 3	IN2 – OUT1	Not destroyed
3 – 4	OUT1 – GND	Not destroyed
4 – 5	GND – OUT2	Not destroyed
5 – 6	OUT2 – N.C	Not destroyed
6 – 7	N.C – VM	Not destroyed

Conditions: VM = 24 V, Ta = 25°C, between VM and GND: Electrolytic capacitor of 10 μF + ceramic capacitor of 0.1 μF

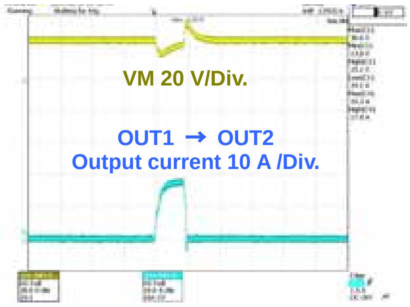
OUT1 Shorted to Ground Waveforms, OUT1-GND



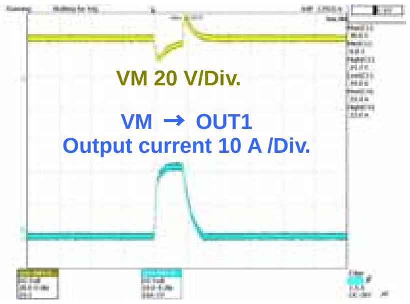
OUT2 Shorted to Ground Waveforms, OUT2-GND



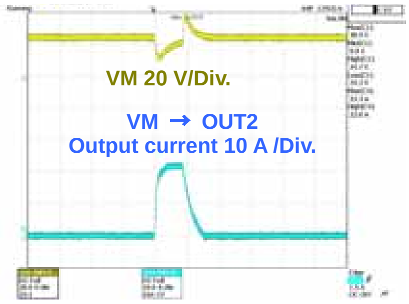
Load Short 1 Waveforms, OUT1: High-OUT2: Low



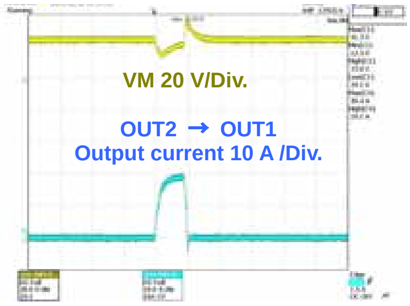
OUT1 Shorted to Supply Waveforms, OUT1-VM



OUT2 Shorted to Supply Waveforms, OUT2-VM



Load Short 2 Waveforms, OUT1: Low-OUT2: High



Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.
Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.

5. Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on Handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

(3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

(4) Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

Points to Remember on Handling of ICs

(1) Over current Protection Circuit

Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Over current protection circuits operate against the over current, clear the over current status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

(2) Thermal Shutdown Circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately. Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

(3) Heat Radiation Design

In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (TJ) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(4) Back-EMF

When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor’s power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device’s motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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