TB6641FG Usage Considerations

The TB6641FG is a full-bridge driver IC for a DC motor providing output transistors that employ a MOS structure.

Low ON-resistance MOSFETs and a PWM control help the TB6641FG exhibit lower heat generation thus efficient motor drive.

Furthermore, the TB6641FG has two inputs, IN1 and IN2, which allow for selection of the four operation modes; forward (clockwise), reverse (counter-clockwise), short brake, and stop modes.

1. Power Supply Voltage

(1) Operating Power Supply Voltage Range

The absolute maximum voltage rating of the TB6641FG is 50 V. However, when it is actually used, the operating supply voltage must fall within the range between 10 V and 45 V.

(2) Power-ON/Power-OFF

Having a single VM as its power supply and the undervoltage lockout circuit, the TB6641FG has no special procedures for turning on and off itself. However, unstable power supplies result in abnormal IC operations. Therefore, it is recommended to run the motor after ensuring both the IN1 and IN2 are in Low states, and subsequently turn the IC on with the stable VM. Then the motor rotational direction should be controlled by switching the inputs.

It is likewise recommended to turn off the TB6641FG after the motor movement is completely stopped.

2. Output Current

Note that the absolute maximum output current rating of the TB6641FG varies with the VM. OUT1 and OUT2 must be kept under 4.5 A when VM = 36 V; they must be kept under 4.0 A when VM < 36 V.

Also, the usage conditions such as the ambient temperature, presence or absence of a heatsink, board layout and IC mount technique have effect on increase and decrease of the available average output current. The TB6641FG must be used with the absolute maximum output current rating of 4.0 A when T_j = 150°C or with the average output current of less than 4.5 A.

3. Control Inputs

Even if there are pulse inputs to IN1, IN2, PWM and VREF, they never seep into VM as long as when the VM power supply is turned off; therefore the TB6641FG will never be turned on.

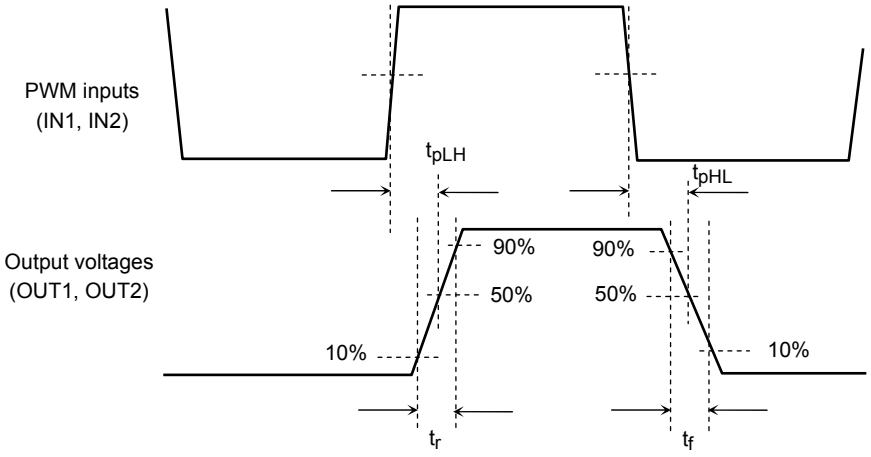
Before releasing the TSD and ISD circuits, keep driving the IN1 and IN2 Low for more than 1 µs.

4. PWM Frequency

The PWM input through the PWM pin allows for the motor speed control.
(The PWM control is also accomplished by the PWM input through the IN1 and IN2 pins instead of the PWM pin.)
The motor controlled by the PWM frequency runs alternately in Normal mode and Short brake mode.
The TB6641FG internally generates the blank time when the upper and lower power transistors in the output circuit switch on and off so as to prevent the shoot-through current that occurs otherwise on overlap of the ON states of the upper and lower power transistors.
Therefore, the PWM control with the synchronous rectification is available without externally off time input.

In this document, the operational range of the PWM frequency is stated as 100 kHz. However, in actual operations, the output voltage will be distorted with respect to the input current even the TB6641FG runs within the stated operating range as shown in the switching characteristics below.
The TB6641FG can support the frequency of even over 100 kHz only as far as its output distortions with respect to the inputs and the duty gaps are taken into account when it is used.
Note that the values of the following switching characteristics are given as typical values. The TB6641FG must be used with a sufficient safety margin because they vary with power supply voltages, temperatures and IC variation.

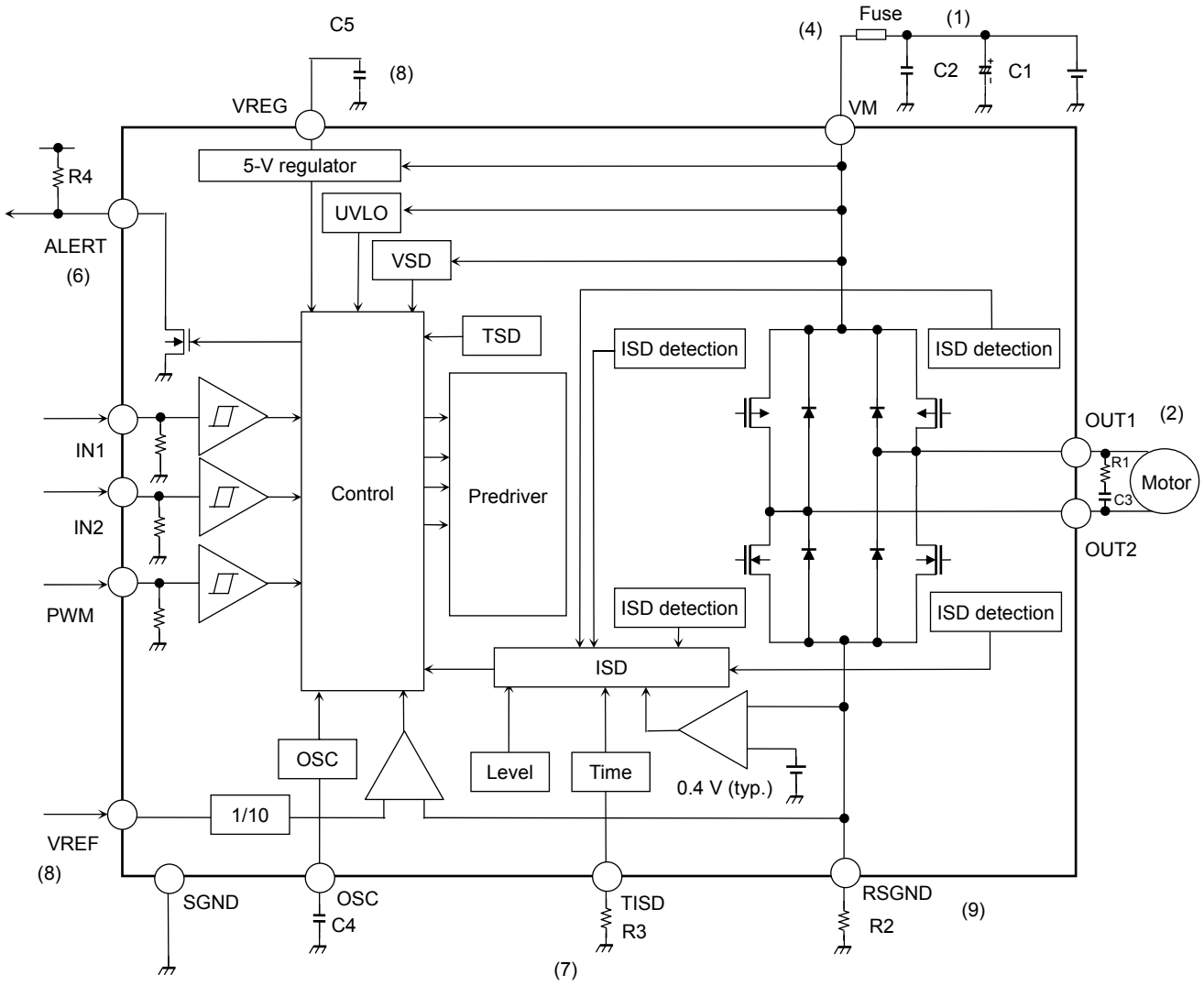
Switching Characteristics



VM = 24 V Ta = 25°C

Characteristics	Value	Unit
t_{pLH}	650 (typ.)	ns
t_{pHL}	450 (typ.)	
t_r	90 (typ.)	
t_f	130 (typ.)	

5. Application Circuit



(1) Capacitors Connected to the Power Supply Pin

Connect the capacitors between VM and GND as near the IC as possible.

Recommended Values

Characteristics	Symbol	Recommended Value	Remarks
VM – GND	C1	10 μF to 100 μF	Electrolytic capacitor
	C2	0.1 μF to 1 μF	Ceramic capacitor

(2) Capacitor and Resistor Between the Outputs

Connect the R1 resistor and the C3 capacitor only for removing the brush noise of the motor. If so, limit the current by using R1 because the outputs momentarily move to the short circuit mode in conduction if C3 is not charged.

(3) Routing of VM, OUT1, OUT2 and RSGND

The motor causes a large current flow through the TB6641FG. Therefore, sufficient space must be secured on designing the IC wiring pattern. Particularly for RSGND and SGND, a space large enough for their connections to GND must be secured so as not to be affected by wiring impedance.

(4) Fuse

For preventing a continuous flow of a large current due to overcurrent or IC damages, an appropriate fuse must be placed in the power supply of the TB6641FG.

The TB6641FG may fail because of illegal use such as exceeding the absolute maximum ratings, incorrect wirings and abnormal pulse noise induced by wirings and loads. As a result, a large current continuously flows into the TB6641FG leads to smoking and ignition. To make these negative impacts as small as possible, appropriate control of the capacitance and weld time of the fuse as well as positioning of the fuse in the circuit is required.

The TB6641FG incorporates an overcurrent detection circuit (ISD). However, it does not necessarily protect the TB6641FG in any case. On activation of the ISD circuit, overcurrent conditions must be removed immediately. Depending on the usage and the use environment of the TB6641FG, like using it with the absolute maximum ratings being exceeded, the ISD circuit may not operate correctly; or the TB6641FG may be broken before the ISD circuit is activated. Even after the activation of the ISD circuit, the TB6641FG may be destroyed due to the IC heating if overcurrent continues flowing too long.

There is a concern that a secondary destruction of the IC due to continuous overcurrent may occur. Another concern is that the ISD circuit may not run due to its blank time, interacting with the output load conditions. Toshiba, therefore, describes in the specification that the ISD circuit does not necessarily run in any case as one of the usage considerations.

For instance, if a current that neither reaches the absolute maximum output current rating nor infringes the lower limit of the operating voltage of the ISD circuit continues flowing, the DMOS transistors in the output stage will be degraded. On the other hand, if once a current exceeding the absolute maximum output current rating flows into the DMOS transistors in the output stage, they are degraded as well. Therefore, even though the TB6641FG is not broken after a single overcurrent detection, it may be broken after two or three times of overcurrent detection because repeated detections will deepen the DMOS degradation.

Toshiba recommends the use of a fuse in the power supply to cope with such a secondary destruction.

(5) FIN

FIN plays a role as a heatsink. The heat protection must be considered when designing the board layout. (FIN is electrically connected to the rear surface of the chip; thus must be insulated or shorted to GND.)

(6) ALERT Pin

The ALERT pin behaves as an open-drain output that has a pull-up resistor in an external power source to send out the High state. When the Low state is sent out on the ALERT pin, the TB6641FG operates normally. The High state (High-impedance) on the ALERT pin indicates some failure of the TB6641FG operation (UVLO, TSD, VSD and/or ISD is running).

It is recommended to use a pull-up resistor of 10 kΩ to 100 kΩ.

(7) Resistor set for TSID pin

One ISD detection feature is provided for each of the four output power transistors.

Detection current is programmed 7A (typ.) (4.5A to 10A) internally. If any one of the four ISD detection runs over the ISD detection time (mask time), it turns off all the output power transistors (puts them in High-impedance state).

The resistor control of the TISD pin enables the ISD detection time (mask time) tuning.

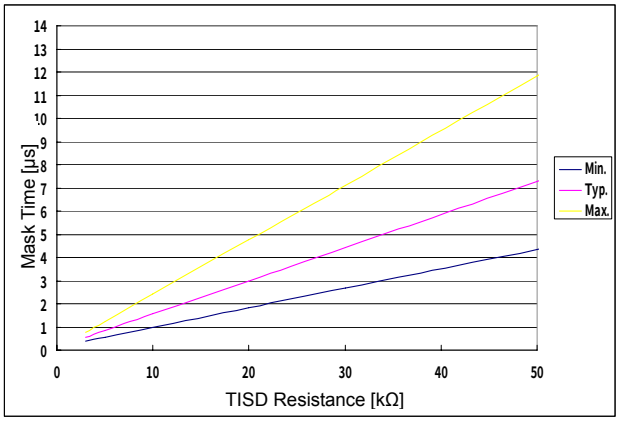
Driving both the IN1 and IN2 pins Low releases the ISD detection and brings the TB6641FG back to the normal operation.

The change of the external resistor values of the TISD pin with respect to the ISD mask time is shown below in graph form as a guide.

The mask time must be controlled through the TISD pin so as to be long enough for preventing incorrect operations of the TB6641FG due to noises; and it must be controlled so as to be short enough for preventing the IC destruction upon overcurrent detection.

The resistor provided for the TISD pin must be controlled to be over 5 kΩ. When disabling the overcurrent detection feature, the TISD pin must be connected to GND.

**External Resistor Value of the TISD Pin –
ISD Mask Time Curves (given as a guide)**



Note: The complementary output circuit consists of N-channel and P-channel DMOS transistors, thus the ISD current thresholds show slight differences.

(8) Capacitors Connected to VREG Pin

Connect the capacitors between VREG and GND as near the IC as possible.

Recommended Values

Characteristics	Symbol	Recommended Value	Remarks
VREG-GND	C5	100pF to 0.01 µF	Ceramic capacitor

(9) Calculations for Constant Current PWM Control of the RSGND and VREF Pins

The constant current PWM control frequency is determined by the peak current in the constant current operations caused by the voltage across the VREF pin. The peak current values are calculated by the following equation:

I_O = VREF/R2 × 1/10 [A] For example, if R2 = 0.2 Ω, and VREF = 2 V, then I_O = 1 A

The constant current PWM frequency is also configurable by controlling the capacitor of the OSC pin. The oscillation frequency is approximated by the following equation:

fosc [Hz] (typ.) = 0.42/ (Cosc [F] × 10^3) For example, if C4; Cosc = 1800 pF, then fosc = 233 kHz

The OSC frequency must be configured to be less than 500 kHz. If it is configured higher than 500 kHz, the switching loss of the output stages controlled by the PWM frequency becomes larger. Note, however, that if the OSC frequency is too low, the PWM frequency may fall within the audible range.

Sufficient safety margin must be secured because the PWM frequency varies with the power supply voltage, temperature and IC variation.

The RSGND pin with the resistor for detecting overvoltage will turns off all the output transistors (puts them in High-impedance state) when the voltage exceeds 0.4 V (typ.); and remainder of its control shall be the same as that of the ISD circuit. At this time, also the ALERT pin is driven High. To return the TB6641FG to Normal operation mode, the overvoltage detection must be released by pulling both the IN1 and IN2 pins Low.

For the RSGND pin, it is recommended to use an overvoltage detection resistor of over 0.1 Ω.

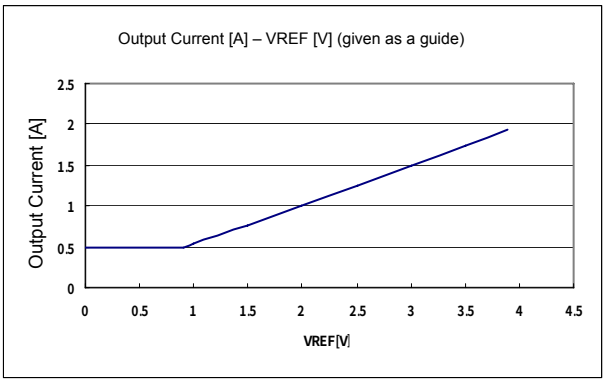
The voltage across the detection resistor will be compared to the reference voltage across the SGND pin. Therefore, the overvoltage detection resistor of the RSGND must be installed near the RSGND pin and SGND pin but not to be affected by wiring impedance.

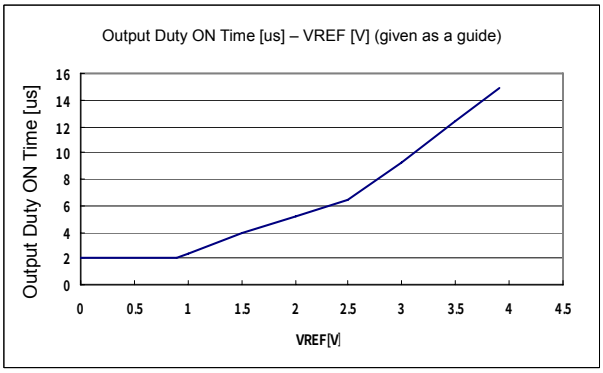
When the constant current PWM control is not used, the RSGND pin must be shorted to the SGND pin instead of connected to the R2 resistor.

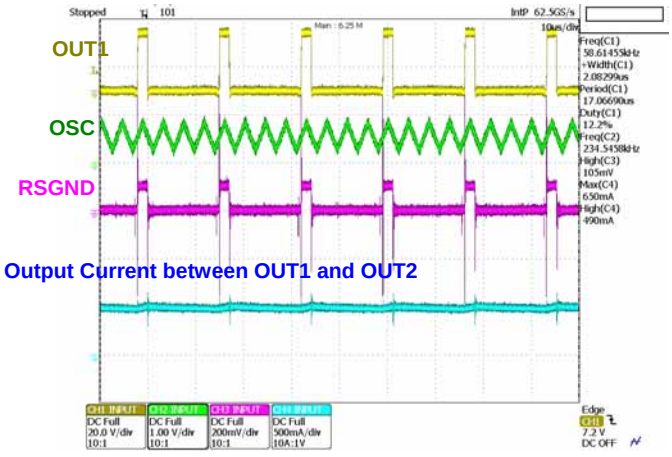
In this case, sufficient space must be secured between the RSGND pin and the SGND pin; otherwise wiring impedance generated between these pins will work like a detection resistor. As a result, the motor moves as if its speed is controlled by a constant current PWM frequency.

The characteristics curves of the output current and the output duty ON time with respect to VREF respectively in addition to their active waveforms are shown below.

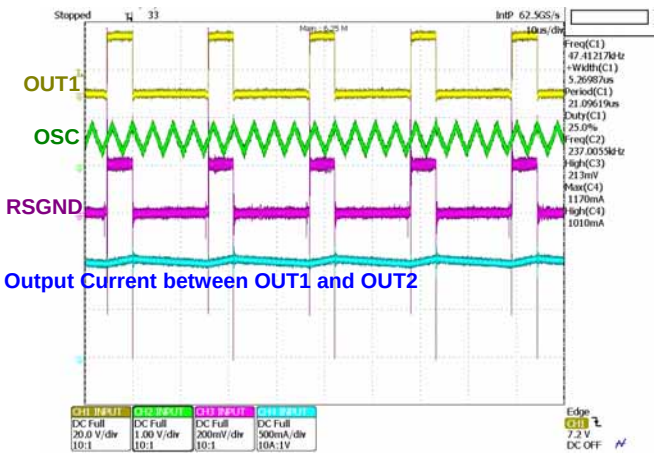
For prevention of abnormal operations due to noise, the duty ON time of about 2 µs is provided by default. Note that the offset current is provided at the output. Output offset currents vary with amount of loads. As for the load conditions shown below (a resistor and a load of 5Ω + 2 mH), the nominal offset is 0.5 A.







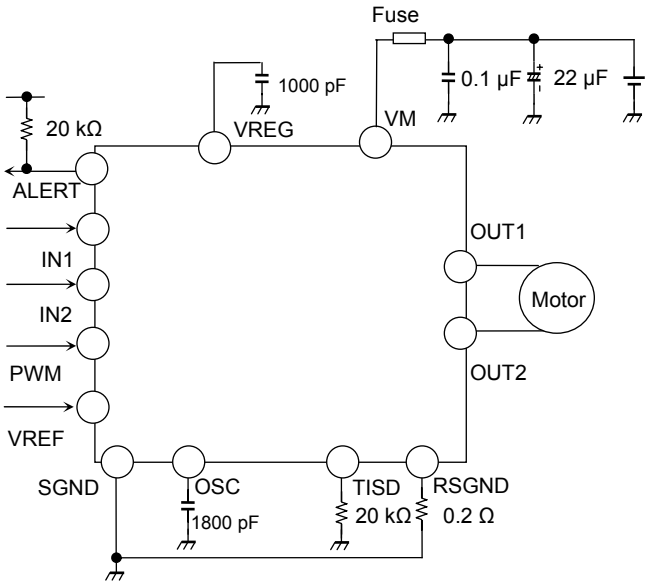
Reference waveforms when VREF = 0 V



Reference waveforms when VREF = 2.0 V

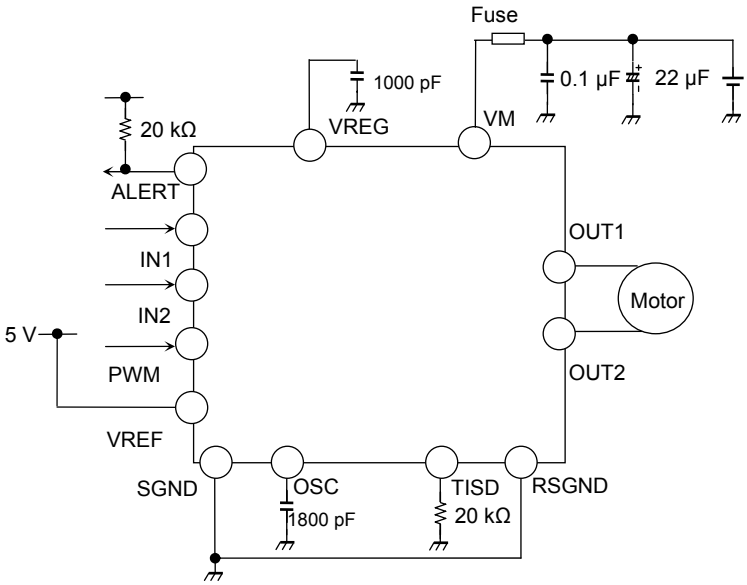
Conditions: VM = 24 V, OSC = 1800 pF, RSGND; 0.2 Ω, IN1 = H, IN2 = L,
VREF = any value, Loads; 5 Ω + 2 mH

Application Circuit Example When Using Constant Current PWM Control



Application Circuit Example When NOT Using Constant Current PWM Control

The RSGND pin must be shorted to the SGND pin, and the VREF pin must be pulled High (5 V).



6. Power Dissipation

The power loss of the TB6641FG can be roughly estimated by the following equations:

(1) When PWM Duty = 100%

$P = VM \times I_{CC} + I_O^2 \times R_{ON}\ (U + L)$

For example, when VM = 24 V and the output current, I_O = 0.5 A (For I_{CC} and R_{ON} (U + L), refer to the electrical characteristics on the data sheet.)

P (typ.) = 24 V × 2.5 mA (typ.) + (0.5 A)² × 0.55 Ω (typ.) = 0.1975 W
P (max) = 24 V × 8 mA (max) + (0.5 A)² × 0.9 Ω (max) = 0.417 W

(2) When using the PWM control

The power dissipation when using the PWM control can be roughly calculated as follows: (Switching loss occurring actually is not considered.)

$P = VM \times I_{CC} + I_O^2 \times R_{ON}\ (U + L) \times$ PWM duty

Mutual relationship of the ambient temperature, Ta, and the junction temperature, T_j, are roughly estimated by the following equation:

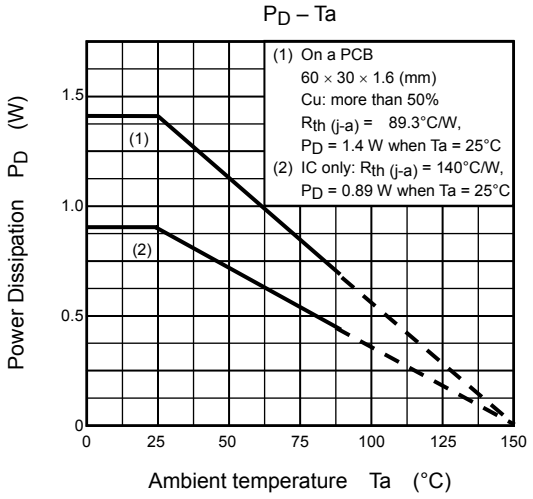
$T_j = P \times R_{th\ (j\text{-}a)} + Ta$

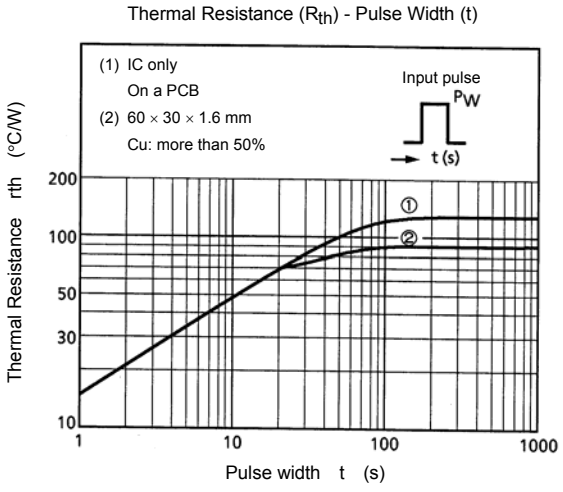
*: $R_{th\ (j\text{-}a)}$: Heat resistance between the junction and ambient temperatures

*: Ta: Ambient temperature (Stable ambient temperature avoiding the affect of any heat radiation)

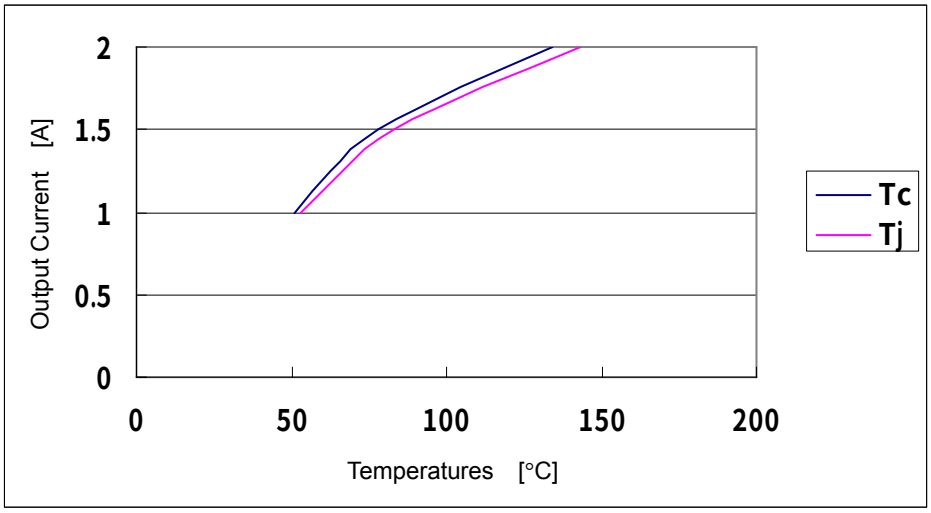
For example, when $R_{th\ (j\text{-}a)}$ = 89.3°C/W, Ta = 85°C, P (max) = 0.417 W, then
T_j = 0.417 W × 89.3°C/W + 85°C = 122.24°C

Care must be taken for $R_{th\ (j\text{-}a)}$ which is dependent on use conditions such as a board mount method.
Higher the ambient temperature is, smaller will be the power dissipation.
Note that the equations described in this document are only the ways to find out rough estimation. A sufficient evaluation of the TB6641FG with the junction temperature less than 150°C is required for using the TB6641FG with a full safety margin.



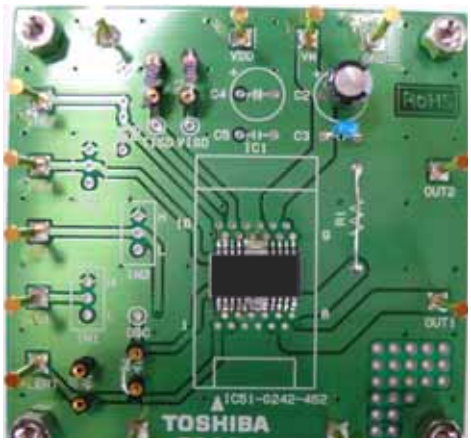


The test curves of the package surface temperature, T_C [°C], and the junction temperature, T_j [°C], when Ta = 25°C and current flows between the OUT1 and OUT2 outputs on a PCB are shown below:

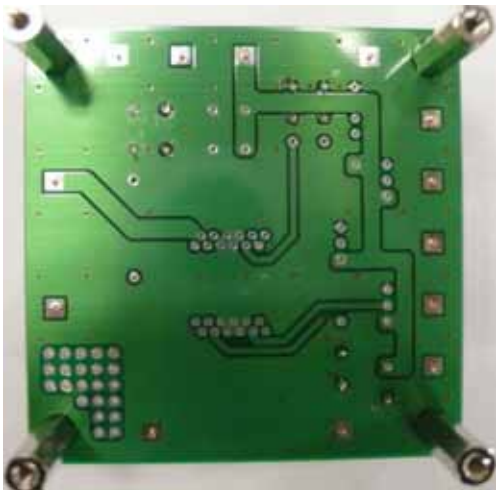


Conditions: Ta = 25°C VM = 24 V IN2, PWM, V_{RFE} = 5 V RSGND = GND TISD; 20 k Ω, OSC = GND IN1 = −100 μA (Diode voltage monitor circuit), on a PCB

Used PCB: Glass epoxy board 70 × 70 × 1.6 (mm), a double-sided PCB, Cu 67%, Cu thickness 50 μm



Top View



Bottom View

The test curves shown above are only typical ones. They fluctuate depending on power supply voltages, temperatures and IC variation.

Also, the conditions such as board mount method and running motors affect the results; therefore the TB6641FG must be used after a sufficient evaluation and provided with a safety margin before used.

Care must be taken for the junction temperature to be kept less than 150°C.

7. Pin Shorting

The results of evaluations performed by Toshiba are listed below.

The TB6641FG has never been destroyed even when the following pairs of the pins are shorted together. However, amount of the current flow upon short depends on how the TISD pin is controlled.

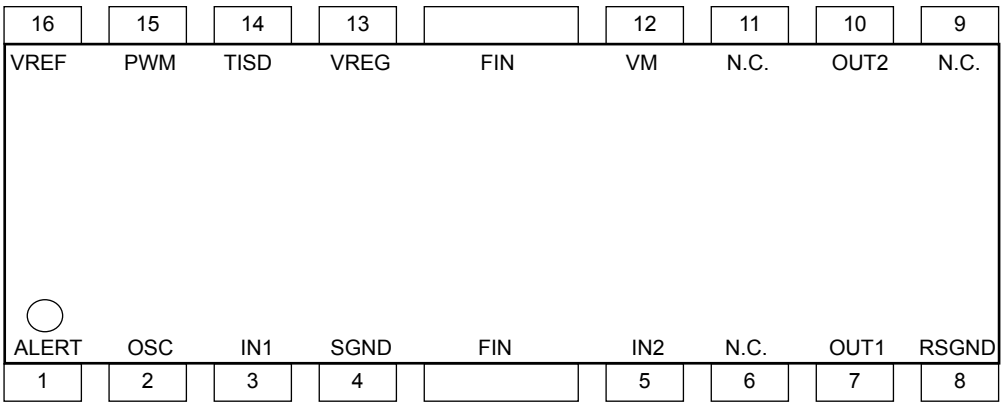
Also, power supply impedance and shorted wiring impedance affects amount of the current flow on short.

Furthermore, whether or not the TB6641FG is destroyed depends on the power supply voltage, temperature and the IC variation. Therefore, a sufficient evaluation of the TB6641FG in your application and providing a safety margin are required.

For example, if the TISD pin is connected to GND under the following conditions not to make the TB6641FG activate the ISD circuit, the output current continues flowing and finally would destroy the TB6641FG. Therefore, care must be taken not to break the TB6641FG.

Adjacent Shorted Pin Numbers	Adjacent Shorted Pin Names	Condition of TB6641FG	Adjacent Shorted Pin Numbers	Adjacent Shorted Pin Names	Condition of TB6641FG
1 – 2	ALERT – OSC	Not destroyed	9 – 10	N.C – OUT2	Not destroyed
2 – 3	OSC – IN1	Not destroyed	10 – 11	OUT2 – N.C	Not destroyed
3 – 4	IN1 – SGND	Not destroyed	11 – 12	N.C – VM	Not destroyed
4 – FIN	SGND – FIN(GND)	Not destroyed	12 – FIN	VM – FIN(GND)	Not destroyed
FIN – 5	FIN(GND) – IN2	Not destroyed	FIN – 13	FIN(GND) – VREG	Not destroyed
5 – 6	IN2 – N.C	Not destroyed	13 – 14	VREG – TISD	Not destroyed
6 – 7	N.C – OUT1	Not destroyed	14 – 15	TISD – PWM	Not destroyed
7 – 8	OUT1 – RSGND	Not destroyed	15 – 16	PWM – VREF	Not destroyed

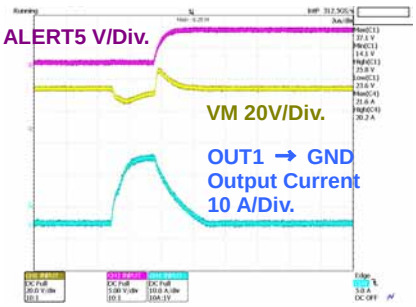
Conditions: VM = 24 V, Ta = 25°C, RSGND = GND, TISD = 20 kΩ
Between VM and GND: Electrolytic capacitor of 10 μF + ceramic capacitor of 0.1 μF



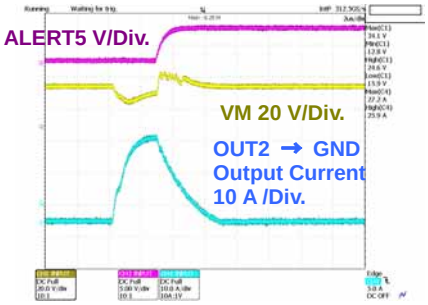
Shorting Condition	Shorted Pin Names	Condition of TB6641FG
OUT1 to GND	OUT1 – GND	Not destroyed
OUT1 to Supply	OUT1 – VM	Not destroyed
OUT2 to GND	OUT2 – GND	Not destroyed
OUT2 to Supply	OUT2 – VM	Not destroyed
Load Short 1	OUT1: High – OUT2: Low	Not destroyed
Load Short 2	OUT1: Low – OUT2: High	Not destroyed

Conditions: VM = 24 V, Ta = 25°C, RSGND = GND, ALERT, TISD = 20 kΩ
Between VM and GND: Electrolytic capacitor of 10 μF + ceramic capacitor of 0.1 μF

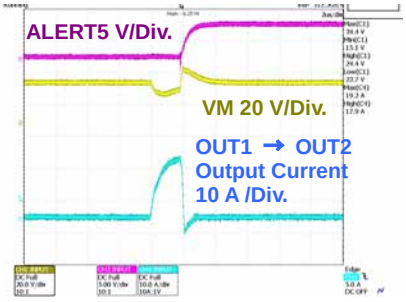
OUT1 Shorted to Ground
Waveforms, OUT1-GND



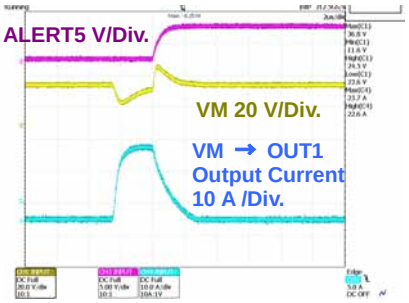
OUT2 Shorted to Ground
Waveforms, OUT2-GND



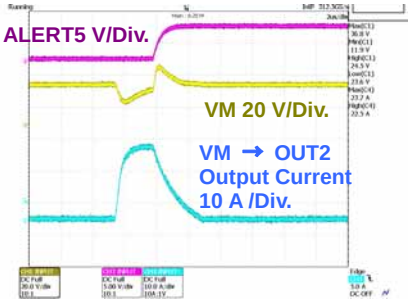
Load Short 1 Waveforms,
OUT1: High-OUT2: Low



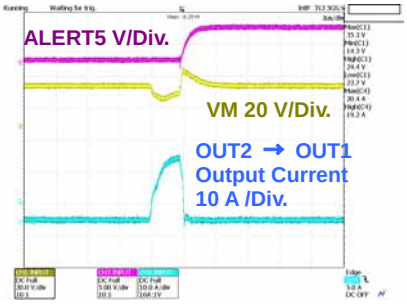
OUT1 Shorted to Supply
Waveforms, OUT1-VM



OUT2 Shorted to Supply
Waveforms, OUT2-VM



Load Short 2 Waveforms,
OUT1: Low-OUT2: High



ISD behavior on load shorts

Irrespective of whether or not to use the constant current PWM control (i.e. a detection resistor is connected between the RSGND and SGND pins), if wiring impedance occurs between the RSGND and SGND pins, care should be taken because it invokes the constant current PWM control before the ISD circuit running; the ISD circuit cannot be activated on a load short.

Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.
Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.

5. Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on Handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

(3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

(4) Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

Points to Remember on Handling of ICs

(1) Over current Protection Circuit
Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Over current protection circuits operate against the over current, clear the over current status immediately.
Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

(2) Thermal Shutdown Circuit
Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately. Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

(3) Heat Radiation Design
In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (TJ) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(4) Back-EMF
When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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