

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC74VHC273F, TC74VHC273FK

## Octal D-Type Flip-Flop with Clear

The TC74VHC273 is an advanced high speed CMOS OCTAL D-TYPE FLIP FLOP fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

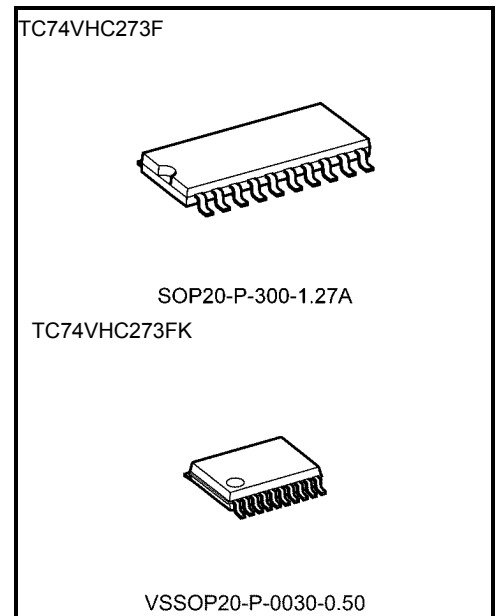
Information signals applied to D inputs are transferred to the Q outputs on the positive going edge of the clock pulse.

When the  $\overline{\text{CLR}}$  input is held "L", the Q outputs are at a low logic level independent of the other inputs.

An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

## Features

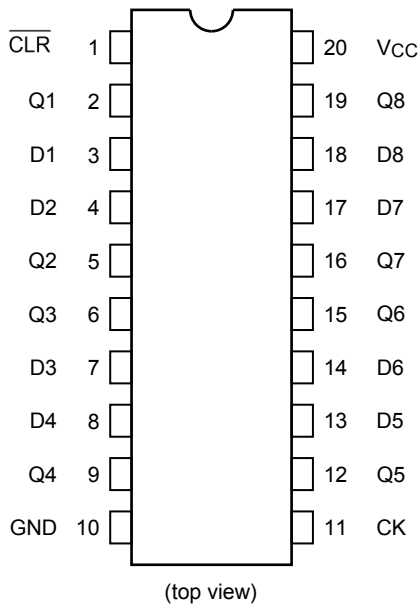
- High speed:  $f_{\text{max}} = 165 \text{ MHz}$  (typ.) at  $V_{\text{CC}} = 5 \text{ V}$
- Low power dissipation:  $I_{\text{CC}} = 4 \mu\text{A}$  (max) at  $T_a = 25^\circ\text{C}$
- High noise immunity:  $V_{\text{NIH}} = V_{\text{NIL}} = 28\% V_{\text{CC}}$  (min)
- Power down protection is provided on all inputs.
- Balanced propagation delays:  $t_{\text{pLH}} \approx t_{\text{pHL}}$
- Wide operating voltage range:  $V_{\text{CC}}(\text{opr}) = 2 \text{ to } 5.5 \text{ V}$
- Low noise:  $V_{\text{OLP}} = 0.8 \text{ V}$  (max)
- Pin and function compatible with 74ALS273



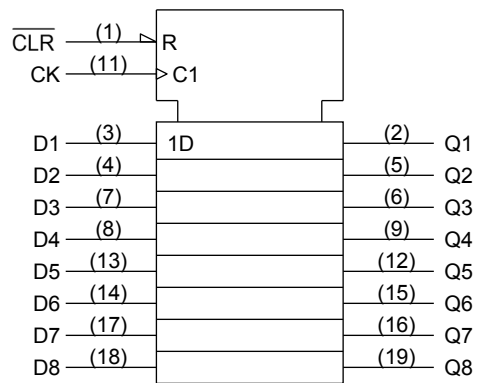
Weight	
SOP20-P-300-1.27A	: 0.22 g (typ.)
VSSOP20-P-0030-0.50	: 0.03 g (typ.)

Start of commercial production  
1991-05

### Pin Assignment



### IEC Logic Symbol

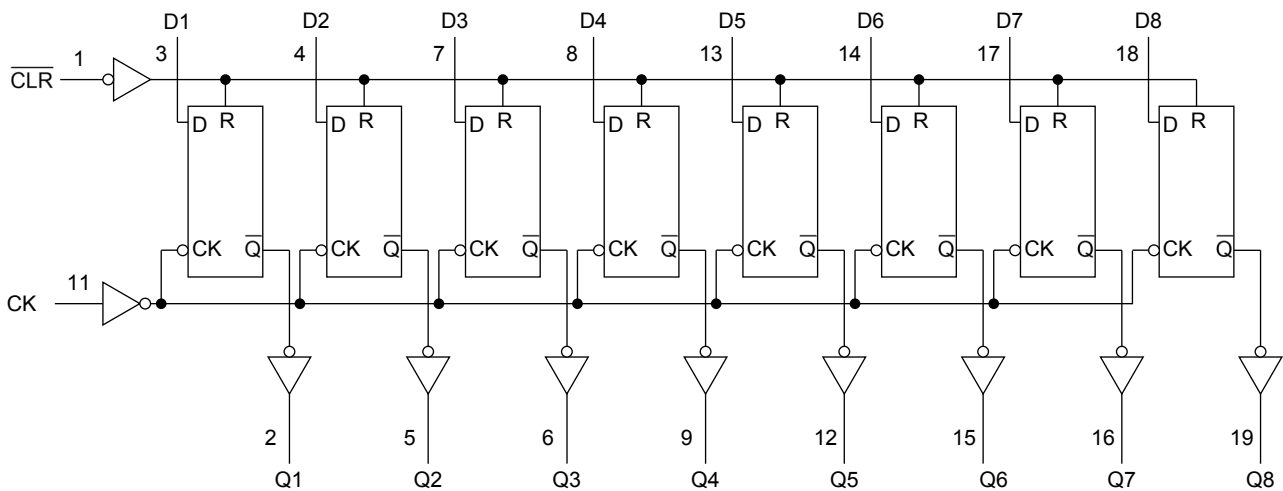


### Truth Table

Inputs			Output	Function
$\overline{\text{CLR}}$	D	CK	Q	
L	X	X	L	Clear
H	L	$\uparrow$	L	—
H	H	$\uparrow$	H	—
H	X	$\downarrow$	$Q_n$	No Change

X: Don't care

### System Diagram



### Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V <sub>CC</sub>	-0.5 to 7.0	V
DC input voltage	V <sub>IN</sub>	-0.5 to 7.0	V
DC output voltage	V <sub>OUT</sub>	-0.5 to V <sub>CC</sub> + 0.5	V
Input diode current	I <sub>IK</sub>	-20	mA
Output diode current	I <sub>OK</sub>	±20	mA
DC output current	I <sub>OUT</sub>	±25	mA
DC V <sub>CC</sub> /ground current	I <sub>CC</sub>	±75	mA
Power dissipation	P <sub>D</sub>	180	mW
Storage temperature	T <sub>stg</sub>	-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.  
 Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.  
 Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

### Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V <sub>CC</sub>	2.0 to 5.5	V
Input voltage	V <sub>IN</sub>	0 to 5.5	V
Output voltage	V <sub>OUT</sub>	0 to V <sub>CC</sub>	V
Operating temperature	T <sub>opr</sub>	-40 to 85	°C
Input rise and fall time	dt/dv	0 to 100 (V <sub>CC</sub> = 3.3 ± 0.3 V) 0 to 20 (V <sub>CC</sub> = 5 ± 0.5 V)	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.  
 Unused inputs must be tied to either V<sub>CC</sub> or GND.

## Electrical Characteristics

### DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit	
				V <sub>CC</sub> (V)	Min	Typ.	Max	Min		Max
High-level input voltage	V <sub>IH</sub>	—		2.0 3.0 to 5.5	1.50 V <sub>CC</sub> × 0.7	— —	— —	1.50 V <sub>CC</sub> × 0.7	— —	V
Low-level input voltage	V <sub>IL</sub>	—		2.0 3.0 to 5.5	— —	— —	0.50 V <sub>CC</sub> × 0.3	— —	0.50 V <sub>CC</sub> × 0.3	V
High-level output voltage	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50 μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	— — —	1.9 2.9 4.4	— — —	V
			I <sub>OH</sub> = -4 mA	3.0	2.58	—	—	2.48	—	
			I <sub>OH</sub> = -8 mA	4.5	3.94	—	—	3.80	—	
Low-level output voltage	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50 μA	2.0 3.0 4.5	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
			I <sub>OL</sub> = 4 mA	3.0	—	—	0.36	—	0.44	
			I <sub>OL</sub> = 8 mA	4.5	—	—	0.36	—	0.44	
Input leakage current	I <sub>IN</sub>	V <sub>IN</sub> = 5.5 V or GND		0 to 5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		5.5	—	—	4.0	—	40.0	μA

### Timing Requirements (input: tr = tf = 3 ns)

Characteristics	Symbol	Test Condition		Ta = 25°C		Ta = -40 to 85°C	Unit	
				V <sub>CC</sub> (V)	Typ.	Limit		Limit
Minimum pulse width (CK)	t <sub>w</sub> (L)	—		3.3 ± 0.3	—	5.5	6.5	ns
	t <sub>w</sub> (H)	—		5.0 ± 0.5	—	5.0	5.0	
Minimum pulse width ( $\overline{\text{CLR}}$ )	t <sub>w</sub> (L)	—		3.3 ± 0.3 5.0 ± 0.5	— —	5.0 5.0	6.0 5.0	ns
Minimum set-up time	t <sub>s</sub>	—		3.3 ± 0.3	—	5.5	6.5	ns
		—		5.0 ± 0.5	—	4.5	4.5	
Minimum hold time	t <sub>h</sub>	—		3.3 ± 0.3	—	1.0	1.0	ns
		—		5.0 ± 0.5	—	1.0	1.0	
Minimum removal time ( $\overline{\text{CLR}}$ )	t <sub>rem</sub>	—		3.3 ± 0.3	—	2.5	2.5	ns
		—		5.0 ± 0.5	—	2.0	2.0	

### AC Characteristics (input: $t_r = t_f = 3 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C		Unit			
			VCC (V)	CL (pF)	Min	Typ.	Max		Min	Max	
Propagation delay time (CK-Q)	t <sub>pLH</sub> t <sub>pHL</sub>	—	3.3 ± 0.3	15	—	8.7	13.6	1.0	16.0	ns	
				50	—	11.2	17.1	1.0	19.5		
			5.0 ± 0.5	15	—	5.8	9.0	1.0	10.5		ns
				50	—	7.3	11.0	1.0	12.5		
Propagation delay time (CLR-Q)	t <sub>pHL</sub>	—	3.3 ± 0.3	15	—	8.9	13.6	1.0	16.0	ns	
				50	—	11.4	17.1	1.0	19.5		
			5.0 ± 0.5	15	—	5.2	8.5	1.0	10.0		ns
				50	—	6.7	10.5	1.0	12.0		
Maximum clock frequency	f <sub>max</sub>	—	3.3 ± 0.3	15	75	120	—	65	—	MHz	
				50	50	75	—	45	—		
			5.0 ± 0.5	15	120	165	—	100	—		MHz
				50	80	110	—	70	—		
Output to output skew	t <sub>osLH</sub> t <sub>osHL</sub>	(Note 1)	3.3 ± 0.3	50	—	—	1.5	—	1.5	ns	
			5.0 ± 0.5	50	—	—	1.0	—	1.0		
Input capacitance	C <sub>IN</sub>	—	—	—	4	10	—	10	pF		
Power dissipation capacitance	CPD	(Note 2)	—	—	31	—	—	—	pF		

Note 1: Parameter guaranteed by design.

$$t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|$$

Note 2: CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr}) = CPD \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$$

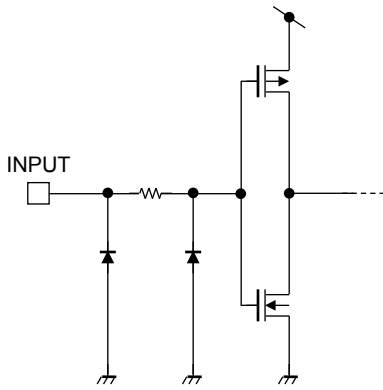
And the total CPD when n pcs. of flip flop operate can be gained by the following equation:

$$CPD(\text{total}) = 22 + 9 \cdot n$$

### Noise Characteristics (input: $t_r = t_f = 3 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Ta = 25°C			Unit
			VCC (V)	Typ.	Max	
Quiet output maximum dynamic V <sub>OL</sub>	V <sub>OLP</sub>	C <sub>L</sub> = 50 pF	5.0	0.5	0.8	V
Quiet output minimum dynamic V <sub>OL</sub>	V <sub>OLV</sub>	C <sub>L</sub> = 50 pF	5.0	-0.5	-0.8	V
Minimum high level dynamic input voltage	V <sub>IHD</sub>	C <sub>L</sub> = 50 pF	5.0	—	3.5	V
Maximum low level dynamic input voltage	V <sub>ILD</sub>	C <sub>L</sub> = 50 pF	5.0	—	1.5	V

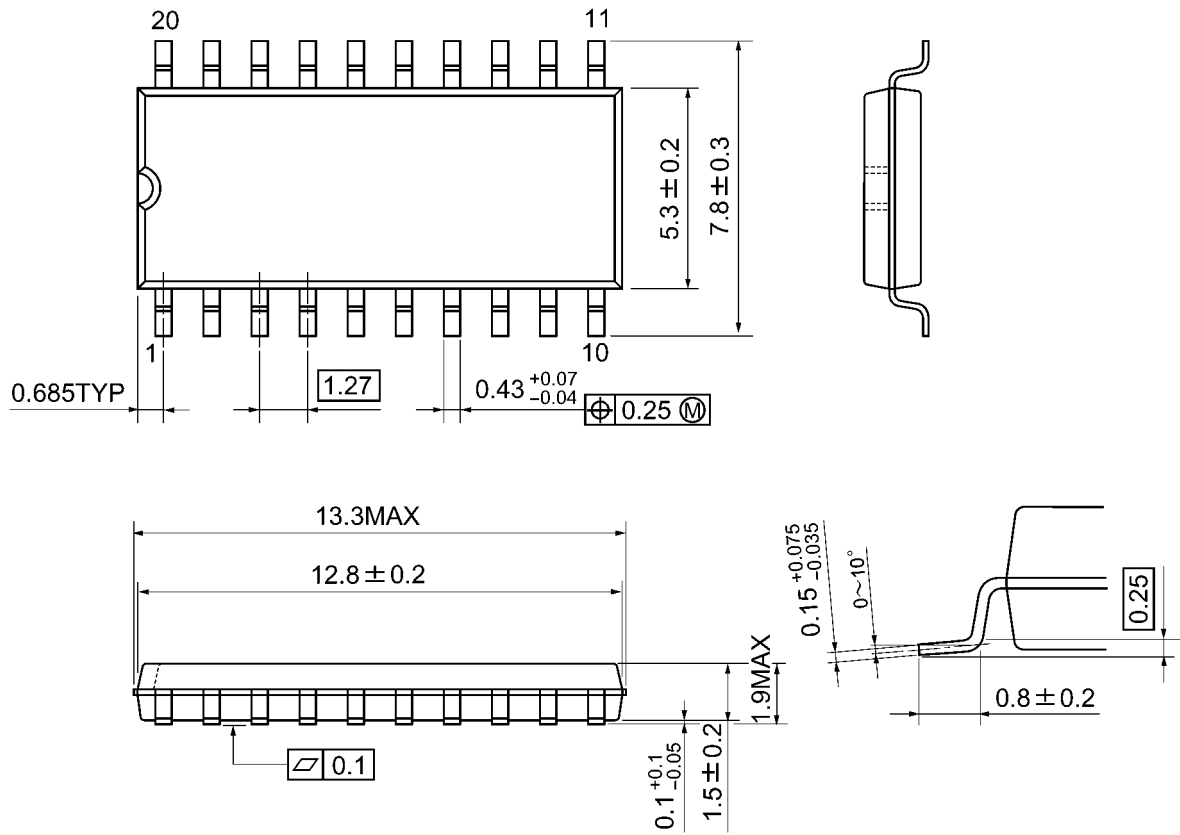
### Input Equivalent Circuit



### Package Dimensions

SOP20-P-300-1.27A

Unit: mm

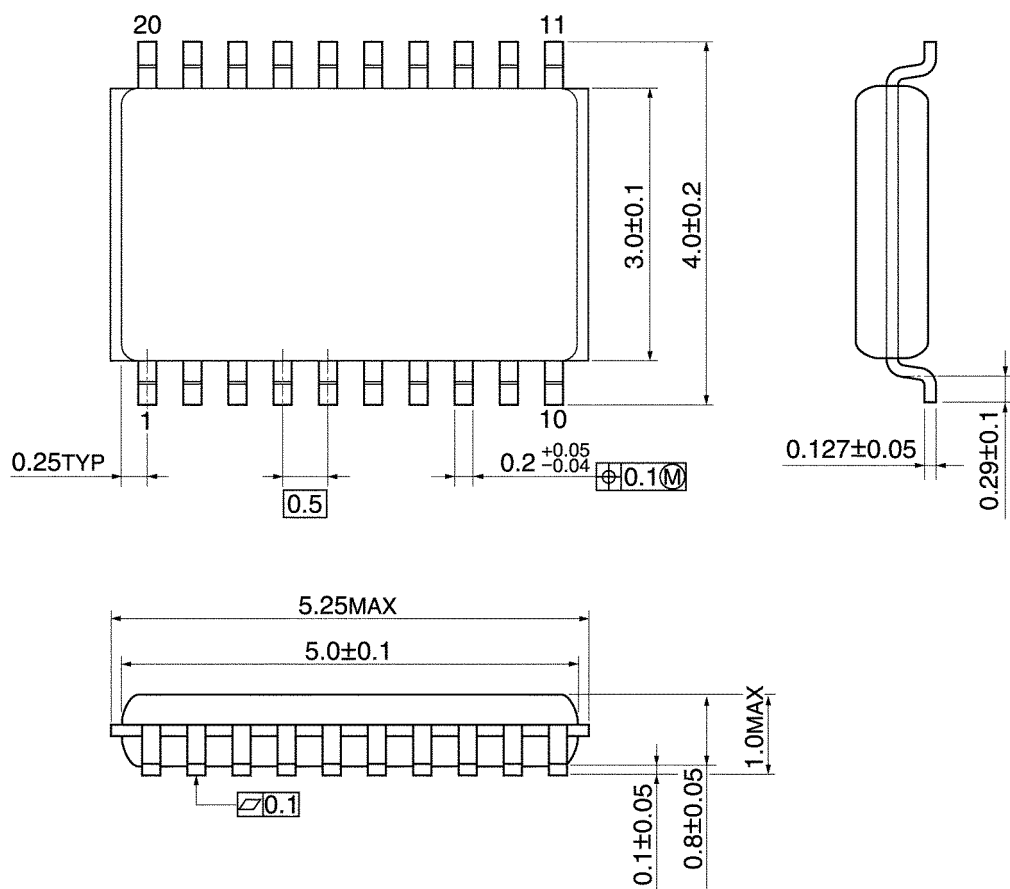


Weight: 0.22 g (typ.)

### Package Dimensions

VSSOP20-P-0030-0.50

Unit: mm



Weight: 0.03 g (typ.)

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