MOSFETs Silicon P-Channel MOS (U-MOSⅥ)

TJ15P04M3

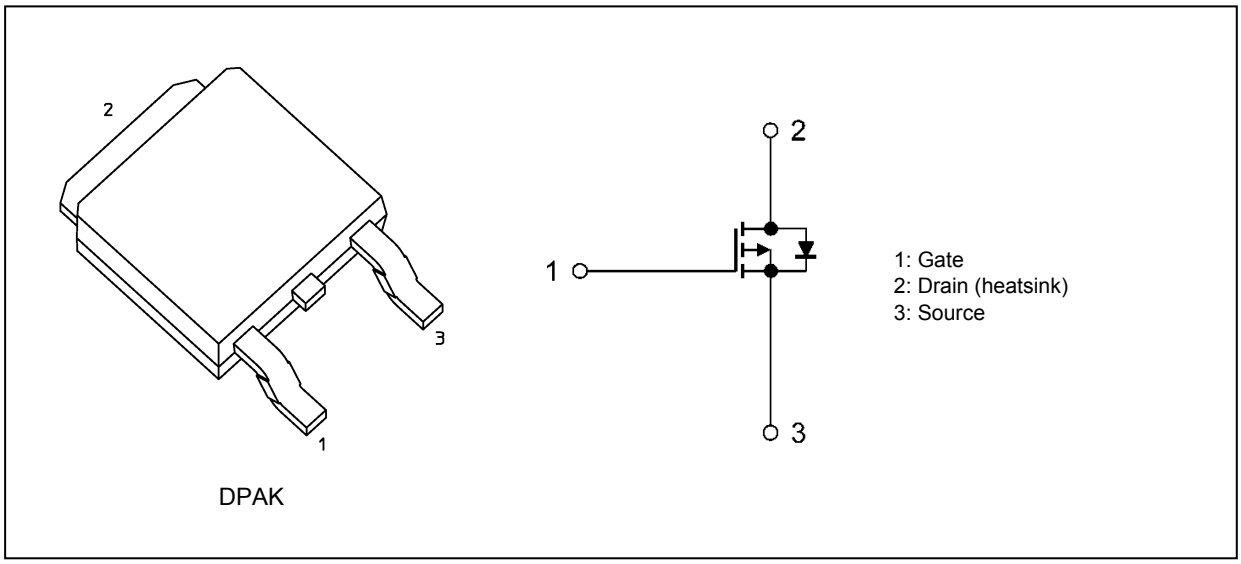
1. Applications

- Motor Drivers
- Power Management Switches

2. Features

(1) Low drain-source on-resistance: $R_{DS(ON)}$ = 28 mΩ (typ.) (V_{GS} = -10 V)
(2) Low leakage current: I_{DSS} = -10 μA (max) (V_{DS} = -40 V)
(3) Enhancement mode: V_{th} = -0.8 to -2.0 V (V_{DS} = -10 V, I_D = -0.1 mA)

3. Packaging and Internal Circuit



DPAK

4. Absolute Maximum Ratings (Note) (T_a = 25°C unless otherwise specified)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	-40	V
Gate-source voltage		V_{GSS}	±20	
Drain current (DC)	(Note 1)	I_D	-15	A
Drain current (pulsed)	(Note 1)	I_{DP}	-45	
Power dissipation	(T_c = 25°C)	P_D	29	W
Single-pulse avalanche energy	(Note 2)	E_{AS}	29	mJ
Single-pulse avalanche current		I_{AS}	-15	A
Channel temperature		T_{ch}	150	°C
Storage temperature		T_{stg}	-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Start of commercial production
2010-01

5. Thermal Characteristics

Characteristics	Symbol	Max	Unit
Channel-to-case thermal resistance	$R_{th(ch-c)}$	4.3	°C/W
Channel-to-ambient thermal resistance	$R_{th(ch-a)}$	125	

Note 1: Ensure that the channel temperature does not exceed 150°C.
Note 2: V_{DD} = -32 V, T_{ch} = 25°C (initial), L = 100 μH, R_G = 25 Ω, I_{AS} = -15 A

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

6. Electrical Characteristics

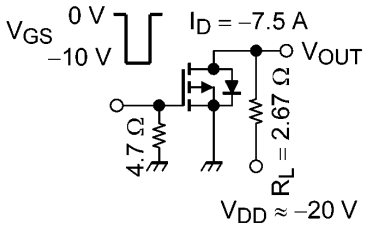
6.1. Static Characteristics (T_a = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V	—	—	±0.1	μA
Drain cut-off current	I_{DSS}	V_{DS} = -40 V, V_{GS} = 0 V	—	—	-10	
Drain-source breakdown voltage	$V_{(BR)DSS}$	I_D = -10 mA, V_{GS} = 0 V	-40	—	—	V
Drain-source breakdown voltage (Note 3)	$V_{(BR)DSX}$	I_D = -10 mA, V_{GS} = 10 V	-30	—	—	
Gate threshold voltage	V_{th}	V_{DS} = -10 V, I_D = -0.1 mA	-0.8	—	-2.0	
Drain-source on-resistance	$R_{DS(ON)}$	V_{GS} = -4.5 V, I_D = -7.5 A	—	37	48	mΩ
		V_{GS} = -10 V, I_D = -7.5 A	—	28	36	

Note 3: If a reverse bias is applied between gate and source, this device enters $V_{(BR)DSX}$ mode. Note that the drain-source breakdown voltage is lowered in this mode.

6.2. Dynamic Characteristics (T_a = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	C_{iss}	V_{DS} = -10 V, V_{GS} = 0 V, f = 1 MHz	—	1100	—	pF
Reverse transfer capacitance	C_{rss}		—	130	—	
Output capacitance	C_{oss}		—	170	—	
Switching time (rise time)	t_r	See Figure 6.2.1.	—	11	—	ns
Switching time (turn-on time)	t_{on}		—	19	—	
Switching time (fall time)	t_f		—	42	—	
Switching time (turn-off time)	t_{off}		—	170	—	



Duty ≤ 1%, t_w = 10 μs

Fig. 6.2.1 Switching Time Test Circuit

6.3. Gate Charge Characteristics (T_a = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Q_g	V_{DD} ≈ -32 V, V_{GS} = -10 V, I_D = -15 A	—	26	—	nC
Gate-source charge 1	Q_{gs1}		—	6.7	—	
Gate-drain charge	Q_{gd}		—	2.5	—	

6.4. Source-Drain Characteristics (T_a = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Reverse drain current (pulsed) (Note 4)	I_{DRP}	—	—	—	-45	A
Diode forward voltage	V_{DSF}	I_{DR} = -15 A, V_{GS} = 0 V	—	—	1.2	V

Note 4: Ensure that the channel temperature does not exceed 150°C.

7. Marking

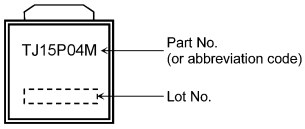


Fig. 7.1 Marking

8. Characteristics Curves (Note)

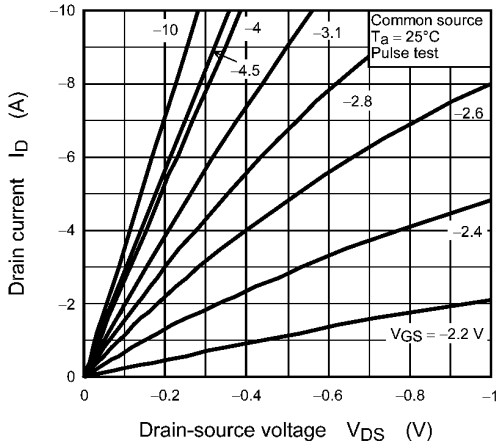


Fig. 8.1 I_D - V_{DS}

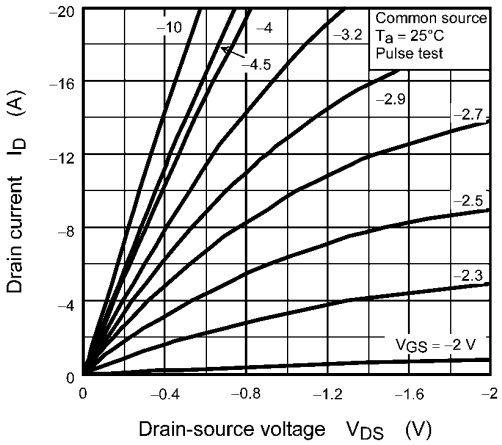


Fig. 8.2 I_D - V_{DS}

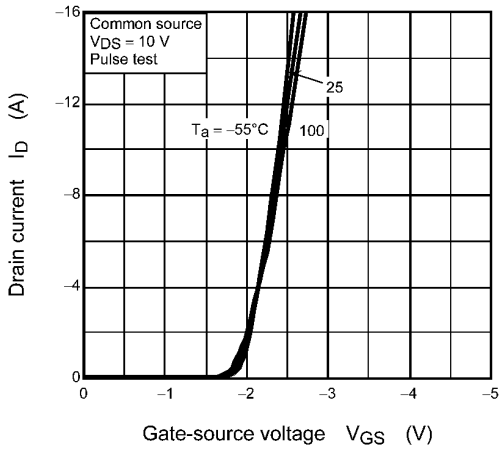


Fig. 8.3 I_D - V_{GS}

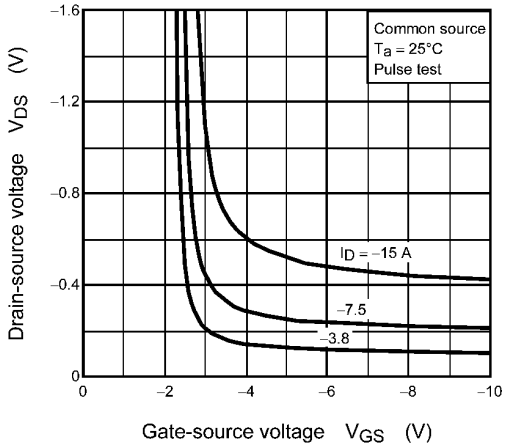


Fig. 8.4 V_{DS} - V_{GS}

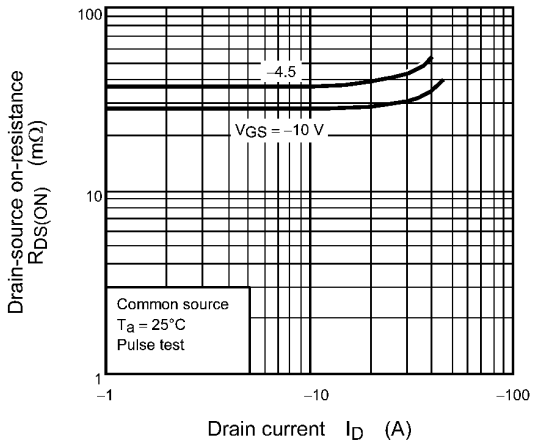


Fig. 8.5 $R_{DS(ON)}$ - I_D

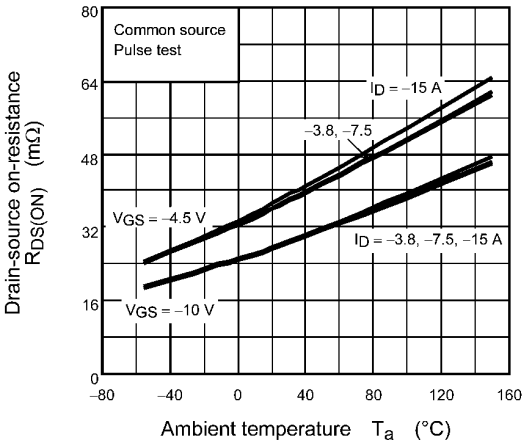


Fig. 8.6 $R_{DS(ON)}$ - T_a

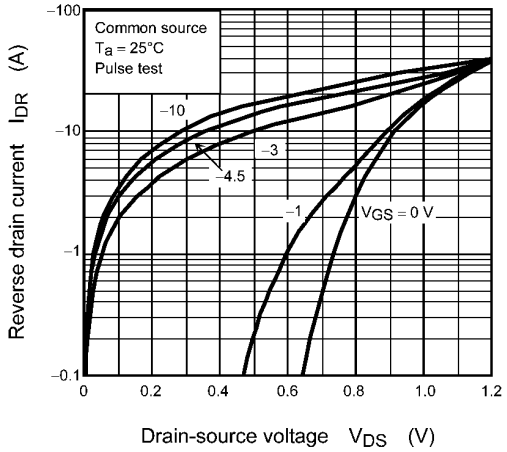


Fig. 8.7 I_{DR} - V_{DS}

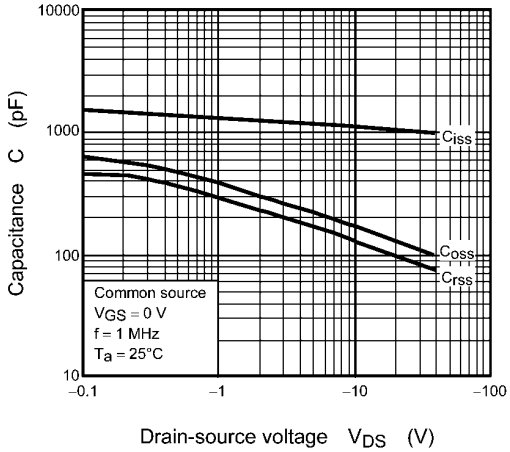


Fig. 8.8 Capacitance - V_{DS}

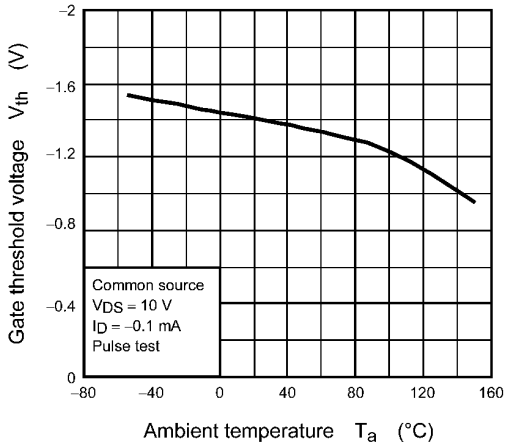


Fig. 8.9 V_{th} - T_a

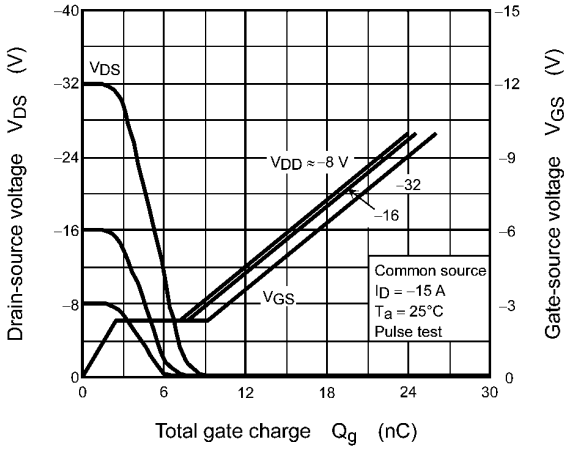


Fig. 8.10 Dynamic Input/Output Characteristics

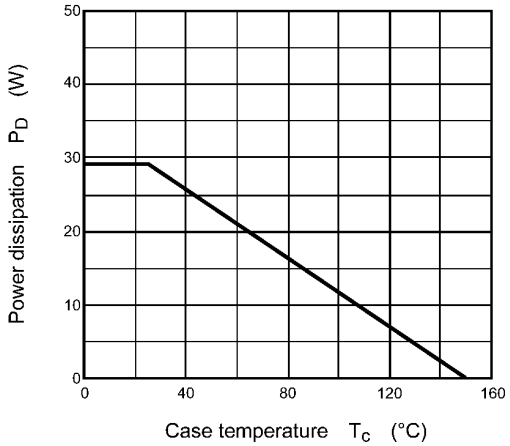


Fig. 8.11 P_D - T_c
(Guaranteed Maximum)

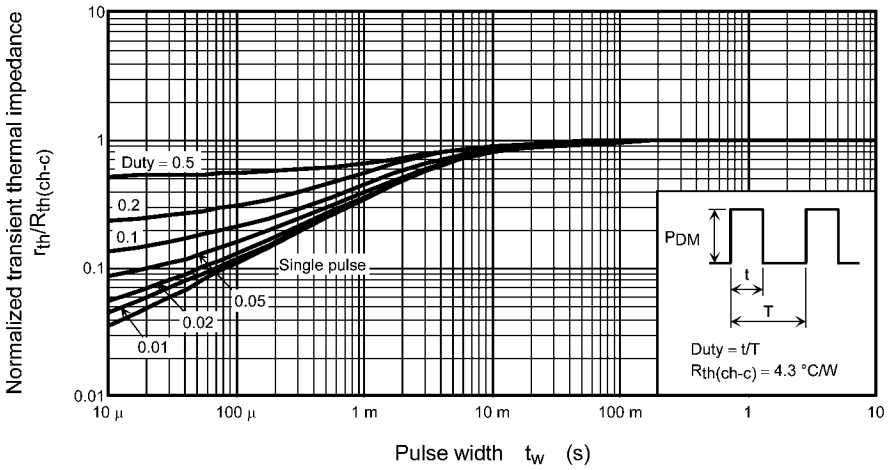


Fig. 8.12 $r_{th}/R_{th(ch-c)}$ - t_w (Guaranteed Maximum)

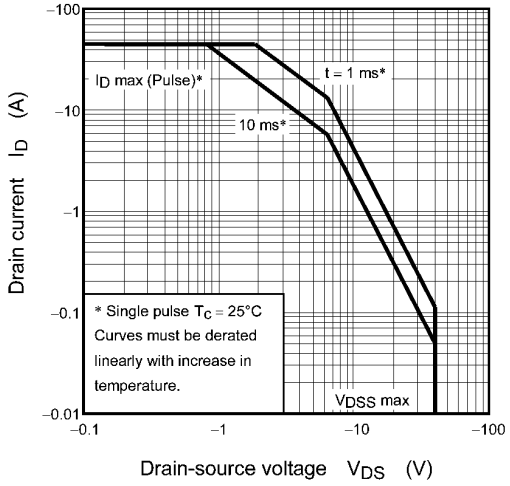


Fig. 8.13 Safe Operating Area (Guaranteed Maximum)

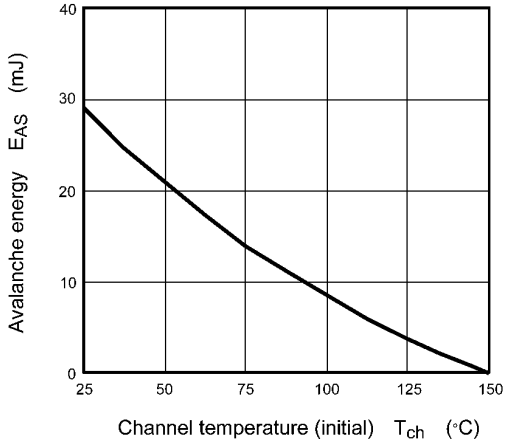
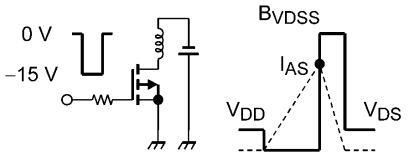


Fig. 8.14 E_{AS} - T_{ch} (Guaranteed Maximum)



$R_G = 25\ \Omega$
$V_{DD} = -32$ V, L = 100 μH

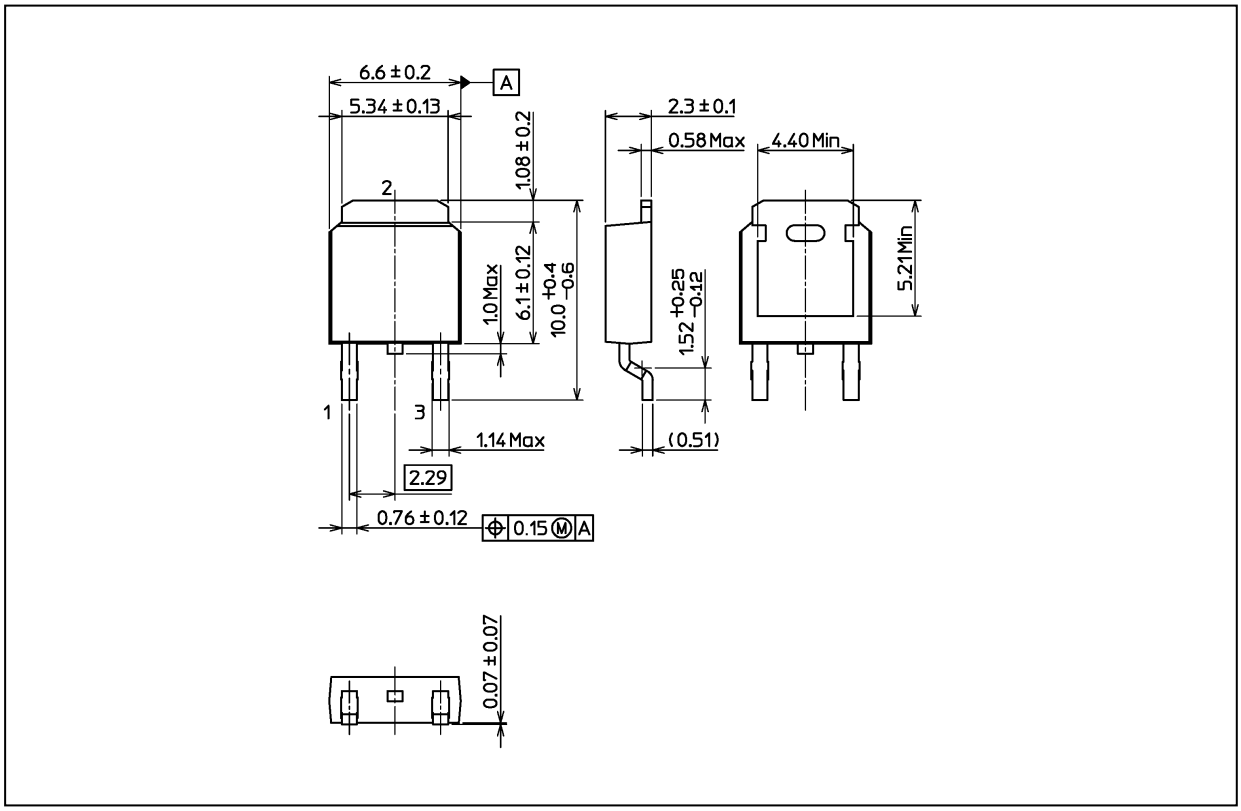
$$E_{AS} = \frac{1}{2} \cdot L \cdot I_{AS}^2 \cdot \left[\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right]$$

Fig. 8.15 Test Circuit/Waveform

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Package Dimensions

Unit: mm



Weight: 0.36 g (typ.)

Package Name(s)
TOSHIBA: 2-7K1S
Nickname: DPAK

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