Application Processor Lite *ApP Lite*

TZ1000 Series

Reference Manual

MCU Overview

Revision 1.3

2018-01

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

Table of Contents

List of Figures

List of Tables

Preface

This document provides the specification for the MCU Overview designed for the TZ1000 Series.

Intended Audience

This document is intended for the following users.

Driver software developers.

System designers

Conventions in this document

- The numerical values are expressed as follows.
  Hexadecimal number**:** 0xABC
  Decimal number**:** 123 or 0d123 - Only when it needs to be explicitly shown that they are decimal numbers.
  Binary number**:** 0b111 - It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [3**:**0].
  [3**:**0] shows four signal names 3, 2, 1, and 0 together.
- The characters surrounded by [] defines the register.
  Example**:** ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example**:** ***[XYZ1]***, ***[XYZ2]***, and ***[XYZ3]*** to ***[XYZn]***
- The bit range of a register is written like as [3**:**0].
  Example**:** Bit[3**:**0] expresses the range of bits 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example**:** ***[ABCD]***.EFG = 0x01 (hexadecimal), ***[XYZn]***.VW = 1 (binary)
- Word and Byte represent the following bit length.
  Byte**:** 8-bit
  Half word**:** 16-bit
  Word**:** 32-bit
  Double word**:** 64-bit
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, don't use the read value.
- Properties of each bit in a register are expressed as follows.
  R**:** Read only
  W**:** Write only
  W1C**:** Write 1 Clear - The corresponding bit is cleared (=0) when "1" is written to this bit.
  W1S**:** Write 1 Set - The corresponding bit is set (=1) when "1" is written to this bit.
  R/W**:** Read and Write are possible.
  R/W0C**:** Read/Write 0 Clear
  R/W1C**:** Read/Write 1 Clear
  R/W1S**:** Read/Write 1 Set
  RS/WC**:** Read Set/Write Clear - Set after read operation, cleared after write operation.
- The value read from the bit having default value of "—" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value. In the cases that default is "—," follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value. In the cases that default is "—," follow the definition of each register.

1. Summary

The MCU is a family of microcontrollers which adopts a high performance 32-bit Arm® Cortex®-M4 with FPU processor.

The MCU incorporates 288 KB SRAM, and all functions which are necessary to compose a one-chip wearable device.

The MCU supports a variety of peripheral interfaces such as the USB Device mode, UART, SPI, and I²C. These interfaces allow the MCU to easily connected to the MEMS sensors with digital interfaces, such as atmospheric pressure sensors and moisture sensors. The MCU also incorporates a 12-bit ADC and a 24-bit ΔΣADC. Without any special analog front-end devices, this 24-bit ΔΣADC allows the MCU to be directly connected to a photo diode for pulse sensing, a photoelectric sensor and a wide variety of sensors, such as a gas sensor. This contributes to reducing the total system cost.

1.1. Features

- CPU Core
  - Arm Cortex-M4 with FPU processor running at up to 48 MHz
  - Floating Point Unit (FPU)
  - Memory Protection Unit (MPU)
  - Arm® Thumb®-2 instruction set
- Memories
  - 288 KB embedded SRAM
- System Functions
  - Embedded linear and switching voltage regulator for single power supply operation
  - Brown-out Detectors
  - Crystal oscillators**:** 12 MHz for CPU and USB, 32.768 kHz for RTC
  - High precision 4 MHz factory trimmed internal RC oscillator
  - Low power 32 kHz internal RC oscillator
- Peripherals
  - USB 2.0 Device**:** 12 Mbps, 1 port 4 bidirectional endpoints
  - Two Master/Slave I²C interface up to 400 kbps
  - Two UART
  - Two SPI Master with chip selects signals
  - One 4-channel ADC with 12 bits resolution
  - One 3-channel Delta-Sigma ADC with 24 bits resolution
  - Advanced Encryption System (AES) Engine with 128/192/256-bit key length
  - True random number generator
  - 24 general purpose IOs (GPIO)
  - Real-time clock which supports calender mode
  - Watchdog timer
  - Four 16-bit Advanced Timer/Counter channels with capture, compare and PWM mode
  - Two 32-bit Timer/Counter channels
  - One 8 channels DMA controller
- Single Power Supply
  - Voltage range**:** 2.1 to 3.6 V or 1.71 to 1.89 V.

2. Description

The MCU adopts a high performance 32-bit Arm Cortex-M4 with FPU processor. The Cortex-M4 with FPU processor consists of a floating point processor unit, a memory protection unit, and a flexible interrupt controller. It supports many kinds of real time OS.

The MCU can select the most suitable power supply voltage and circuit to its operating frequency. Users can achieve lower power consumption in their applications to use the power saving mode.

The MCU includes a low power and as large capacity as 288 KB of SRAM which is used to store program codes and data. The MCU can realize an activity meter and other devices without any other components.

An ASE engine and a random number generator are incorporated for a security function. The AES complies with FIPS (Federal Information Processing Standard) Publication 197, Advanced Encryption Standard. It can select a key length among 128 bits, 192 bits, and 256 bits, and executes the encryption and decryption without any processes of the processor.

The random number generator has passed the random number test of NIST SP800-22 (National Institute of Standards and Technology Special Publication 800-22), and it can be used for the bases of keys and others.

The 8 channel DMA controllers perform the data transfer between the SRAM and the peripheral such as the UART or between the SRAMs without any processes of the processor. The data transfer engine (SRAMC) in the SRAM controller enables the data transfer between the SRAMs without passing the data buses.

The MCU also incorporates a 12-bit ADC and a 24-bit ΔΣADC. Without any special analog front-end devices, this 24-bit ΔΣADC allows the MCU to be directly connected to a photo diode for pulse sensing, photoelectric sensors with small output voltage like for ECG measure application and a wide variety of sensors, such as a gas sensor. This contributes to reducing the total system cost.

3. Features

3.1. Block Diagram

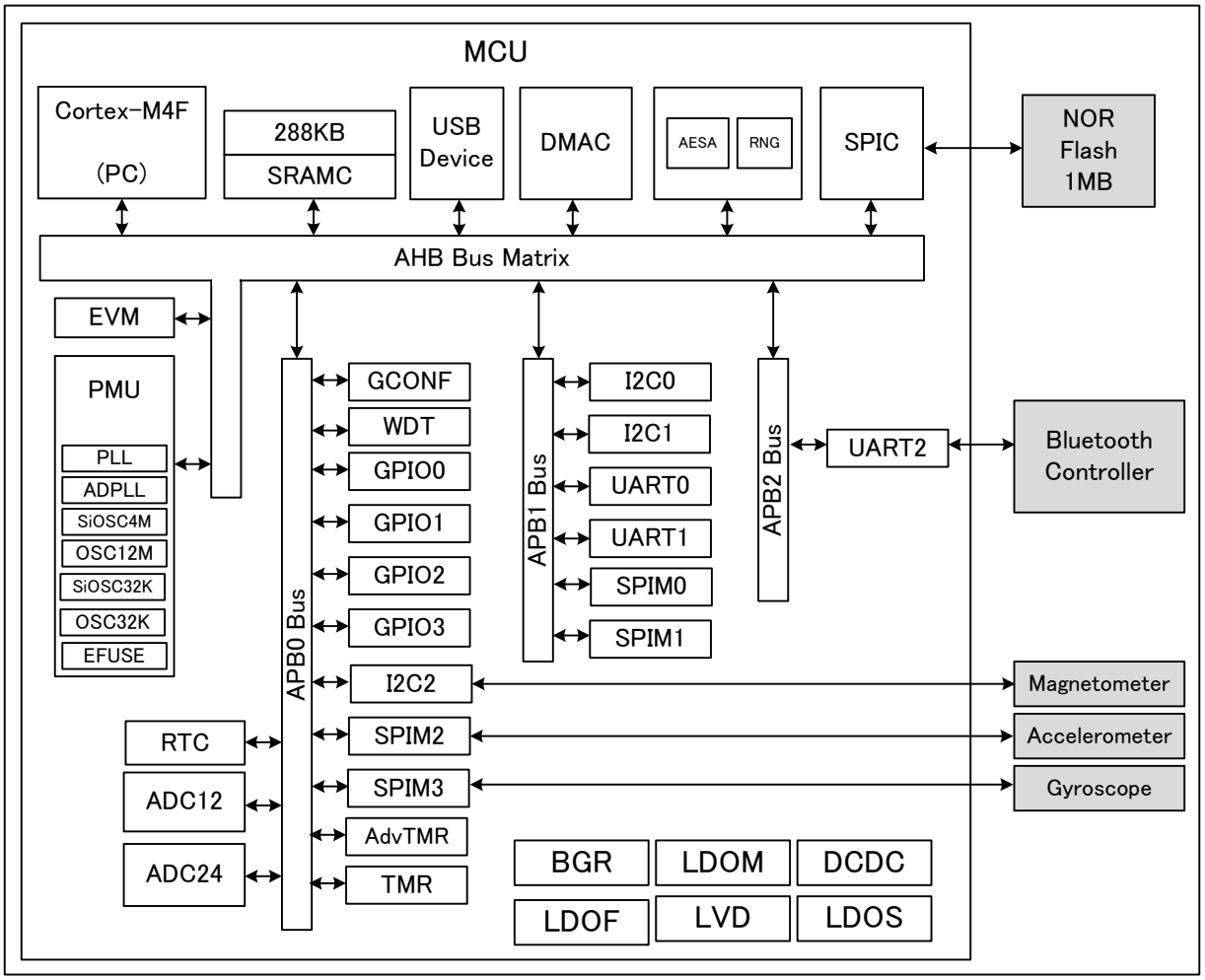


Figure 3.1 Block Diagram

3.2. MCU Summary

3.2.1. CPU Core

Arm Cortex-M4 with FPU processor
Instruction set Architecture: Armv7E-M architecture
Single Precision floating point unit with IEEE 754 compliant
Supports SIMD and MAC DSP extension instructions
Tumb2 instruction set
Memory protection unit
Integrated bit manipulation instructions & bit banding
Operating Frequency: selectable from 32 kHz to 48 MHz
Debug function: Arm® CoreSight™ component
V7 debug architecture with JTAG debug port

3.2.2. Memories

SRAM
Memory size: 288 KB

3.2.3. System

Embedded voltage linear and switching regulator (1.2 V/1.1 V/1.0 V/0.9 V)
Embedded LDO (1.7 V)
High precision 4 MHz internal Silicon oscillator
Low power 32 kHz internal Silicon oscillator
Analog PLL up to 48 MHz for whole system and USB with reference clock 12 MHz
Digital PLL up to 48 MHz with reference clock 32 kHz

AES Accelerator (AESA)
AES accelerator engine with 128, 192, 256-bit key length
Compliant with FIPS 197 (Advanced Encryption Standard)
Encryption/Decryption with dedicated DMA engine
Supported 3 block cipher modes of operation (ECB, CBC, CTR)

True Random Number Generator (RNG)
Generates 32-bit true random number
NIST SP800-22 (NIST special publication 800-22) passed

Real Time Clock (RTC)
- Clock (hour, minute and second)
- Calendar (month, week, date and leap year)
- Selectable 12(am/pm) and 24 hour display
- Time adjustment + or – 30 seconds
- Alarm interrupt
- Periodic interrupt
- BCD format for calendar data

Watch Dog Timer (WDT)
- 32-bit Timer with interrupt and reset when timeout

DMA Controller (SDMAC)
- 8 Channels
  - Each channel has source and destination pair
- Programmable source and destination addresses
  - Addressing mode can be increment, decrement or no change
  - Handshaking interfaces for source and destination peripherals
    - UART, I²C, SPI, ADC12, ADC24

Timer (TMR)
- 32-bit down Counter
  - Selectable 32-bit/16-bit count mode
- Two Channels
- Operation Mode
  - One shot timer mode
  - Periodic timer mode
  - Free running timer mode
- Pre-scale unit generating timer clock
  - (×1, ×1/16, ×1/256)

Advanced Timer (AdvTMR)
- 16-bit down Counter
  - Selectable 16-bit/8-bit count mode
  - Input capture function for each channel
  - Output compare function for each channel
- Four Channels
- Operation Mode
  - One shot timer mode
  - Periodic timer mode
  - Free running timer mode
- Pre-scale unit generating timer clock
  - (×1,×1/2, ×1/4, ×1/8, ×1/32, ×1/128, ×1/512, ×1/1024)
- Timing selection of input capture
  - (Pulse, Rising edge, Falling edge, both edges)
- PWM (Pulse Width Modulation) operation that uses output compares function

3.2.4. Peripherals

SPI for general purpose (SPIM)
- Four Channels
- SPI Clock up to 6 MHz
- FIFO Depth
  - Ch0, Ch1: RX FIFO 8, TX FIFO 8
  - Ch2, Ch3: RX FIFO 8, TX FIFO 2

SPI for NOR flash connection (SPIC)
- Quad SPI Clock up to 48 MHz
- Application eXecute-In-Place (XIP)
- Hardware image transferring feature to internal SRAM
- Programmable source and destination address

UART (UART)
- Three Channels
- FIFO Depth
  - RX FIFO 12, TX FIFO 8
- Programmable baud rate generator
  - Input reference clock; up to 16 MHz
  - Data rate up to 1 Mbps
  - Division of reference clock by (1×16) to (65535 ×16)
- Hardware flow control
- Fully-programmable serial interface characteristics
  - Data can be 5, 6, 7, or 8 bits
  - Even, odd, stick, or no-parity bit generation and detection
  - 1 or 2 stop bit generation

I^2C
- Three Channels
- Transfer mode; Standard mode (100 kbps), Fast mode (400 kbps)
- Master or slave I^2C operation
- 7-bit or 10-bit addressing
- 7-bit combined format transfers
- Bulk transfer mode
- FIFO Depth
  - RX FIFO 6, TX FIFO 6

USB

- Compliant with Universal Serial Bus Specification revision 2.0
- Supports Full Speed (12 Mbps)
- One port, four endpoints
  - Endpoint 1-3 can be configured as interrupt/bulk transfer mode
- Internal DMA Controller

GPIO

- 32 Pins
- Individually programmable as input or output
- Interrupt generation capability from a transition or level condition
- Pull-up/pull-down resistors configurable

12-bit Analog to Digital Convertor (ADC12)

- Successive approximation type
- 12 bits resolution
- Conversion time: 17 cycles at 1 to 12 MHz
- Four channel analog inputs
- Selectable conversion mode (Single/One-time scan/Cyclic scan)
- FIFO Depth 8 for each channel

24-bit Analog to Digital Convertor (ADC24)

- Delta-Sigma type up to 24 bits resolution
- Three channel differential analog inputs
- Conversion time: 4130 cycles at 24 bits resolution
- Selectable conversion mode (Single/One-time scan/Cyclic scan)
- FIFO Depth 16 for each channel
- Configurable analog front end

4. Boot Mode

The MCU supports the several boot modes to switch the boot function. It is possible to select the boot mode by setting the state of the external pins, before de-asserting reset.

The pins of the boot mode is exclusively for an input. The Boot mode can be set by fixing to H (MCU_VDD33) or L (VSS) externally. In addition, these pins cannot be changed during operation. The value needs to be set before de-asserting reset.

The pin name for boot modes and its function are described below. Refer to "Table 4.1 Boot Mode."

Table 4.1 Boot Mode

PIN NAME	FUNCTION
MCU_BOOTMODE0	SRAM pre load setting H/W pre load from SPI Flash to SRAM is selected at the time of boot. 0: SPI (XiP) Boot Mode Pre load is not performed from SPI Flash to SRAM. 1: SRAM pre load & SPI (XiP) Boot Mode Pre load is performed from SPI Flash to SRAM.
MCU_BOOTMODE1	Address Remap setting The size of Code area and SRAM area is selected. Regarding the address of Code and SRAM area, refer to "5. Address Map." 0: Remap0 Mode Code area = 256 KB, SRAM area = 32 KB 1: Remap1 Mode Code area = 224 KB, SRAM area = 64 KB
MCU_BOOTMODE2	SPI Flash Access Boot Mode setting The access mode to SPI Flash at the time of boot and the return from RTC/STOP mode is selected. 0: Single Access Boot Mode 1: Quad Access Boot Mode
MCU_BOOTMODE3	SPI Flash Power Supply Mode setting The power supply source for SPI Flash is selected 0: Internal LDO mode 1: External Power Supply mode
MCU_BOOTMODE4	SPI Flash Direct Access mode / Erase mode setting It is possible to write the program code to the SPI flash memory directly via the other external pins by the FLASH Writer, or erase the SPI flash memory. 0: Normal Boot Mode 1: SPI Flash Direct Access Mode / Erase Mode When using these modes, MCU_BOOTMODE[2:0] signals are necessary to be set to 0b000 or 0b111.

Table 4.2 Boot Mode Setting

Mode	MCU_BOOTMODE					Description
	4	3	2	1	0	
Normal Mode	L	*	*	*	L	SPI (XiP) Boot Mode
	L	*	*	*	H	SRAM pre load & SPI (XiP) Boot Mode
	L	*	*	L	*	Remap0 Mode (Code = 256 KB, SRAM = 32 KB)
	L	*	*	H	*	Remap1 Mode (Code = 224 KB, SRAM = 64 KB)
	L	*	L	*	*	SPI Flash Single Access Boot Mode
	L	*	H	*	*	SPI Flash Quad Access Boot Mode
	L	L	*	*	*	Internal LDO mode
	L	H	*	*	*	External Power Supply mode
SPI Flash writing Mode	H	*	L	L	L	SPI Flash Direct Access Mode
SPI Flash Erase Mode	H	*	H	H	H	SPI Flash Erase Mode

Note: When using MCU_BOOTMODE[3-0] to select the normal boot mode, MCU_BOOTMODE4 is necessary to be tied to 0.

4.1. SRAM pre load setting

User can select the SPI XiP Boot mode or SRAM pre load mode.

- SPI (XiP) Boot Mode
  - The preload from SRAM does not perform but it boots directly from SPI Flash.
  - Transmitting the contents of SPI Flash to SRAM needs to perform by code in SPI Flash.
  - The code on Flash needs to define addresses, such as the SPI Flash code area which is a transmitting agency, SRAM area used as a transmission place, and handler.

- SRAM pre load & SPI (XiP) Boot Mode
  - According to the setting of MCU_BOOTMODE1 port (Remap), the code size of 256 KB from address 0 in SPI Flash or 224 KB are transmitted by H/W. The transmission place address is written to the code area of a head 0x1000.0000. For details, refer to "5. Address Map."
    - MCU_BOOTMODE1 = L **:** 256 KB (Remap0 code area)
    - MCU_BOOTMODE1 = H **:** 224 KB (Remap1 code area)
  - Reset of CPU is released by H/W after completing the transmission to SRAM from SPI Flash.
  - CPU starts code fetch (XiP) from SPI Flash.
  - The address 0x4 of SPI Flash needs to be set the reset vector address to jump to the SRAM.
  - CPU fetches a code from the above-mentioned SRAM address, and continues a boot process.
  - On the SRAM code, the place of handler needs to redefine to SRAM.

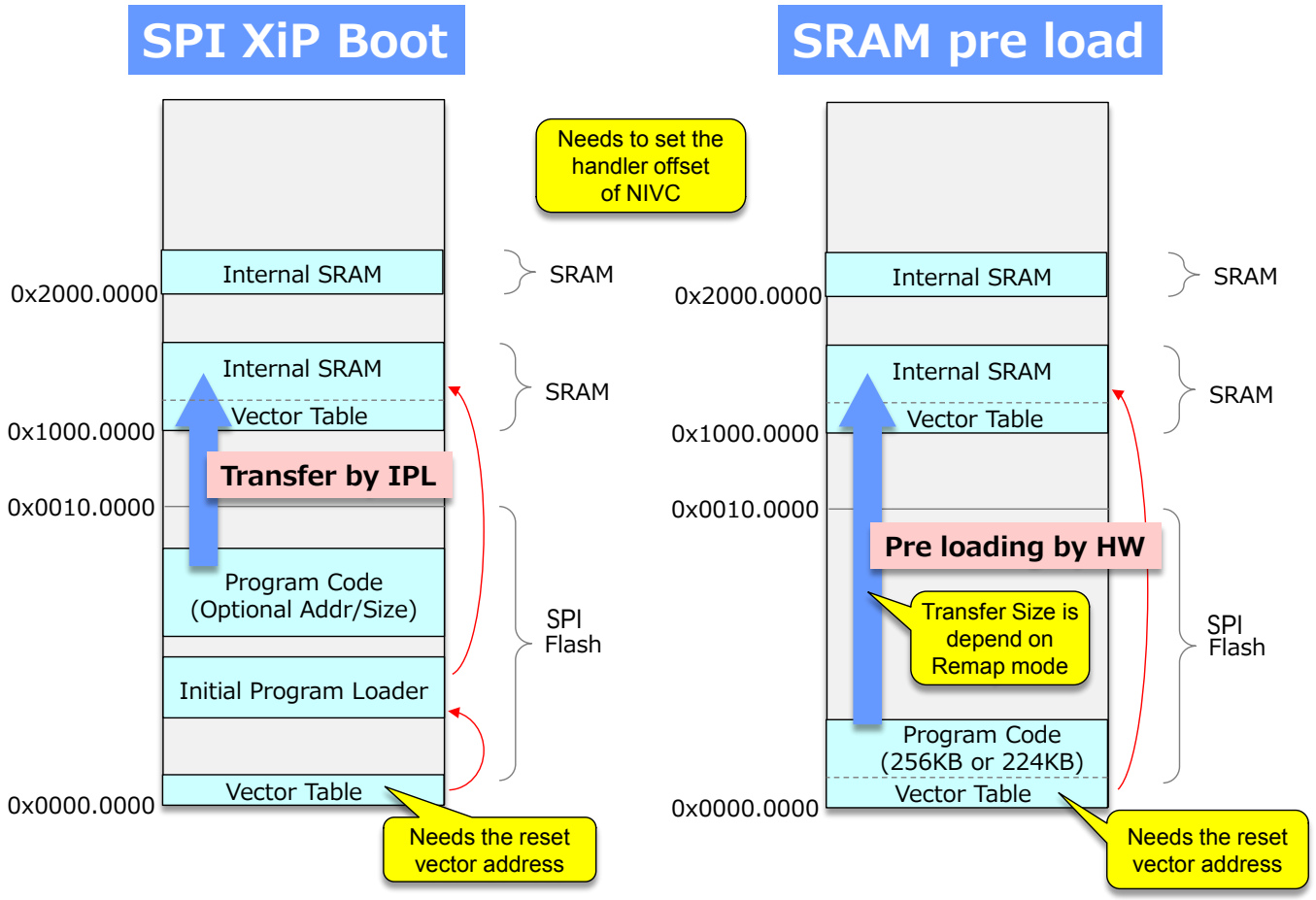


Figure 4.1 SRAM pre load images

4.2. Address Remap setting

Two kinds of address maps which are Code/SRAM different area can be selected. This two kinds of address map is switched by MCU_BOOTMODE1 port.

Refer to "5. Address Map" for each address map of Remap 0/1.

- Remap0 Mode
  - Code area: 256 KB
  - SRAM area: 32 KB

- Remap1 Mode
  - Code area: 224 KB
  - SRAM area: 64 KB

4.3. SPI Flash Access Mode setting

This mode determines the access mode to SPI Flash. User can select the Single mode or Quad mode.

- Single Access Boot Mode
  - It is used to access the SPI flash memory with single access mode.
  - Also when it changes to Quad Access Mode by S/W after boot, it operates by Single Access Mode at the time of reset and the return from RTC/STOP mode.
  - In addition, while operating with XiP to fetch the code from SPI Flash, A change in Quad mode by S/W is not permitted. For details, refer to "SPIC data sheet."

- Quad Access Boot Mode
  - It is used to access the SPI flash memory with quad access mode.
  - In order to use Quad Access Mode, Quad Enable of SPI Flash is needed to set effectively beforehand.
  - In JTAG ICE or SPI Flash direct access mode, when a code is written in SPI Flash, since Quad Enable bit of SPI Flash is 0 (Single) at the time of initial shipment, Quad Enable bit is needed to set 1 after finishing writing the code.

4.4. SPI Flash Power Supply Mode setting

This mode determines the power supply source for SPI Flash. User can select the internal LDO or external power supply.

- Internal LDO mode
  - Internal LDO is selected for SPI Flash power supply.
  - This LDO is dedicated for SPI Flash and supply voltage is tuned to 1.7 V.

- External Power Supply mode
  - External power supply is selected for SPI Flash power supply.
  - Power switch located between MCU_VDD33 pin and internal power line for SPI Flash is enabled so that the power can be supplied from external power source.

Note: The supply voltage specifications are not identical for these two power supply mode. Please refer Electrical Specification section for details.

4.5. SPI Flash Direct Access Mode Setup

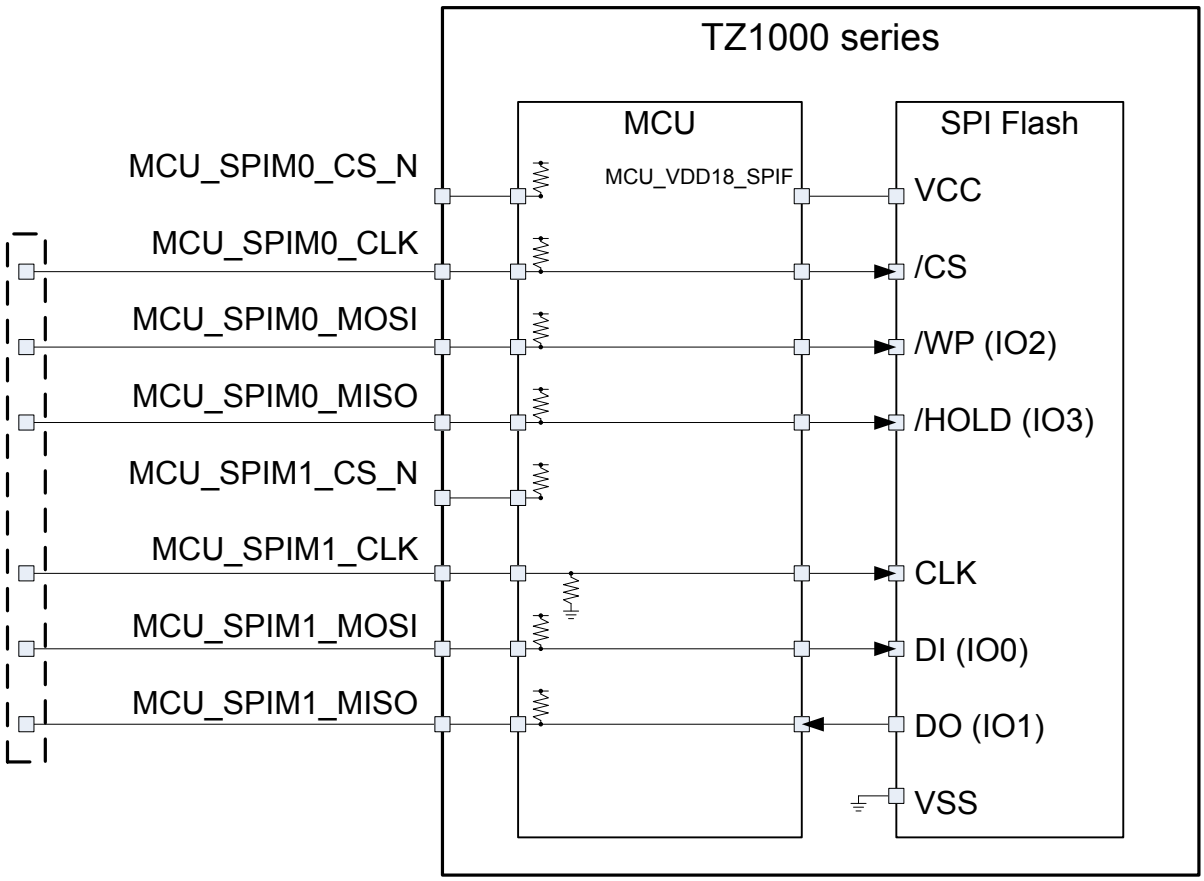
Using an external SPI Flash writer, it is used when writing a code in SPI Flash in a package.

External pins	Connection with SPI Flash	Description
MCU_SPIM0_CS_N	—	pull-up
MCU_SPIM0_CLK	/CS	—
MCU_SPIM0_MOSI	/WP (IO2)	If not using, it is necessary to fix to H.
MCU_SPIM0_MISO	/HOLD (IO3)	If not using, it is necessary to fix to H.
MCU_SPIM1_CS_N	—	pull-up
MCU_SPIM1_CLK	CLK	—
MCU_SPIM1_MOSI	DI (IO0)	—
MCU_SPIM1_MISO	DO (IO1)	—

Note 1: It is possible to use only Single Access Mode in this flash direct access mode. Dual and Quad Access does not support in this mode.

Note 2: In this mode, MCU_SPIM0_CS_N and MCU_SPIM1_CS_N pin are pull-up, in order to avoid the SPI Slave Device of SPIM0/SPIM1 on Board at the time of Flash writing.

Note 3: MCU_SPIM0_*, MCU_SPIM1_* signals are driven by MCU_VDD33.



4.6. SPI Flash Erase Mode

This mode is used to erase the SPI Flash. In order to erase the SPI Flash, set up MCU_BOOTMODE[4]/[2:0], and then de-assert reset. 14 seconds after de-assert reset, erase operation is complete.

5. Address Map

This chapter explains the address map of the MCU section.

5.1. Remap

The address map of SRAMs can be remapped by external pin (MCU_BOOTMODE1). This pin cannot be changed during operation. It is necessary to fix the level before deasserting reset.
Refer to the chapter 4 for the detail of Boot Mode.

The difference of the address map by remapping is as in the following Table 5.1. Any addresses other than SRAM are the same.

Table 5.1 Remap Table

Region	remap 0	remap 1
—	MCU_BOOTMODE1 = 0	MCU_BOOTMODE1 = 1
SRAM T0	128 KB (0x10000000 to 0x1001FFFF)	128 KB (0x10000000 to 0x1001FFFF)
SRAM T1	128 KB (0x10020000 to 0x1003FFFF)	96 KB (0x10020000 to 0x10037FFF)
SRAM T2	32 KB (0x20000000 to 0x20007FFF)	64 KB (0x20000000 to 0x2000FFFF)

5.2. Address Mapping

Figure 5.1 Address Map (1), Figure 5.2 Address Map (2) show the address map of MCU chip which has embedded 288 KB SRAM memories, a lot of peripheral blocks and SPI for flash in package.
Refer to Table 5.2 for each region of address map.

Table 5.2 Address Map regions

Address Map	Region
Code	Instruction fetches are performed over the ICode bus. Data accesses are performed over the DCode bus.
SRAM (Bit band region)	Instruction fetches and data accesses are performed over the system bus.
SRAM (Bit band alias)	Alias region. Data accesses are aliases. Instruction accesses are not aliases.
Peripheral (Bit band region)	Instruction fetches and data accesses are performed over the system bus.
Peripheral (Bit band region)	Alias region. Data accesses are aliases. Instruction accesses are not aliases.
Undefined	Undefined area.
System	System segment for vendor system peripherals. This memory region is XN, and so instruction fetches are prohibited. An MPU, if present, cannot change this.

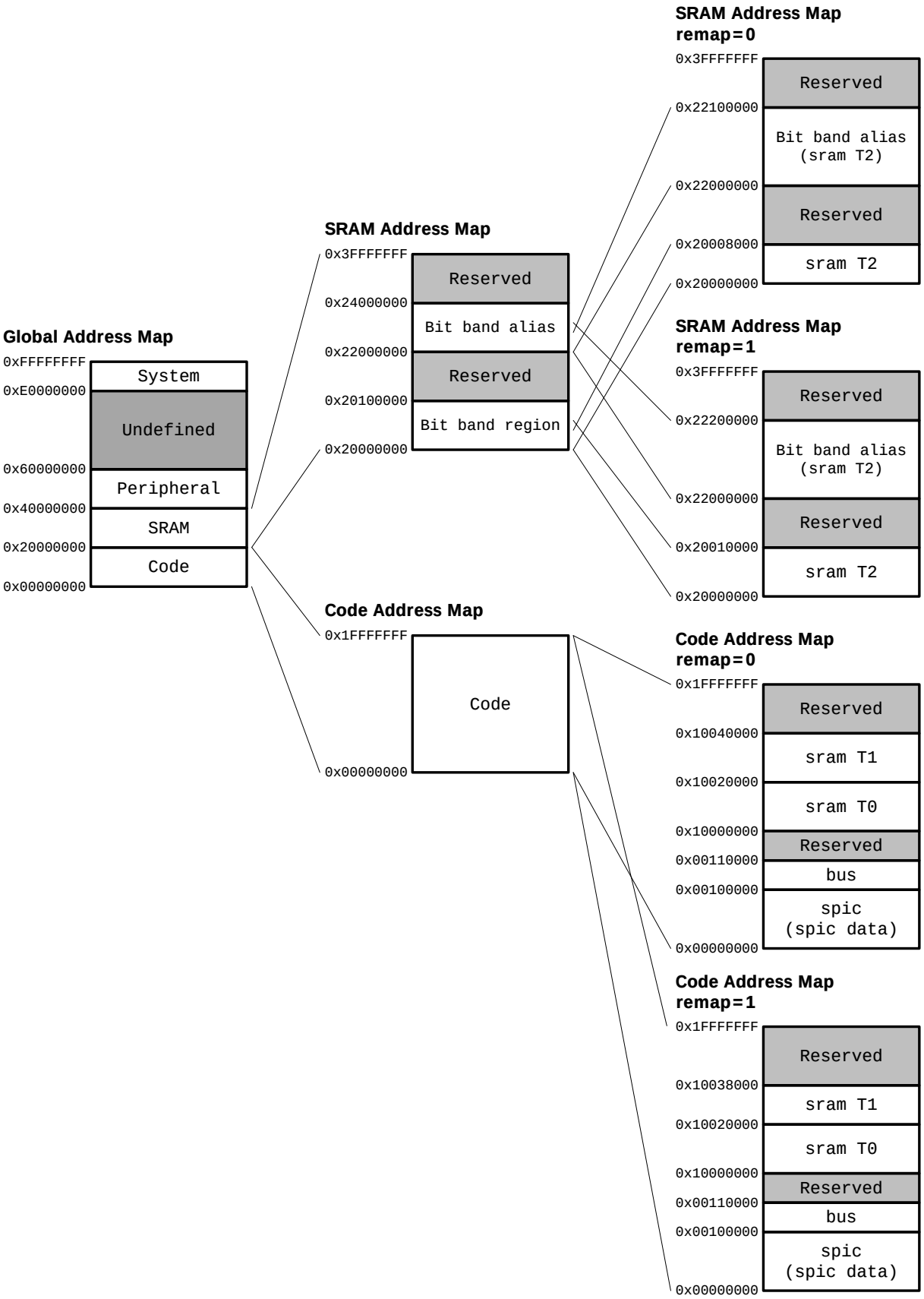


Figure 5.1 Address Map (1)

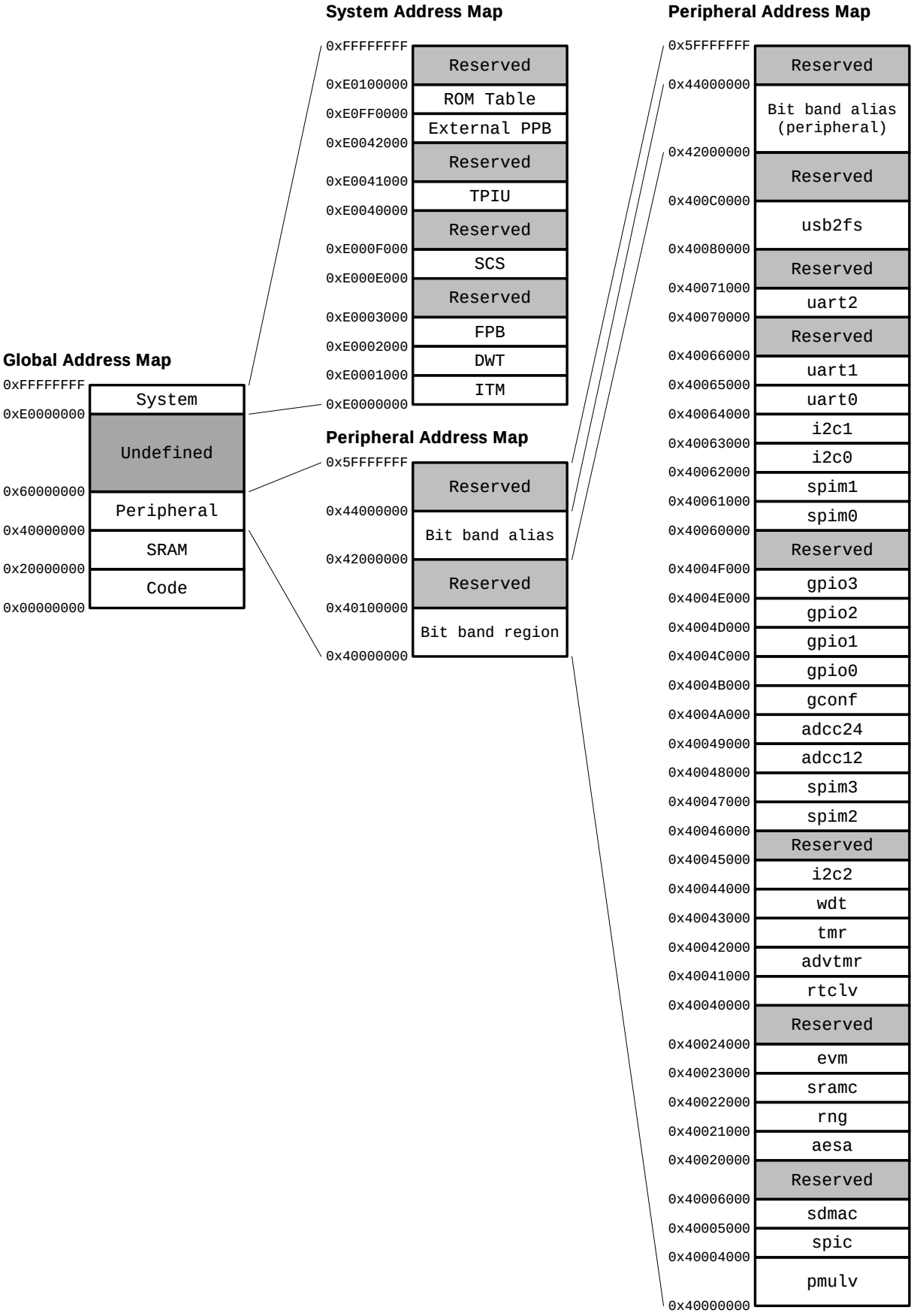


Figure 5.2 Address Map (2)

6. Revision History

Table 6.1 Revision History

Revision	Date	Description
0.1	2014-03-12	Newly released
0.2	2014-07-16	Revised for rev 2.0: added bus address region to Figure 5.1.
0.3	2014-09-29	Modified for VDD33 = 1.8 V specification. Deleted Debug section.
0.4	2014-10-07	Added "4.6. SPI Flash Erase Mode" section.
0.5	2014-10-22	Deleted "3.2.1. Configuration Summary" section. Corrected Power Supply Voltage from 2.0 V to 2.1 V in section 1.1.
0.6	2014-12-17	Corrected "SPI Flash Direct Access Mode" of Table 4.2. Corrected UART maximum data rate in section 3.2.5.
1.0	2015-01-21	Official version.
1.1	2015-04-09	Modified 1.8 V Voltage range in section 1.1.
1.2	2015-06-08	Revised Peripherals GPIO in Section 3.2.4.
1.3	2018-01-25	Changed header, footer and the last page. Changed corporate name and descriptions. Modified Arm logo and descriptions.

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