Application Processor Lite *ApP Lite*

TZ1000 Series

Reference Manual

MCU Bus Interconnect

Revision 1.1

2018-02

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

© 2015-2018
Toshiba Electronic Devices & Storage Corporation

Table of Contents

List of Figures

List of Tables

Preface

This document provides the specification for the MCU Bus Interconnect designed for the TZ1000 Series.

Intended Audience

This document is intended for the following users.

Driver software developers.

System designers

Conventions in this Document

- The following notational conventions apply to numbers:
  Hexadecimal number: 0xABC
  Decimal number: 123 or 0d123 (only when it should be explicitly indicated that the number is decimal)
  Binary number: 0b111 (It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.)
- Low active signals are indicated with a name suffixed with "_N".
- A signal is asserted when it goes to its active level while it is de-asserted when it goes to its inactive level.
- A set of multiple signals may be referred to as [m:n].
  Example: S[3:0] indicates four signals, S3, S2, S1 and S0, collectively.
- In the text, register names are enclosed in brackets *[ ]*.
  Example:*[ABCD]*
- A set of multiple registers, fields or bits of the same type may be described collectively using "n".
  Example: *[XYZ1], [XYZ2], and [XYZ3] to [XYZn]*
  A range of register bits are referred to as [m:n].
  Example: [3:0] indicates a range from bit 3 to bit 0.
- Values set in registers are indicated using either a hexadecimal or binary number.
- Example: *[ABCD]*.EFG = 0x01 (hexadecimal), *[XYZn]*.VW = 1 (binary)
- Words and bytes are defined as follows:
  Byte: 8 bits
  Halfword: 16 bits
  Word: 32 bits
  Doubleword: 64 bits
- Register bit attributes are defined as follows:
  R: Read-only
  W: Write-only
  W1C: Clear by write of 1 (a write of "1" clears the corresponding bit to 0)
  W1S: Set by write of 1 (a write of "1" sets the corresponding bit to 1)
  R/W: Read/Write
  R/W0C: Read/Clear by write of 0
  R/W1C: Read/Clear by write of 1
  R/W1S: Read/Set by write of 1
  RS/WC: Set by read/Clear by write (set after a read and cleared after a data write)
- Registers only support word access unless otherwise specified.
- Any registers defined as Reserved in the text must not be rewritten. Also, any values read from such registers should not be used.
- Any bits for which default values are defined as "-" would return undefined values if read.
- When a data is written to a register containing both writable and read-only (R) bit fields, its default values should be written to read-only (R) bit fields. For any bit fields with default values defined as "-", refer to the definitions of the relevant register.
- Default values should be written to any reserved bit fields in a write-only register. For any bit fields with default values defined as "-", refer to the definitions of the relevant register.

Abbreviation

These specifications introduce a part of the abbreviation which they used

AHB	Advanced High-Performance Bus
APB	Advanced Peripheral Bus

* All other company names, product names, and service names mentioned herein may be trademarks of their respective companies.

1. Overview

This document is the specification of the TZ1000 MCU Bus. The feature of the TZ1000 MCU Bus is as follows.

- The TZ1000 MCU Bus is a 32-bit interconnect which consists of AHB Bus Matrix, APB0 Bus, APB1 Bus, APB2 Bus, and some bridge circuits.
- Communication via AHB Bus Matrix can be done with 0 cycle latency.
  - Except for accesses through the asynchronous or semi-synchronous bridge which needs some additional latency.
- The AHB Bus Matrix arbiters do the arbitration with the fixed priority order.
- Remap input (Boot time configurable) can switch the address map of the SRAM.
- Bus Error Logging for the software debug is not supported.
- Low power technique based on the notification of the bus activities to the PMU is supported.

2. Connectivity Matrix

The connectivity matrix of the TZ1000 MCU Bus is shown in Figure 2.1. The black circles on the cross points indicate the communication available between the masters and the slaves.

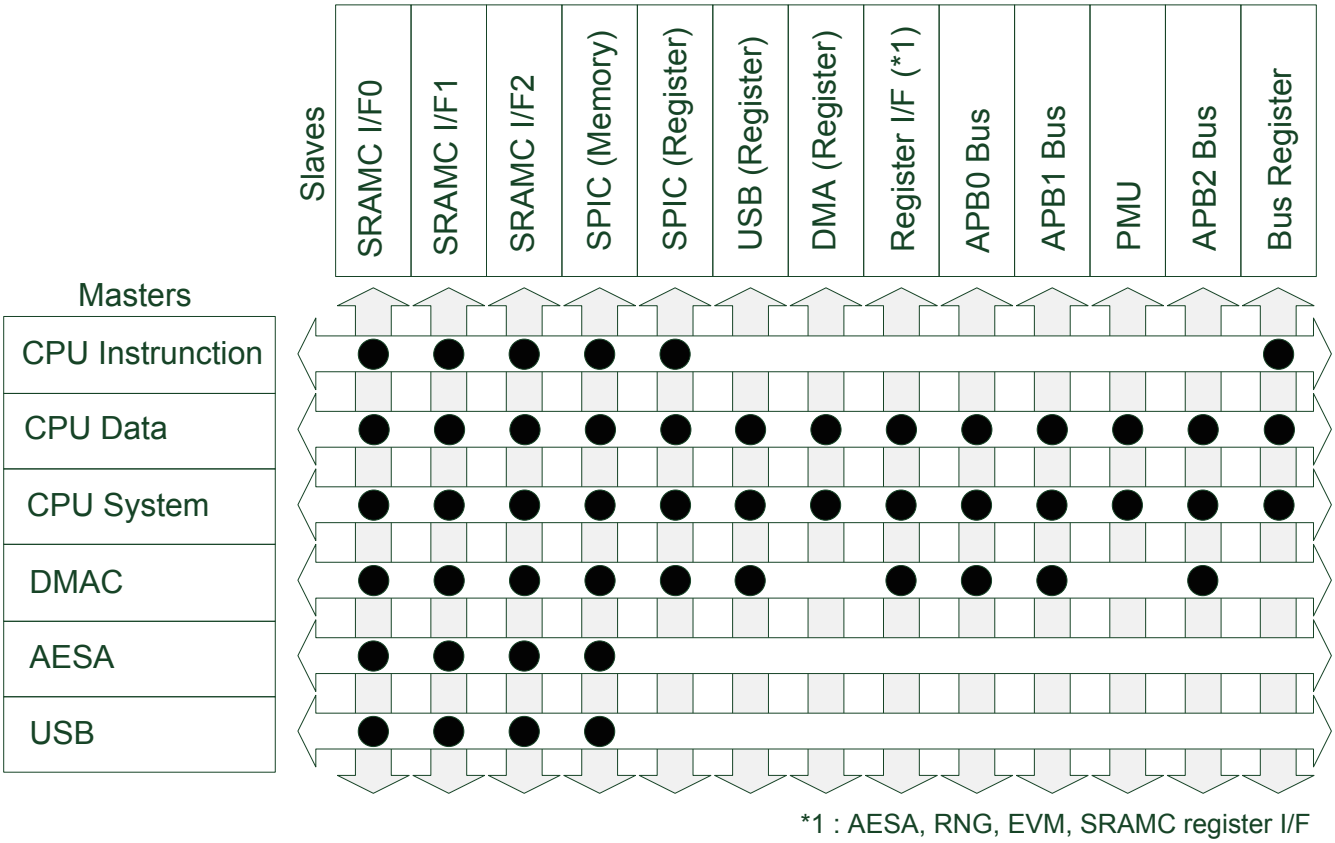

Figure 2.1 Connectivity Matrix

3. Clock

The TZ1000 MCU Bus supports the data transfer between the different clock domains. So, several clocks are supplied to the Bus block. From the PMU, the clocks of CD_MPIER, CD_PPIER0, CD_PPIER1, CD_PPIER2, and CD_PMULV domains are supplied to the Bus block. Each clock can be stopped by software using the PMU register except for the clock for the AHB Bus Matrix and the bridge circuit between the AHB Bus Matrix and the PMU.

4. Register map

Table 4.1 Register Map

Register Name	Type	Width	Reset Value	Address Offset
BUS_BUSY	RO	32	0x0000 0000	0x0000 FFFC

5. Function

5.1. Power Management

- Sleep0: Normal operation.
- Sleep1/2, WAIT, WAIT-RETENTION, and RETENTION: Bus transaction control is disabled because the clock of the AHB Bus Matrix stops. Before transition to these modes, it should be confirmed that no bus transactions are issued according to the transition procedure of the DMAC, AESA, USB, and PMU. This block returns to the state before the transition.
- RTC and STOP: Bus transaction control is disabled because the clock of the AHB Bus Matrix stops. Before transition to these modes, it should be confirmed that no bus transactions are issued according to the transition procedure of the DMAC, AESA, USB, and PMU. When returning from these modes, the start-up procedure should be done according to Section 5.2.1, because the clock supply and reset assertion are initialized in the PMU.

5.2. Start-up and Stop Procedure

The following is the start-up and stop procedures of the Bus block. Before a block is accessed, its own start-up and stop procedure should be done. The Bus block should be started up before the accessed block start-up. And the Bus block should be stopped after the accessed block is stopped.

5.2.1. Start-up Sequence

The Bus block is started up after the reset deassertion sequence of the PMU, because the boot of this product needs the Bus block. The other blocks are started up with the settings as follows. The successive writes to the same register can be done simultaneously.

5.2.1.1. Start-up of Bridge Circuit between USB Device and AHB Bus Matrix

(1) It is confirmed that the power is supplied to the power domain (PU) which includes the bridge circuit between the USB device and the AHB Bus Matrix by reading the PMU.*[PSW_PU]*.PSW_PU_VDDCS and PMU.*[PSW_PU]*.PSW_PU_VDDCW.

(2) The dividing ratio of the clock supplied to the bridge circuit from the CD_USBB clock domain is set to the PMU.*[PRESCAL_MAIN]*.PSSEL_CD_USBB, except 0x0.

(3) The bridge circuit is supplied with the clock by setting the PMU.*[CG_OFF_PU]*.CG_mpierclk_h2hdnu_hclk.

(4) The bridge circuit is supplied with the clock by setting the PMU.*[CG_OFF_PU]*.CG_mpierclk_h2hupu_hclk.

(5) The reset of the CD_MPIER and CD_USBB clock domains for the bridge circuit is deasserted by setting the PMU.*[SRST_OFF_PU]*.SRST_asyncrst_h2hdnu_hrstn.

(6) The reset of the CD_MPIER clock domain for the bridge circuit is deasserted by setting the PMU.*[SRST_OFF_PU]*.SRST_asyncrst_h2hupu_hrstn.

5.2.1.2. Start-up of Bridge circuit between AESA, RNG, EVM, or SRAMC register and AHB Bus Matrix

(1) The clock of the bridge circuit which is connected to AESA, RNG, EVM, or SRAMC register interface is supplied by setting the PMU.*[CG_OFF_PM_0]*.CG_mpierclk_h2pm_hclk.

(2) The reset of the bridge circuit for the CD_MPIER clock domain is deasserted by setting the PMU.*[SRST_OFF_PM_0]*.SRST_asyncrst_h2pm_hrstn.

5.2.1.3. APB0 Bus Start-up

(1) The dividing ratio of the clock supplied to the APB0 Bus from the CD_PPIER0 clock domain is set to the PMU.*[PRESCAL_MAIN]*.PSSEL_CD_PPIER0, except 0x0.

(2) The clock of the CD MPIER clock domain is supplied to the APB0 Bus by setting the PMU.*[CG_OFF_PM_1]*.CG_mpierclk_h2hp0_hclk.

(3) The clock of the CD_PPIER0 clock domain is supplied to the APB0 Bus by setting the PMU.*[CG_OFF_PM_1]*.CG_ppier0clk_h2pp0_hclk.

(4) The reset of the CD_MPIER clock domain for the APB0 Bus is deasserted by setting the PMU.*[SRST_OFF_PM_1]*.SRST_asyncrst_h2hp0_hrstn.

(5) The reset of the CD_PPIER0 for the APB0 Bus is deasserted by setting the PMU.*[SRST_OFF_PM_1]*.SRST_asyncrst_h2pp0_hrstn.

5.2.1.4. APB1 Bus Start-up

(1) It is confirmed that the power is supplied to the power domain (PP1) which includes the APB1 Bus by reading the PMU.*[PSW_PP1]*.PSW_PP1_VDDCS and PMU.*[PSW_PP1]*.PSW_PP1_VDDCW.

(2) The dividing ratio of the clock supplied to the APB1 Bus from the CD_PPIER1 clock domain is set to the PMU.*[PRESCAL_MAIN]*.PSSEL_CD_PPIER1, except 0x0.

(3) The clock of the CD MPIER clock domain is supplied to the APB1 Bus by setting the PMU.*[CG_OFF_PM_2]*.CG_mpierclk_h2hp1_hclk.

(4) The clock of the CD_PPIER1 clock domain is supplied to the APB1 Bus by setting the PMU.*[CG_OFF_PP1]*.CG_ppier1clk_h2pp1_hclk.

(5) The reset of the CD_MPIER clock domain for the APB1 Bus is deasserted by setting the PMU.*[SRST_OFF_PM_2]*.SRST_asyncrst_h2hp1_hrstn.

(6) The reset of the CD_PPIER1 for the APB1 Bus is deasserted by setting the PMU.*[SRST_OFF_PP1]*.SRST_asyncrst_h2pp1_hrstn.

5.2.1.5. APB2 Bus Start-up

(1) The dividing ration of the clock supplied to the APB2 Bus from the CD_PPIER2 clock domain is set to the PMU.*[PRESCAL_MAIN]*.PSSEL_CD_PPIER2, except 0x0.

(2) The clock of the CD_MPIER clock domain is supplied to the APB2 Bus by setting the PMU.*[CG_OFF_PM_2]*. CG_mpierclk_h2hp2_hclk.

(3) The clock of the CD_PPIER2 clock domain is supplied to the APB2 Bus by setting the PMU.*[CG_OFF_PM_2]*.CG_ppier2clk_h2pp2_hclk.

(4) The reset of the CD_MPIER clock domain for the APB2 Bus is deasserted by setting the PMU.*[SRST_OFF_PM_2]*.SRST_asyncrst_h2hp2_hrstn.

(5) The reset of the CD_PPIER2 clock domain for the APB2 Bus is deasserted by setting the PMU.*[SRST_OFF_PM_2]*.SRST_asyncrst_h2pp2_hrstn.

5.2.2. Stop Sequence

5.2.2.1. Stop of Bridge Circuit between USB device and AHB Bus Matrix

(1) The reset of CD_MPIER domain for the bridge circuit between the USB device and the AHB Bus Matrix is asserted by setting the PMU.*[SRST_ON_PU]*.SRST_asyncrst_h2hupu_hrstn.

(2) The reset of the CD_MPIER and CD_USBB domains for the bridge circuit is asserted by setting the PMU.*[SRST_ON_PU]*.SRST_asyncrst_h2hdnu_hrstn.

(3) The clock of the CD_MPIER clock domain to the bridge circuit is stopped by setting the PMU.*[CG_ON_PU]*.CG_mpierclk_h2hupu_hclk.

(4) The clock of the CD_MPIER clock domain to the bridge circuit is stopped by setting the PMU.*[CG_ON_PU]*.CG_mpierclk_h2hdnu_hclk.

5.2.2.2. Stop of Bridge Circuit between AESA, RNG, EVM, or SRAMC register and AHB Bus Matrix

(1) The reset of the CD_MPIER clock domain for the bridge circuit between the AESA, RNG, EVM, and SRAMC register interface is asserted by setting the PMU.*[SRST_ON_PM_0]*.SRST_asyncrst_h2pm_hrstn.

(2) The CD_MPIER clock domain for the bridge circuit is stopped by setting the PMU.*[CG_ON_PM_0]*.CG_mpierclk_h2pm_hclk.

5.2.2.3. APB0 Bus Stop

(1) The reset of CD_PPIER0 clock domain for the APB0 Bus is asserted by setting the PMU.*[SRST_ON_PM_1]*.SRST_asyncrst_h2pp0_hrstn.

(2) The reset of CD_MPIER clock domain for the APB0 Bus is asserted by setting the PMU.*[SRST_ON_PM_1]*.SRST_asyncrst_h2hp0_hrstn.

(3) The clock of the CD_PPIER1 clock domain for the APB0 Bus is stopped by setting the PMU.*[CG_ON_PM_1]*.CG_ppier0clk_h2pp0_hclk.

(4) The clock of the CD_MPIER clock domain for the APB0 Bus is stopped by setting the PMU.*[CG_ON_PM_1]*.CG_mpierclk_h2hp0_hclk.

5.2.2.4. APB1 Bus Stop

(1) The reset of the CD_PPIER1 clock domain for the APB1 Bus is asserted by setting the PMU.*[SRST_ON_PP1]*.SRST_asyncrst_h2pp1_hrstn.

(2) The reset of the CD_MPIER clock domain for the APB1 Bus is asserted by setting the PMU.*[SRST_ON_PM_2]*.SRST_asyncrst_h2hp1_hrstn.

(3) The clock of the CD_PPIER1 clock domain for the APB1 Bus is stopped by setting the PMU.*[CG_ON_PP1]*.CG_ppier1clk_h2pp1_hclk.

(4) The clock of the CD_MPIER clock domain for the APB1 Bus is stopped by setting the PMU.*[CG_ON_PM_2]*.CG_mpierclk_h2hp1_hclk.

5.2.2.5. APB2 Bus Stop

(1) The reset of the CD_PPIER2 clock domain for the APB2 Bus is asserted by setting the PMU.*[SRST_ON_PM_2]*.SRST_asyncrst_h2pp2_hrstn.

(2) The reset of the CD_MPIER clock domain for the APB2 Bus is asserted by setting the PMU.*[SRST_ON_PM_2]*.SRST_asyncrst_h2hp2_hrstn.

(3) The clock of the CD_PPIER2 clock domain for the APB2 Bus is stopped by setting the PMU.*[CG_ON_PM_2]*.CG_ppier2clk_h2pp2_hclk.

(4) The clock of the CD_MPIER clock domain for the APB2 Bus is stopped by setting the PMU.*[CG_ON_PM_2]*. CG_mpierclk_h2hp2_hclk.

5.2.3. Other Block Start-up and Stop Procedure

The Bus circuits which are used to access the blocks other than described above cannot be stopped by software after the system start-up. So there are no special procedures for the start-up or stop of the Bus blocks.

5.3. Frequency Setting

The change of the frequency of the MCU Bus clock can be done by the setting of the prescaler in the PMU. The following registers are necessary to change the frequency.

- PMU.*[PRESCAL_MAIN]*.PSSEL_CD_MPIER: The clock frequency of the CD_MPIER clock domain is changed.
- PMU.*[PRESCAL_MAIN]*.PSSEL_CD_PPIER0: The clock frequency of the CD_PPIER0 clock domain is changed.
- PMU.*[PRESCAL_MAIN]*.PSSEL_CD_PPIER1: The clock frequency of the CD_PPIER1 clock domain is changed.
- PMU.*[PRESCAL_MAIN]*.PSSEL_CD_PPIER2: The clock frequency of the CD_PPIER2 clock domain is changed.

6. Details of MCU Bus Interconnect Register

6.1. BUS_BUSY

BUS_BUSY			
Description	Bus busy flag for monitoring whether there are outstanding transactions on APB buses. For detail of procedure for power mode transition using this register, refer to Chapter 2. MCU Power Management Unit.		
Address Region	bus	**Type:**	RO
Offset	0x0000 FFFC		
Physical address View0	0x0010 FFFC		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:4	Reserved	-	-	-
3	APBM_BUSY	APB bus for AESA, RNG, EVM, SRAMC register busy 0 : IDLE 1 : BUSY	RO	0
2	APB2_BUSY	APB2 bus busy 0 : IDLE 1 : BUSY	RO	0
1	APB1_BUSY	APB1 bus busy 0 : IDLE 1 : BUSY	RO	0
0	APB0_BUSY	APB0 bus busy 0 : IDLE 1 : BUSY	RO	0

7. Priority at Access Contention

7.1. Arbiter Priority

The arbiter of the TZ1000 MCU Bus does not support the QoS function. It has the fixed priority order. When the access contention occurs, the priority is as the following order unless it is in lock-access.

(1) USB
(2) AESA
(3) DMAC
(4) CPU system I/F
(5) CPU data I/F
(6) CPU instruction I/F

7.2. Lock-access

While a master is executing a lock-access, other higher prioritized masters cannot take over the lock-access master.

7.3. Arbitration Change during Burst Transfer

When a master A is executing a burst transfer and a higher prioritized master B issues its request to the same slave, the arbiter of the TZ1000 MCU Bus operates as follows.

- In the case that the master A transfer is in the lock-access:
  - The master B transfer is done after the completion of the master A transfer.
- In the case that the master A transfer is not in the lock-access:
  - The Bus arbiter notifies to the slave that the master A transfer is stopped before the transfer completion. The Bus interface of the master A is inserted with wait cycles and notified that the remaining transfer request is suspended.
  - The master B transfer is done.
  - The Bus arbiter is doing bus arbitration. If the remaining transfer request of the master A wins the arbitration, the AHB Bus Matrix issues the undefined length burst transfer to the slave.

8. Bus Error

The TZ1000 MCU Bus may return an error response to the master. The causes of the error response are as follows.

- Access to the reserved region
- Access to the slave which is not connected to the initiating master.
- Error response from a slave

8.1. Bus Error by Reserved Region Access

If a master issues a transfer request to a reserved region, the TZ1000 MCU Bus will return an error response to the master. The Bus, however, does not return the error response depending on the combination of a master and a reserved region. Table 8.1 shows the bus error status at a master's access to a reserved region.

Table 8.1 Reserved region access and bus error

Master	*CPU instruction I/F*	*CPU data I/F*	*CPU system I/F*	*DMAC*	*AESA*	*USB*
Address						
0x40045000 to 0x40045FFF	ERROR	NO ERROR	NO ERROR	NO ERROR	ERROR	ERROR
0x4004F000 to 0x4005FFFF	ERROR	NO ERROR	NO ERROR	NO ERROR	ERROR	ERROR
the other reserved addresses	ERROR	ERROR	ERROR	ERROR	ERROR	ERROR

9. Restriction

9.1. Register Access Width

The access to the following slaves is supported with only 32-bit wide. 16-bit and 8-bit accesses are not supported. The software access should be done with 32-bit wide.

- AESA, RNG, EVM, and SRAMC registers
- ADC12, ADC24, TMR, AdvTMR, WDT, I2C0-2, SPIM0-3, GCONF, GPIO0-3, UART0-3, and RTC
- PMU

10. Revision History

Table 10.1 Revision History

Revision	Date	Description
0.1	2014-03-28	Newly released
0.2	2014-03-31	4.2.1.4 APB1 Bus Start-up sequence: - modified register name
0.3	2014-06-18	Modified Table 6.1 address
0.4	2014-09-29	Revised for rev 2.0
1.0	2015-01-22	Official version
1.1	2018-02-05	Changed header, footer and the last page. Changed corporate name and descriptions. Added description of the trademark.

RESTRICTIONS ON PRODUCT USE

Toshiba Corporation and its subsidiaries and affiliates are collectively referred to as “TOSHIBA”.
Hardware, software and systems described in this document are collectively referred to as “Product”.

- TOSHIBA reserves the right to make changes to the information in this document and related Product without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, devices related to electric power, and equipment used in finance-related fields. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**