Application Processor Lite *ApP Lite*

TZ1000 Series

Reference Manual

MCU General-Purpose Input/Output Controller

Revision 1.1

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TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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Preface

This document provides the specification for the MCU General-Purpose Input/Output Controller designed for the TZ1000 Series.

Intended Audience

This document is intended for the following users.

Driver software developers.

System designers

Conventions in this document

- The numerical values are expressed as follows.
  Hexadecimal number: 0xABC
  Decimal number: 123 or 0d123 - Only when it needs to be explicitly shown that they are decimal numbers.
  Binary number: 0b111 - It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [3:0].
  [3:0] shows four signal names 3, 2, 1, and 0 together.
- The characters surrounded by [] defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1]***, ***[XYZ2]***, and ***[XYZ3]*** to ***[XYZn]***
- The bit range of a register is written like as [3:0].
  Example: Bit[3:0] expresses the range of bits 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***.EFG = 0x01 (hexadecimal), ***[XYZn]***.VW = 1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8-bit
  Half word: 16-bit
  Word: 32-bit
  Double word: 64-bit
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, don't use the read value.
- Properties of each bit in a register are expressed as follows.
  R:Read only
  W: Write only
  W1C: Write 1 Clear - The corresponding bit is cleared (=0) when "1" is written to this bit.
  W1S: Write 1 Set - The corresponding bit is set (=1) when "1" is written to this bit.
  R/W: Read and Write are possible.
  R/W0C: Read/Write 0 Clear
  R/W1C: Read/Write 1 Clear
  R/W1S: Read/Write 1 Set
  RS/WC: Read Set/Write Clear - Set after read operation, cleared after write operation.
- The value read from the bit having default value of "—" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value. In the cases that default is "—," follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value. In the cases that default is "—," follow the definition of each register.

Abbreviation

These specifications introduce a part of the abbreviation which they used

MIS	Masked Interrupt Status
PMU	Power Management Unit

1. Overview

This module consists of general purpose I/O ports.

The main feature is as follows.

- Compliant with the Arm® AMBA® (2.0). The APB slave.
- 4 Channels (GPIO0, GPIO1, GPIO2, GPIO3)
- 8 programmable input and output pins for each channel - The reset state is input as a default.
- The interrupt trigger is selectable for each pin between an edge or a level trigger.
- Bit masking function for read and write using its address line.

2. Block Diagram

The internal block diagram is shown in Figure 2.1.

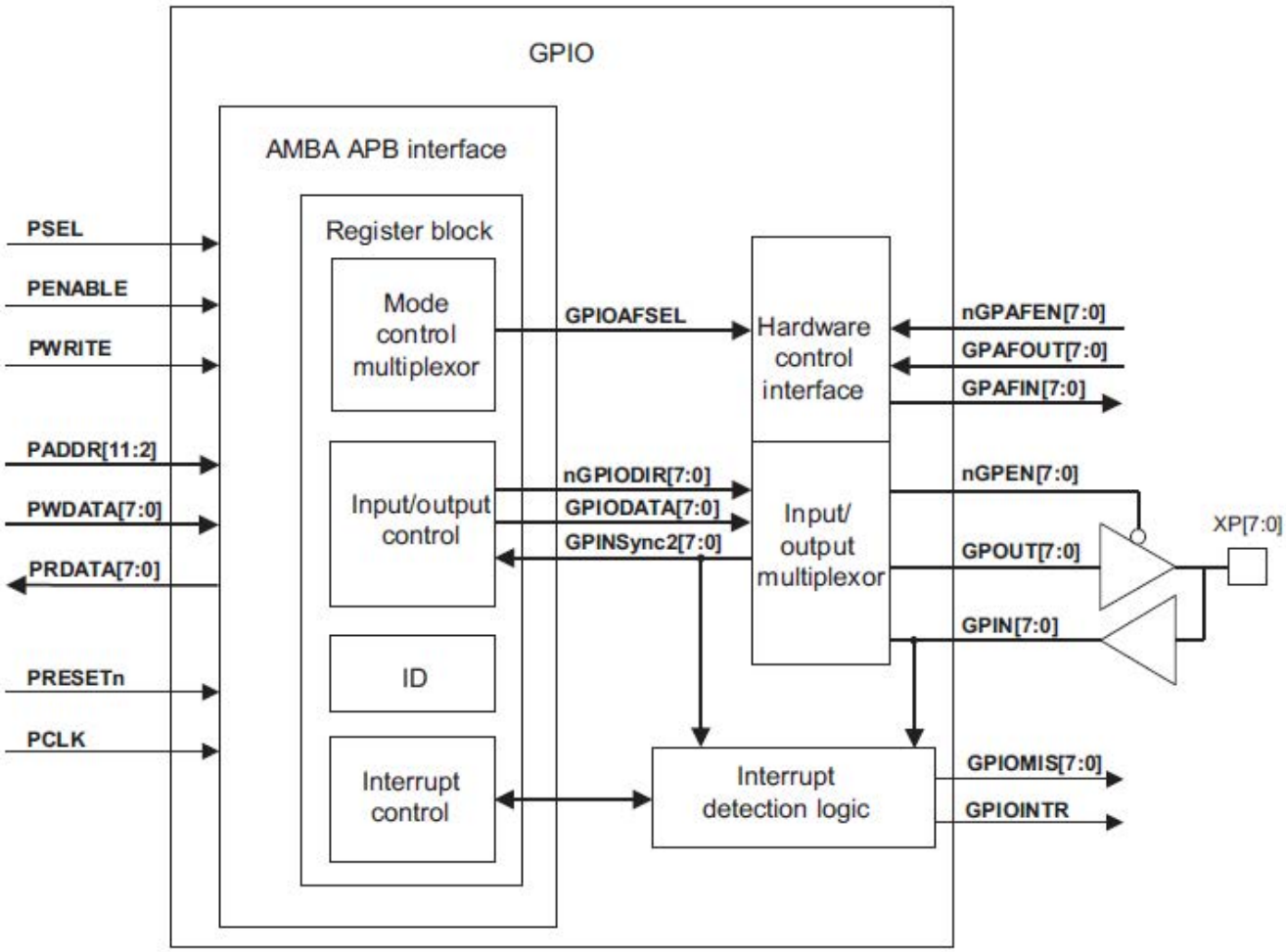


Figure 2.1 GPIO internal block diagram

The outlines of the internal blocks of the GPIO are as follows.

- **AMBA APB interface**
  It has the APB slave interface accessed by the CPU. It is used to access registers which are allocated in the 4 KB address space.
- **Interrupt detection logic**
  It controls interrupt signals issued from the GPIO pins.
- **Input/output multiplexor**
  It is a multiplexor for input or output data through the GPIO pins.
- **Hardware control interface**
  It controls the input or output signals through the GPIO pins. It is not used by the TZ1000 Series.

3. Address Map

Table 3.1 MCU General-Purpose Input/Output Controller 0 Register Map

Register Name	Type	Width	Reset Value	Address Offset
GPIO0_GPIODATA	RW	32	0x0000 0000	0x0000 0000-
GPIO0_GPIODIR	RW	32	0x0000 0000	0x0000 0400
GPIO0_GPIOIS	RW	32	0x0000 0000	0x0000 0404
GPIO0_GPIOIBE	RW	32	0x0000 0000	0x0000 0408
GPIO0_GPIOIEV	RW	32	0x0000 0000	0x0000 040C
GPIO0_GPIOIE	RW	32	0x0000 0000	0x0000 0410
GPIO0_GPIORIS	RO	32	0x0000 0000	0x0000 0414
GPIO0_GPIOMIS	RO	32	0x0000 0000	0x0000 0418
GPIO0_GPIOIC	RW	32	0x0000 0000	0x0000 041C
GPIO0_GPIOITCR	RW	32	0x0000 0000	0x0000 0600
GPIO0_GPIOITIP1	RW	32	0x0000 0000	0x0000 0604
GPIO0_GPIOITIP2	RW	32	0x0000 0000	0x0000 0608
GPIO0_GPIOITOP1	RW	32	0x0000 0000	0x0000 060C
GPIO0_GPIOITOP2	RO	32	0x0000 0000	0x0000 0610
GPIO0_GPIOITOP3	RW	32	0x0000 0000	0x0000 0614
GPIO0_GPIOPERIPHID0	RO	32	0x0000 0061	0x0000 0FE0
GPIO0_GPIOPERIPHID1	RO	32	0x0000 0010	0x0000 0FE4
GPIO0_GPIOPERIPHID2	RO	32	0x0000 0004	0x0000 0FE8
GPIO0_GPIOPERIPHID3	RO	32	0x0000 0000	0x0000 0FEC
GPIO0_GPIOPCELLID0	RO	32	0x0000 000D	0x0000 0FF0
GPIO0_GPIOPCELLID1	RO	32	0x0000 00F0	0x0000 0FF4
GPIO0_GPIOPCELLID2	RO	32	0x0000 0005	0x0000 0FF8
GPIO0_GPIOPCELLID3	RO	32	0x0000 00B1	0x0000 0FFC

Table 3.2 MCU General-Purpose Input/Output Controller 1 Register Map

Register Name	Type	Width	Reset Value	Address Offset
GPIO1_GPIODATA	RW	32	0x0000 0000	0x0000 0000-
GPIO1_GPIODIR	RW	32	0x0000 0000	0x0000 0400
GPIO1_GPIOIS	RW	32	0x0000 0000	0x0000 0404
GPIO1_GPIOIBE	RW	32	0x0000 0000	0x0000 0408
GPIO1_GPIOIEV	RW	32	0x0000 0000	0x0000 040C
GPIO1_GPIOIE	RW	32	0x0000 0000	0x0000 0410
GPIO1_GPIORIS	RO	32	0x0000 0000	0x0000 0414
GPIO1_GPIOMIS	RO	32	0x0000 0000	0x0000 0418
GPIO1_GPIOIC	RW	32	0x0000 0000	0x0000 041C
GPIO1_GPIOITCR	RW	32	0x0000 0000	0x0000 0600
GPIO1_GPIOITIP1	RW	32	0x0000 0000	0x0000 0604
GPIO1_GPIOITIP2	RW	32	0x0000 0000	0x0000 0608
GPIO1_GPIOITOP1	RW	32	0x0000 0000	0x0000 060C
GPIO1_GPIOITOP2	RO	32	0x0000 0000	0x0000 0610
GPIO1_GPIOITOP3	RW	32	0x0000 0000	0x0000 0614
GPIO1_GPIOPERIPHID0	RO	32	0x0000 0061	0x0000 0FE0
GPIO1_GPIOPERIPHID1	RO	32	0x0000 0010	0x0000 0FE4
GPIO1_GPIOPERIPHID2	RO	32	0x0000 0004	0x0000 0FE8
GPIO1_GPIOPERIPHID3	RO	32	0x0000 0000	0x0000 0FEC
GPIO1_GPIOPCELLID0	RO	32	0x0000 000D	0x0000 0FF0
GPIO1_GPIOPCELLID1	RO	32	0x0000 00F0	0x0000 0FF4
GPIO1_GPIOPCELLID2	RO	32	0x0000 0005	0x0000 0FF8
GPIO1_GPIOPCELLID3	RO	32	0x0000 00B1	0x0000 0FFC

Table 3.3 MCU General-Purpose Input/Output Controller 2 Register Map

Register Name	Type	Width	Reset Value	Address Offset
GPIO2_GPIODATA	RW	32	0x0000 0000	0x0000 0000-
GPIO2_GPIODIR	RW	32	0x0000 0000	0x0000 0400
GPIO2_GPIOIS	RW	32	0x0000 0000	0x0000 0404
GPIO2_GPIOIBE	RW	32	0x0000 0000	0x0000 0408
GPIO2_GPIOIEV	RW	32	0x0000 0000	0x0000 040C
GPIO2_GPIOIE	RW	32	0x0000 0000	0x0000 0410
GPIO2_GPIORIS	RO	32	0x0000 0000	0x0000 0414
GPIO2_GPIOMIS	RO	32	0x0000 0000	0x0000 0418
GPIO2_GPIOIC	RW	32	0x0000 0000	0x0000 041C
GPIO2_GPIOITCR	RW	32	0x0000 0000	0x0000 0600
GPIO2_GPIOITIP1	RW	32	0x0000 0000	0x0000 0604
GPIO2_GPIOITIP2	RW	32	0x0000 0000	0x0000 0608
GPIO2_GPIOITOP1	RW	32	0x0000 0000	0x0000 060C
GPIO2_GPIOITOP2	RO	32	0x0000 0000	0x0000 0610
GPIO2_GPIOITOP3	RW	32	0x0000 0000	0x0000 0614
GPIO2_GPIOPERIPHID0	RO	32	0x0000 0061	0x0000 0FE0
GPIO2_GPIOPERIPHID1	RO	32	0x0000 0010	0x0000 0FE4
GPIO2_GPIOPERIPHID2	RO	32	0x0000 0004	0x0000 0FE8
GPIO2_GPIOPERIPHID3	RO	32	0x0000 0000	0x0000 0FEC
GPIO2_GPIOPCELLID0	RO	32	0x0000 000D	0x0000 0FF0
GPIO2_GPIOPCELLID1	RO	32	0x0000 00F0	0x0000 0FF4
GPIO2_GPIOPCELLID2	RO	32	0x0000 0005	0x0000 0FF8
GPIO2_GPIOPCELLID3	RO	32	0x0000 00B1	0x0000 0FFC

Table 3.4 MCU General-Purpose Input/Output Controller 3 Register Map

Register Name	Type	Width	Reset Value	Address Offset
GPIO3_GPIODATA	RW	32	0x0000 0000	0x0000 0000-
GPIO3_GPIODIR	RW	32	0x0000 0000	0x0000 0400
GPIO3_GPIOIS	RW	32	0x0000 0000	0x0000 0404
GPIO3_GPIOIBE	RW	32	0x0000 0000	0x0000 0408
GPIO3_GPIOIEV	RW	32	0x0000 0000	0x0000 040C
GPIO3_GPIOIE	RW	32	0x0000 0000	0x0000 0410
GPIO3_GPIORIS	RO	32	0x0000 0000	0x0000 0414
GPIO3_GPIOMIS	RO	32	0x0000 0000	0x0000 0418
GPIO3_GPIOIC	RW	32	0x0000 0000	0x0000 041C
GPIO3_GPIOITCR	RW	32	0x0000 0000	0x0000 0600
GPIO3_GPIOITIP1	RW	32	0x0000 0000	0x0000 0604
GPIO3_GPIOITIP2	RW	32	0x0000 0000	0x0000 0608
GPIO3_GPIOITOP1	RW	32	0x0000 0000	0x0000 060C
GPIO3_GPIOITOP2	RO	32	0x0000 0000	0x0000 0610
GPIO3_GPIOITOP3	RW	32	0x0000 0000	0x0000 0614
GPIO3_GPIOPERIPHID0	RO	32	0x0000 0061	0x0000 0FE0
GPIO3_GPIOPERIPHID1	RO	32	0x0000 0010	0x0000 0FE4
GPIO3_GPIOPERIPHID2	RO	32	0x0000 0004	0x0000 0FE8
GPIO3_GPIOPERIPHID3	RO	32	0x0000 0000	0x0000 0FEC
GPIO3_GPIOPCELLID0	RO	32	0x0000 000D	0x0000 0FF0
GPIO3_GPIOPCELLID1	RO	32	0x0000 00F0	0x0000 0FF4
GPIO3_GPIOPCELLID2	RO	32	0x0000 0005	0x0000 0FF8
GPIO3_GPIOPCELLID3	RO	32	0x0000 00B1	0x0000 0FFC

4. Input and Output Signals

4.1. Function Signals and GPIO signals

The correspondence between the function signals and the GPIO signals is shown in Table 4.1.
The function signals are described in the section "5. Function".

Table 4.1 Correspondence Table

function signal name	GPIO signals	Description
PCLK	PCLK	bus clock
PRESETn	PRESETn	reset
PADDR	PADDR	APB signals
PENABLE	PENABLE	
PSEL	PSEL	
PWDATA	PWDATA	
PWRITE	PWRITE	
PRDATA	PRDATA	
GPIN	GPIN	GPIO Input
GPOUT	GPOUT	GPIO Output
nGPEN	nGPEN	GPIO direction control
nGPAFEN	nGPAFEN	not used
GPAFOUT	GPAFOUT	
GPAFIN	GPAFIN	
GIOMIS	GIOMIS	GPIO Interrupt
GIOINTR	GIOINTR	GPIO Interrupt (combined)

The connection to external pins is shown in Table 4.2.
The function of each GPIO pin can be changed by the pin share setting.

Table 4.2 External pin signals (1)

PIN name	direction	connect	Pin share	internal_connection signals (Block: signals)
MCU_GPIO_0	input	PIN	FMOD1	GPIO0: GPIN[0]
MCU_GPIO_1	In/out	PIN	FMOD1	GPIO0: GPIN[1]/GPOUT[1]/nGPEN[1]
MCU_GPIO_2	In/out	PIN	FMOD1	GPIO0: GPIN[2]/GPOUT[2]/nGPEN[2]
MCU_GPIO_3	In/out	PIN	FMOD1	GPIO0: GPIN[3]/GPOUT[3]/nGPEN[3]
MCU_GPIO_4	In/out	PIN	FMOD1	GPIO0: GPIN[4]/GPOUT[4]/nGPEN[4]
MCU_GPIO_5	In/out	PIN	FMOD1	GPIO0: GPIN[5]/GPOUT[5]/nGPEN[5]
MCU_GPIO_6	In/out	PIN	FMOD1	GPIO0: GPIN[6]/GPOUT[6]/nGPEN[6]
MCU_GPIO_7	In/out	PIN	FMOD1	GPIO0: GPIN[7]/GPOUT[7]/nGPEN[7]

Table 4.3 External pin signals (2)

PIN name	direction	connect	Pin share	internal_connection signals (Block: signals)
MCU_GPIO_8	In/out	PIN	FMOD1	GPIO1: GPIN[0]/GPOUT[0]/nGPEN[0]
MCU_GPIO_9	In/out	PIN	FMOD1	GPIO1: GPIN[1]/GPOUT[1]/nGPEN[1]
MCU_GPIO_10	In/out	PIN	FMOD1	GPIO1: GPIN[2]/GPOUT[2]/nGPEN[2]
MCU_GPIO_11	In/out	PIN	FMOD1	GPIO1: GPIN[3]/GPOUT[3]/nGPEN[3]
MCU_GPIO_12	In/out	PIN	FMOD1	GPIO1: GPIN[4]/GPOUT[4]/nGPEN[4]
MCU_GPIO_13	In/out	PIN	FMOD1	GPIO1: GPIN[5]/GPOUT[5]/nGPEN[5]
MCU_GPIO_14	In/out	PIN	FMOD1	GPIO1: GPIN[6]/GPOUT[6]/nGPEN[6]
MCU_GPIO_15	In/out	PIN	FMOD1	GPIO1: GPIN[7]/GPOUT[7]/nGPEN[7]
MCU_GPIO_24	In/out	PIN	FMOD1	GPIO3: GPIN[0]/GPOUT[0]/nGPEN[0]
MCU_GPIO_25	In/out	PIN	FMOD1	GPIO3: GPIN[1]/GPOUT[1]/nGPEN[1]
MCU_GPIO_26	In/out	PIN	FMOD1	GPIO3: GPIN[2]/GPOUT[2]/nGPEN[2]
MCU_GPIO_27	In/out	PIN	FMOD1	GPIO3: GPIN[3]/GPOUT[3]/nGPEN[3]
MCU_GPIO_28	In/out	PIN	FMOD1	GPIO3: GPIN[4]/GPOUT[4]/nGPEN[4]
MCU_GPIO_29	In/out	PIN	FMOD1	GPIO3: GPIN[5]/GPOUT[5]/nGPEN[5]
MCU_GPIO_30	In/out	PIN	FMOD1	GPIO3: GPIN[6]/GPOUT[6]/nGPEN[6]
MCU_GPIO_31	In/out	PIN	FMOD1	GPIO3: GPIN[7]/GPOUT[7]/nGPEN[7]
MCU_SPIM0_CS_N	In/out	PIN	FMOD2	GPIO2: GPIN[0]/GPOUT[0]/nGPEN[0]
MCU_SPIM0_CLK	In/out	PIN	FMOD2	GPIO2: GPIN[1]/GPOUT[1]/nGPEN[1]
MCU_SPIM0_MOSI	In/out	PIN	FMOD2	GPIO2: GPIN[2]/GPOUT[2]/nGPEN[2]
MCU_SPIM0_MISO	In/out	PIN	FMOD2	GPIO2: GPIN[3]/GPOUT[3]/nGPEN[3]
MCU_SPIM1_CS_N	In/out	PIN	FMOD2	GPIO2: GPIN[4]/GPOUT[4]/nGPEN[4]
MCU_SPIM1_CLK	In/out	PIN	FMOD2	GPIO2: GPIN[5]/GPOUT[5]/nGPEN[5]
MCU_SPIM1_MOSI	In/out	PIN	FMOD2	GPIO2: GPIN[6]/GPOUT[6]/nGPEN[6]
MCU_SPIM1_MISO	In/out	PIN	FMOD2	GPIO2: GPIN[7]/GPOUT[7]/nGPEN[7]
MCU_ADC24_SYNC	In/out	PIN	FMOD3	GPIO1: GPIN[0]/GPOUT[0]/nGPEN[0]
MCU_UA2_RTS_N	In/out	PIN	FMOD3	GPIO1: GPIN[2]/GPOUT[2]/nGPEN[2]
MCU_UA2_CTS_N	In/out	PIN	FMOD3	GPIO1: GPIN[3]/GPOUT[3]/nGPEN[3]
MCU_UA1_RXD	In/out	PIN	FMOD3	GPIO1: GPIN[4]/GPOUT[4]/nGPEN[4]
MCU_UA1_TXD	In/out	PIN	FMOD3	GPIO1: GPIN[5]/GPOUT[5]/nGPEN[5]
MCU_I2C1_DATA	In/out	PIN	FMOD3	GPIO1: GPIN[6]/GPOUT[6]/nGPEN[6]
MCU_I2C1_CLK	In/out	PIN	FMOD3	GPIO1: GPIN[7]/GPOUT[7]/nGPEN[7]
MCU_I2C0_DATA	In/out	PIN	FMOD3	GPIO2: GPIN[0]/GPOUT[0]/nGPEN[0]
MCU_I2C0_CLK	In/out	PIN	FMOD3	GPIO2: GPIN[1]/GPOUT[1]/nGPEN[1]
MCU_UA2_RXD	In/out	PIN	FMOD3	GPIO2: GPIN[2]/GPOUT[2]/nGPEN[2]
MCU_UA2_TXD	In/out	PIN	FMOD3	GPIO2: GPIN[3]/GPOUT[3]/nGPEN[3]
MCU_UA0_RXD	In/out	PIN	FMOD3	GPIO2: GPIN[4]/GPOUT[4]/nGPEN[4]
MCU_UA0_TXD	In/out	PIN	FMOD3	GPIO2: GPIN[5]/GPOUT[5]/nGPEN[5]
MCU_UA1_RTS_N	In/out	PIN	FMOD3	GPIO2: GPIN[6]/GPOUT[6]/nGPEN[6]
MCU_UA1_CTS_N	In/out	PIN	FMOD3	GPIO2: GPIN[7]/GPOUT[7]/nGPEN[7]

5. Function

The description in this section uses the function signal names. For the correspondence between the function signals and the GPIO signals, refer to Table 3.1.

5.1. GPIO Operation

5.1.1. Reset operation

PRESETn is driven to LOW.

- The interrupt of the specified pin is disabled by the clear of the corresponding bit in the *[GPIOn_GPIOIE]* register.
- All registers are cleared to 0.
- Input and output pins are set to input pins.
- All external interrupts are masked to be disabled.
- Interrupt causes are cleared.
- Edge trigger interrupt is selected.

Recommendation

When an interrupt is set to be generated with the edge trigger, the following initialization sequence should be done so that the system does not recognize a wrong interrupt.

- Set the *[GPIOn_GPIOIBE]* register properly to the edge trigger type among a rising edge, a falling edge, and both edges.
- When either a rising edge or a falling edge is selected, the *[GPIOn_GPIOIEV]* register should be set.
- Set the *[GPIOn_GPIOIS]* register to selecting an edge trigger path.
- Wait 3 clock cyclesto clear the interrupt pipeline.
- During these operation, **GPIN[7:0]** bus should be stable.
- Write FF to the *[GPIOn_GPIOIC]* register to clear all interrupts.
- Set the *[GPIOn_GPIOIE]* register so that the intrrupt is enabled.

5.1.2. Input and output operations

The GPIO module consists of 8 programmable input and output pins. When the software control mode is enabled, the data and the data direction of these pins are controlled by a data register and a data direction register, respectively. When reading the data register, each read data has the status of either the input or the output of the corresponding GPIO pin. The write data to the data register are valid only to the pins which are set to the output.

5.1.2.1. Data register

When software driver sets a bit of the GPIO without disturbing the other bits at a data write to the data register, the address bus is used as the mask of the read or write operation. The data register occupies 256 word addresses in the address space. 8 address signals **PADDR[9:2]** are used to access the data register. At a write to the data register, if the address bit corresponding to the data bit is HIGH, the *[GPIOn_GPIODATA]* register value is changed. If the address bit is LOW, the register value is not changed.

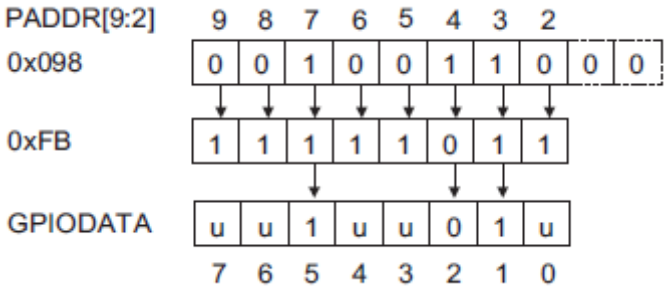
Example:

[GPIOn_GPIODATA] + address 0x098 (= 0b000010011000) write

When the register whose address is PADDR[9:2] = 0b00100110 (the address 0x098) is written to 0xFB, the followings occur.

- The bit 5 and bit 1 of the GPIO pin are set to 1. The bit 2 of that is set to 0.
- The other bits are unchanged.

Figure 5.1 shows how the address value 0x098 affects the data value 0xFB.



Note: "u" indicates that the bit value is unchanged.

Figure 5.1 Example of write of address 0x098 to data 0xFB

At a read from GPIO pins, if the address bit corresponding to the data bit is HIGH, the pin value is read. If the address bit is LOW, the read value becomes 0.

Example:

[GPIOn_GPIODATA] + address 0x0C4 (= 0b000011000100)

When the pins whose address is **PADDR[9:2]** = 0b00110001 (address 0x0C4) is read, the followings occur.

- Bits 5, 4, and 0 of the GPIO pins are read.
- Bits 7, 6, 3, 2, and 1 become 0.

Figure 5.2 shows the read from the address 0x0C4 and the PRDATA[7:0] values.

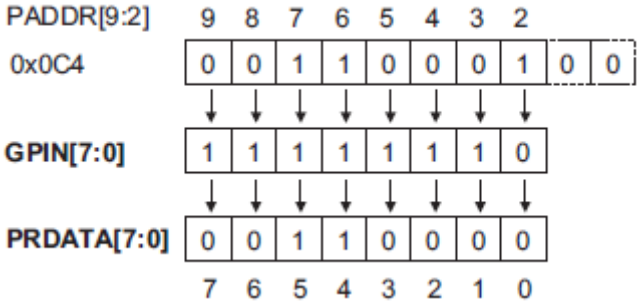


Figure 5.2 Example of read of data 0xFB from address 0x0C4

5.1.2.2. Data direction register

The operation of the data direction register is as follows.

- 0 defines that the corresponding pin is the input.
- 1 defines that the corresponding pin is the output.

The typical write timing is shown in Figure 5.3.

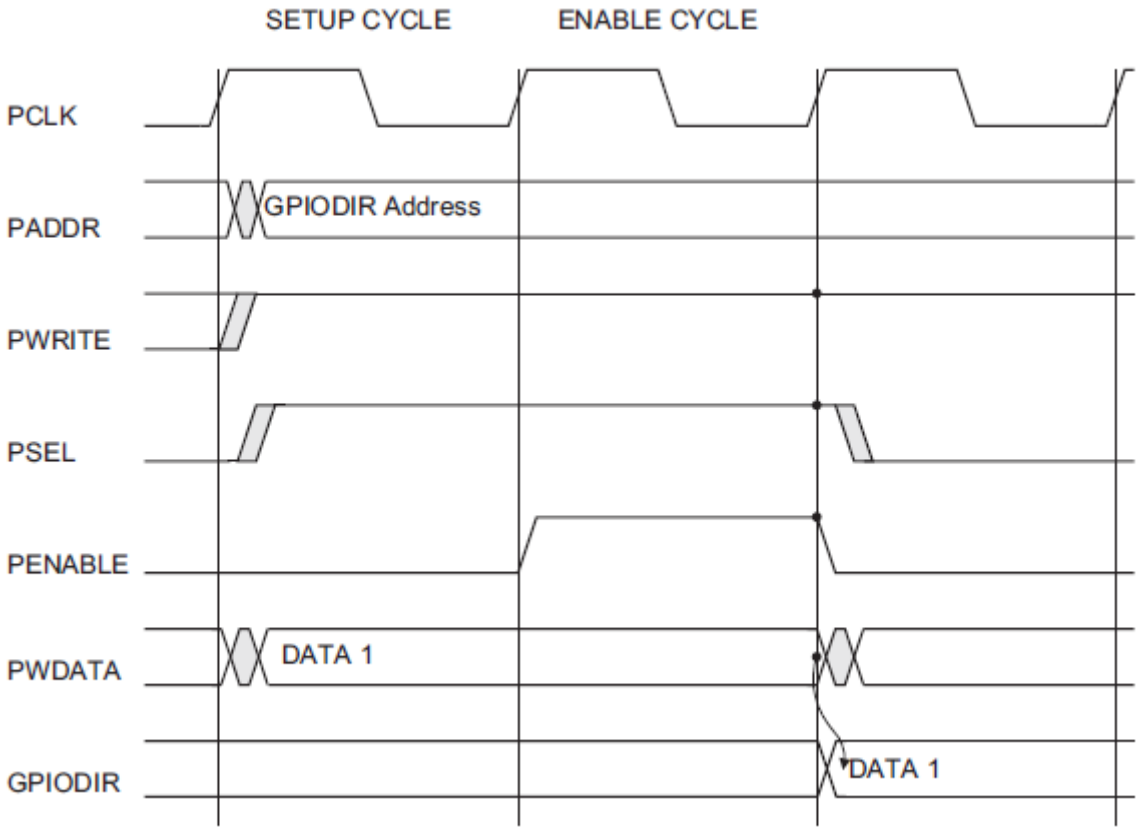


Figure 5.3 Write timing of data direction register

5.1.3. Interrupt

The interrupt operation of the GPIO is controlled by 7 registers. The source of an interrupt, the input polarity, and the edge property can be selected. When one or more GPIO pins generate interrupts, either a single **GPIOINTR** or the GPIO interrupts are transferred to the interrupt controller. If an edge trigger interrupt is set, software should clear it to enable another interrupt. In the level trigger interrupt, the external source has the level information which the processor recognizes as an interrupt.

The following 3 registers are necessary to define the source of an interrupt to either an edge or a level trigger.

- *[GPIOn_GPIOIS]*
- *[GPIOn_GPIOIBE]*
- *[GPIOn_GPIOIEV]*

Figure 5.4 shows the flowchart to select a source trigger of an interrupt using the 3 registers.

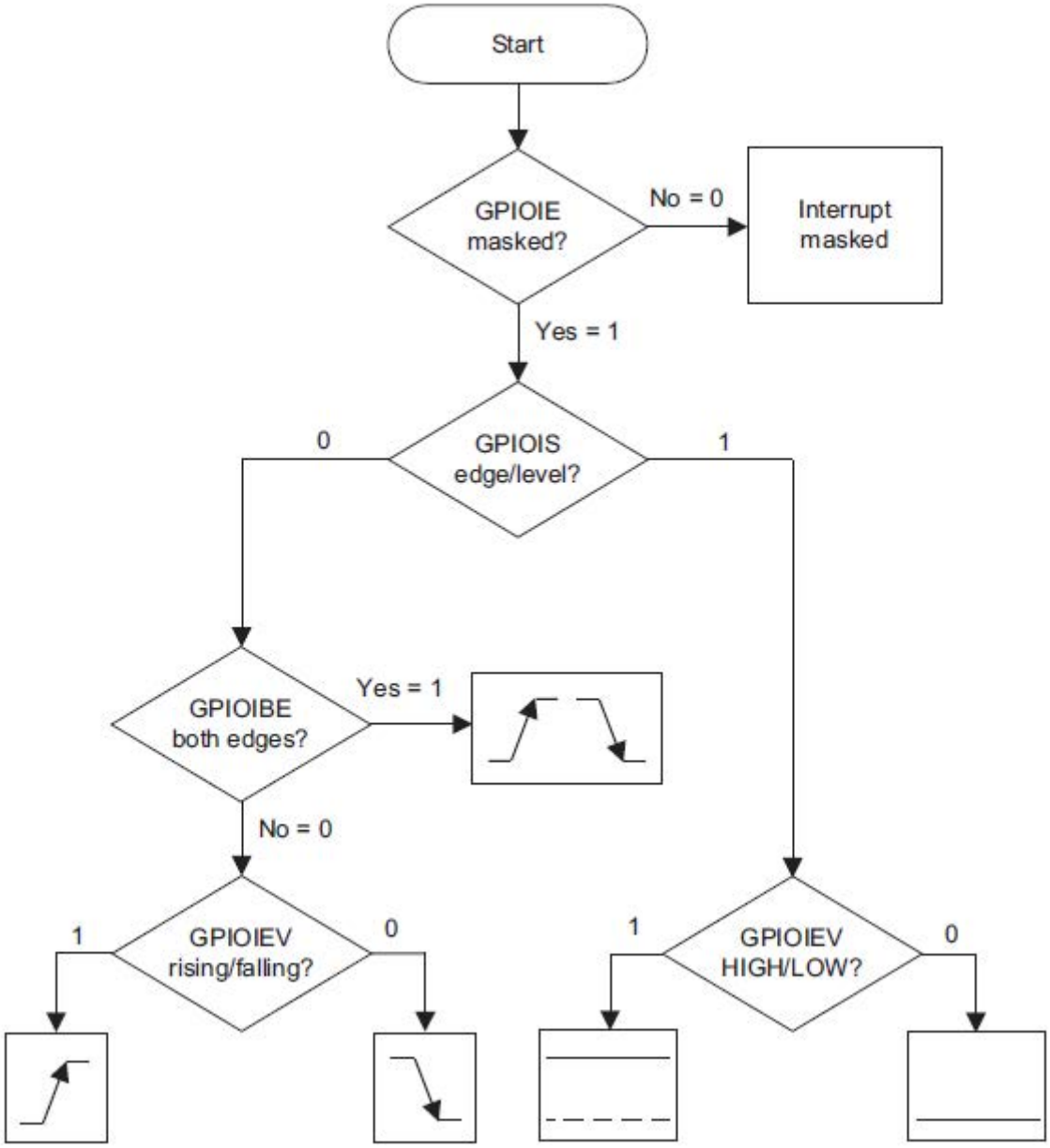


Figure 5.4 GPIO interrupt registers

5.1.3.1. Register Program

Table 5.1 Interrupt trigger of pin 2 shows the setting of the rising edge trigger for the interrupt of the bit 2 of the input pin.

Table 5.1 Interrupt trigger of pin 2

Register	Desired trigger	7	6	5	4	3	2	1	0
GPIOIS	0 = edge 1 = level	x	x	x	x	x	0	x	x
GPIOIBE	0 = single edge 1 = both edges	x	x	x	x	x	0	x	x
GPIOIEV	LOW level, or negative edge HIGH level, or positive edge	x	x	x	x	x	1	x	x
GPIOIE	0 = masked 1 = not masked	0	0	0	0	0	1	0	0

The data 0 in any bit of the *[GPIOn_GPIOIE]* register disables the trigger of the corresponding interrupt.

In Table 5.1, x means that the data has no relations with the bit 2 and is masked by the *[GPIOn_GPIOIE]* register. When an interrupt is not enabled, the interrupt control register should be set. When the interrupt control register is written, an interrupt can be generated if the corresponding bit is enables.

5.2. Power Management

The power modes of the TZ1000 Series are shown in Table 5.2.

Table 5.2 Power mode and operation

Power mode	State of GPIO0/1/2/3
ACTIVE	Run (*1)
SLEEP0	Run (*1)
SLEEP1	Run (*1)
SLEEP2	Clock gating
WAIT	Clock gating
RETENTION	Retention
RTC	Power Down
STOP	Power Down

(*1) The clock can be started or stopped by software.

- ACTIVE/SLEEP0/SLEEP1:
  Normal operation.
  When the clock stop is set by software, the input or output operation and the edge trigger interrupt operation stop, and every signal holds its own data. So, if an interrupt is asserted, it cannot be deasserted because of no clock operation. To prevent that, the clock should be stopped after the interrupt disable (***[GPIOn_GPIOIE]***.IE[m] = 0) is set for PIN m of edge interrupt setting.

GPIO register	Bit name	value	Condition
[GPIOn_GPIOIE]	IE[m]	0b0	***[GPIOn_GPIOIS]***.IS[m]==0b0

(n is a channel number: 0, 1, 2, or 3.)
(m is a PIN number: 0, 1, 2, 3, 4, 5, 6, or 7.)

When the clock start is set, the transfer re-starts with the same state where the clock stopped. For the level trigger interrupt, the interrupt request reaches the CPU and the interrupt can be generated.

- SLEEP2/WAIT/ RETENTION:
  PCLK stops, so the input or output operation and the edge trigger interrupt operation cannot be used. The PMU can, however, receive an interrupt because the GPIO is controlled by the PMU. If the interrupt is asserted, it will not be able to be deasserted. It is necessary to set the disable to them (***[GPIOn_GPIOIE]***.IE = 0x00) before the clock stop.

GPIO register	Bit name	value	Condition
[GPIOn_GPIOIE]	IE	0x00	—

(n is a channel number: 0, 1, 2, or 3.)

When returning from this mode, every signal is restored to the data in the previous mode.

- RTC/STOP:
  Before the transition to this mode, it should be checked that the following settings are done to disable the corresponding function.
  - All IE bits in the ***[GPIOn_GPIOIE]*** register are 0.
  - The return procedure is set in an appropriate register in the PMU.
    (n is a channel number: 0, 1, 2, or 3.)

  When returning from this mode, the registers are initialized. So, the operation should re-start after the configuration of the registers completes.

5.3. Start-up and Stop Procedure

5.3.1. Start-up procedure

The start-up procedure after power-on is as follows.

For detail of the PMU (Power Management Unit) registers, refer to the PMU section.

The following settings are supposed that the main bus (the bus connected to the CPU) and the GCONF are supplied with clocks.

Each GPIO will be supplied with a clock by this setting.

("*" shows the signal which also controls another function. The setting should be done together with another setting.)

The order of the setting procedure is a frequency setting at first, then clock supply, and reset deassertion at last.

- GPIO clock frequency setting

PMU register	Bit name	Description
[CSM_MAIN]	CSMSEL_MAIN	0x0000000u u: 0x0: SiOSC4M, 0x1: OSC12M, 0x2: PLL, 0x3: ADPLL, 0x4: OSC32K/SIOSC32K 0x5-0x7: reserved
[PRESCAL_MAIN]	PSSEL_CD_PPIER0	0x****u*** u: 0x0: not generate clock 0x1: divided by 1, 0x2: divided by 2, 0x3: divided by 3, 0x4: divided by 4, 0x5: divided by 5, 0x6: divided by 6, 0x7: divided by 7, 0x8: divided by 8, 0x9: divided by 9, 0xA: divided by 10, 0xB: divided by 12, 0xC: divided by 18, 0xD: divided by 24, 0xE: divided by 36, 0xF: divided by 48

Note: ***[CSM_MAIN]*** sets the source of the clock. The PLL is set by another register and the frequency is changed by the setting. (For detail, refer to the PMU section.)

Note: ***[PRESCAL_MAIN]*** has a setting to another power domain.

Note: PSSEL_CD_PPIER0 setting specifies all circuits in the PPIER0 power domain.

The start-up sequence of the GPIO0 is as follows.

Setting of the external shared pins at first, then release of the standby for the external pins, Clock supply, and deassertion of the reset at last.

- Setting of the external shared pins of the GPIO0
  It is necessary that the GCONF should configure the shared pins to input or output data. (For detail, refer to the GCONF section.)

- Standby mode release of the external pins in the GPIO0
  When the external pins are used, it is necessary to release the standby mode of the pins. (For detail, refer to the PMU section.)

- GPIO0 clock supply

PMU register	Bit name	value
[CG_OFF_POWERDOMAIN]	CG_PM	0x00000001
[CG_OFF_PM_2]	CG_ppier0clk_gpio0_pclk	0x00000010

Note: Bit 4 in the *[CG_OFF_PM_2]* register corresponds to the GPIO0.

- Reset deassertion of the GPIO0

PMU register	Bit name	value
[SRST_OFF_POWERDOMAIN]	SRST_PM	0x00000001
[SRST_OFF_PM_2]	SRST_asyncrst_gpio0_prstn	0x00000010

Note: Bit 4 in the *[SRST_OFF_PM_2]* register corresponds to the GPIO0.

The start-up sequence of the GPIO1 is as follows.

Setting of the external shared pins at first, then release of the standby for the external pins, Clock supply, and deassertion of the reset at last.

- Setting of the external shared pins of the GPIO1
  It is necessary that the GCONF should configure the shared pins to input or output data. (For detail, refer to the GCONF section.)

- Standby mode release of the external pins in the GPIO1
  When the external pins are used, it is necessary to release the standby mode of the pins. (For detail, refer to the PMU section.)

- GPIO1 clock supply

PMU register	Bit name	value
[CG_OFF_POWERDOMAIN]	CG_PM	0x00000001
[CG_OFF_PM_2]	CG_ppier0clk_gpio1_pclk	0x00000020

Note: Bit 5 in the *[CG_OFF_PM_2]* register corresponds to the GPIO1.

- Reset deassertion of the GPIO1

PMU register	Bit name	value
[SRST_OFF_POWERDOMAIN]	SRST_PM	0x00000001
[SRST_OFF_PM_2]	SRST_asyncrst_gpio1_prstn	0x00000020

Note: Bit 5 in the *[SRST_OFF_PM_2]* register corresponds to the GPIO1.

The start-up sequence of the GPIO2 is as follows.

Setting of the external shared pins at first, then release of the standby for the external pins, Clock supply, and deassertion of the reset at last.

- Setting of the external shared pins of the GPIO2
  It is necessary that the GCONF should configure the shared pins to input or output data. (For detail, refer to the GCONF section.)

- Standby mode release of the external pins in the GPIO2
  When the external pins are used, it is necessary to release the standby mode of the pins. (For detail, refer to the PMU section.)

- GPIO2 clock supply

PMU register	Bit name	value
[CG_OFF_POWERDOMAIN]	CG_PM	0x00000001
[CG_OFF_PM_2]	CG_ppier0clk_gpio2_pclk	0x00000040

Note: Bit 6 in the *[CG_OFF_PM_2]* register corresponds to the GPIO2.

- Reset deassertion of the GPIO2

PMU register	Bit name	value
[SRST_OFF_POWERDOMAIN]	SRST_PM	0x00000001
[SRST_OFF_PM_2]	SRST_asyncrst_gpio2_prstn	0x00000040

Note: Bit 6 in the *[SRST_OFF_PM_2]* register corresponds to the GPIO2.

The start-up sequence of the GPIO3 is as follows.

Setting of the external shared pins at first, then release of the standby for the external pins, Clock supply, and deassertion of the reset at last.

- Setting of the external shared pins of the GPIO3
  It is necessary that the GCONF should configure the shared pins to input or output data. (For detail, refer to the GCONF section.)

- Standby mode release of the external pins in the GPIO3
  When the external pins are used, it is necessary to release the standby mode of the pins. (For detail, refer to the PMU section.)

- GPIO3 clock supply

PMU register	Bit name	value
[CG_OFF_POWERDOMAIN]	CG_PM	0x00000001
[CG_OFF_PM_2]	CG_ppier0clk_gpio3_pclk	0x00000080

Note: Bit 7 in the *[CG_OFF_PM_2]* register corresponds to the GPIO3.

- Reset deassertion of the GPIO3

PMU register	Bit name	value
[SRST_OFF_POWERDOMAIN]	SRST_PM	0x00000001
[SRST_OFF_PM_2]	SRST_asyncrst_gpio3_prstn	0x00000080

Note: Bit 7 in the *[SRST_OFF_PM_2]* register corresponds to the GPIO3.

- GPIO setting
  - After deasserting the reset, the GPIO becomes the input.
    The input or output operation is set by writing the following register.

  - The data direction, the output data and others are set to the *[GPIOn_GPIODIR]*, and *[GPIOn_GPIODATA]* registers.
    (n is a channel number: 0, 1, 2, and 3.)

5.3.2. Stop procedure

- In case that the GPIO is not used (the whole block stops):
  The following two ways are used.
  - No reset assertion:
    Only the clock supply is stopped by the following PMU register setting.
  - Reset assertion:
    The reset assertion and the clock stop are set by the following PMU register.

- GPIO0 reset

PMU register	Bit name	value
[SRST_ON_PM_2]	SRST_asyncrst_gpio0_prstn	0x000000010

Note: Bit 4 in the *[SRST_ON_PM_2]* register corresponds to the GPIO0.

- GPIO1 reset

PMU register	Bit name	value
[SRST_ON_PM_2]	SRST_asyncrst_gpio1_prstn	0x000000020

Note: Bit 5 in the *[SRST_ON_PM_2]* register corresponds to the GPIO1.

- GPIO2 reset

PMU register	Bit name	value
[SRST_ON_PM_2]	SRST_asyncrst_gpio2_prstn	0x000000040

Note: Bit 6 in the *[SRST_ON_PM_2]* register corresponds to the GPIO2.

- GPIO3 reset

PMU register	Bit name	value
[SRST_ON_PM_2]	SRST_asyncrst_gpio3_prstn	0x000000080

Note: Bit 7 in the *[SRST_ON_PM_2]* register corresponds to the GPIO3.

- GPIO0 clock supply stop

PMU register	Bit name	value
[CG_ON_PM_2]	CG_ppier0clk_gpio0_pclk	0x000000010

Note: Bit 4 in the *[CG_ON_PM_2]* register corresponds to the GPIO0.

- GPIO1 clock supply stop

PMU register	Bit name	value
[CG_ON_PM_2]	CG_ppier0clk_gpio1_pclk	0x000000020

Note: Bit 5 in the *[CG_ON_PM_2]* register corresponds to the GPIO1.

- GPIO2 clock supply stop

PMU register	Bit name	value
[CG_ON_PM_2]	CG_ppier0clk_gpio2_pclk	0x000000040

Note: Bit 6 in the *[CG_ON_PM_2]* register corresponds to the GPIO2.

- GPIO3 clock supply stop

PMU register	Bit name	value
[CG_ON_PM_2]	CG_ppier0clk_gpio3_pclk	0x000000080

Note: Bit 7 in the *[CG_ON_PM_2]* register corresponds to the GPIO3.

5.4. Dynamic Clock Gating Setting Procedure

The TZ1000 Series can be set to stop the clock supply unless the clock is necessary. When it is set, the following operation reduces power dissipation.

("*" shows the signal which also controls another function. The setting should be done together with another setting.)

- Clock supply only when the bus access to the GPIO.
  (Only when the GPIOIS register is set to 0x000000ff, the dynamic clock gating is applied. Otherwise, the clock is always supplied.)

- GPIO0 dynamic clock gating setting

PMU register	Bit name	value
[DCG_POWERDOMAIN]	DCG_PM	0x*******1
[DCG_PM_1]	DCG_ppier0clk_h2pp0_hclk	0x*******3
	DCG_mpierclk_h2hp0_hclk	
[DCG_PM_2]	DCG_ppier0clk_gpio0_pclk	0x******1*

Note: Bit 4 in the ***[DCG_ON_PM_2]*** register corresponds to the GPIO0.

- GPIO1 dynamic clock gating setting

PMU register	Bit name	value
[DCG_POWERDOMAIN]	DCG_PM	0x*******1
[DCG_PM_1]	DCG_ppier0clk_h2pp0_hclk	0x*******3
	DCG_mpierclk_h2hp0_hclk	
[DCG_PM_2]	DCG_ppier0clk_gpio1_pclk	0x******2*

Note: Bit 5 in the ***[DCG_ON_PM_2]*** register corresponds to the GPIO1.

- GPIO2 dynamic clock gating setting

PMU register	Bit name	value
[DCG_POWERDOMAIN]	DCG_PM	0x*******1
[DCG_PM_1]	DCG_ppier0clk_h2pp0_hclk	0x*******3
	DCG_mpierclk_h2hp0_hclk	
[DCG_PM_2]	DCG_ppier0clk_gpio2_pclk	0x******4*

Note: Bit 6 in the ***[DCG_ON_PM_2]*** register corresponds to the GPIO2.

- GPIO3 dynamic clock gating setting

PMU register	Bit name	value
[DCG_POWERDOMAIN]	DCG_PM	0x*******1
[DCG_PM_1]	DCG_ppier0clk_h2pp0_hclk	0x*******3
	DCG_mpierclk_h2hp0_hclk	
[DCG_PM_2]	DCG_ppier0clk_gpio3_pclk	0x******8*

Note: Bit 7 in the ***[DCG_ON_PM_2]*** register corresponds to the GPIO3.

The setting of the dynamic clock gating can be cleared by writing 0 to the corresponding bit.

- GPIO0 dynamic clock gating deassertion (GPIO0 only)

PMU register	Bit name	value
[DCG_PM_2]	DCG_ppier0clk_gpio0_pclk	0x******0*

Note: Bit 4 in the *[DCG_ON_PM_2]* register corresponds to the GPIO0.

- GPIO1 dynamic clock gating deassertion (GPIO1 only)

PMU register	Bit name	value
[DCG_PM_2]	DCG_ppier0clk_gpio1_pclk	0x******0*

Note: Bit 5 in the *[DCG_ON_PM_2]* register corresponds to the GPIO1.

- GPIO2 dynamic clock gating deassertion (GPIO2 only)

PMU register	Bit name	value
[DCG_PM_2]	DCG_ppier0clk_gpio2_pclk	0x******0*

Note: Bit 6 in the *[DCG_ON_PM_2]* register corresponds to the GPIO2.

- GPIO3 dynamic clock gating deassertion (GPIO3 only)

PMU register	Bit name	value
[DCG_PM_2]	DCG_ppier0clk_gpio3_pclk	0x******0*

Note: Bit 7 in the *[DCG_ON_PM_2]* register corresponds to the GPIO3.

6. Precaution for Usage

6.1. Access Restriction Associated with Register Access

The registers in this module are assigned to a 4 KB space with 32-bit interval in the little endian format. The bit locations are as follows.

This module is connected to the main data bus (the bus connected to the CPU) with 32-bit wide. When 8-bit or 16-bit data is accessed, the operation is in units of 32-bit only. The GPIO register is assigned to the 8 bits in the lower address 0. This means that the write to the other location (for example, the 8 bits in the lower address) causes the wrong write to the register. So, 32-bit access is recommended. Otherwise, a read error or a write error may occur.

The write to a non-existing bit in a register is ignored. The read of the bit returns 0.

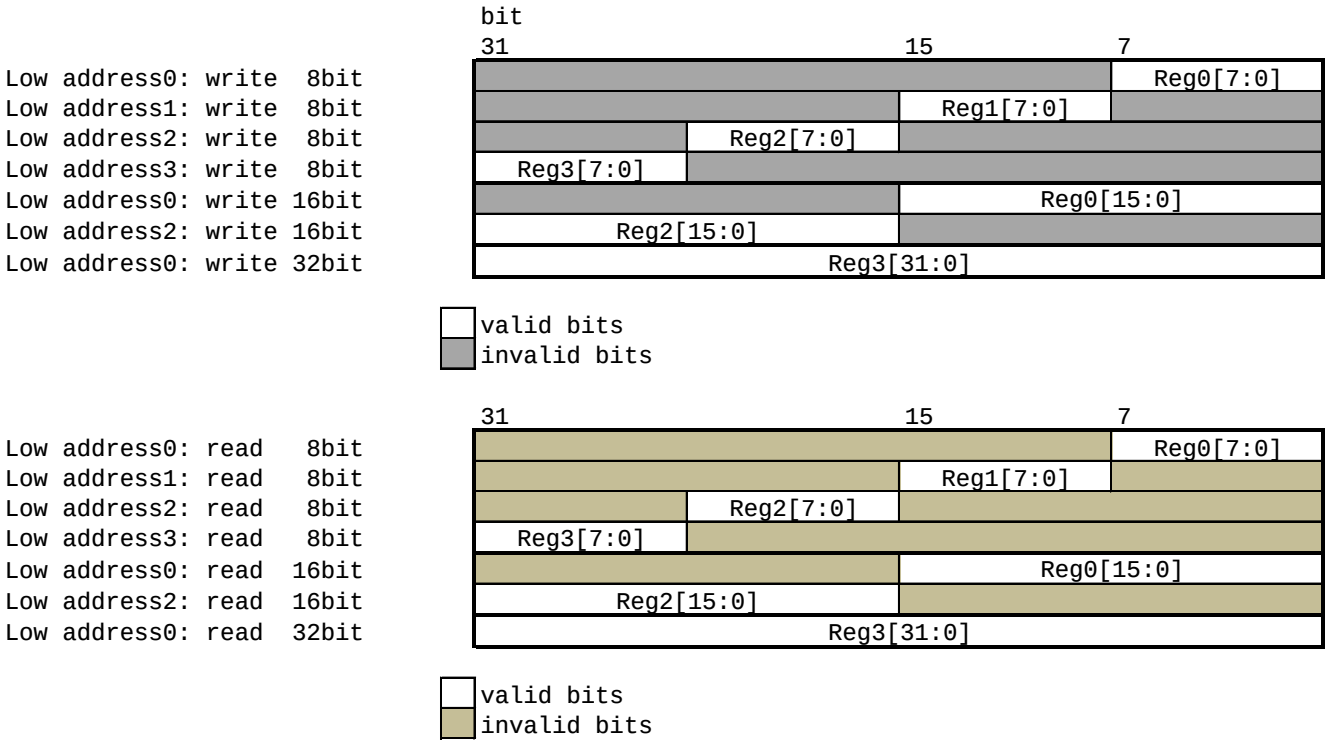


Figure 6.1 Bit allocation of register access

7. Details of MCU General-Purpose Input/Output Controller 0 Registers

7.1. GPIO0_GPIODATA

GPIO0_GPIODATA					
Description	GPIO Data Register				
Address Region	gpio0		**Type:**	RW	
Offset	0x0000 0000-				
Physical address View0	0x4004 B000- 0x4004 B3FC				
Physical address View1	-				
Bitfield Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:8	Reserved	-		-	-
7:0	DATA	At reading: The logical product of the address to be accessed and terminal status can be read. PADDR[9:2] & GPIN[7:0] At writing: The logical product of the address to be accessed and written data and GPIO output settings is set for the terminal. PADDR[9:2] & PWDATA[7:0] & [GPIO0_GPIODIR].DIR[7:0]		RW modify	0x00

7.2. GPIO0_GPIODIR

GPIO0_GPIODIR					
Description	GPIO Data Direction Register				
Address Region	gpio0		**Type:**	RW	
Offset	0x0000 0400				
Physical address View0	0x4004 B400				
Physical address View1	-				
Bitfield Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:8	Reserved	-		-	-
7:0	DIR	Sets the data direction of each GPIO pin. 0b1: GPIO output 0b0: GPIO input		RW modify	0x00

7.3. GPIO0_GPIOIS

GPIO0_GPIOIS					
Description	GPIO Interrupt Sense Register				
Address Region	gpio0		**Type:**	RW	
Offset	0x0000 0404				
Physical address View0	0x4004 B404				
Physical address View1	-				
Bitfield Details					
Bits	**Name**	**Description**		**Access**	**Reset**

31:8	Reserved	-	-	-
7:0	IS	Sets the interrupt detection method of each GPIO pin. GPIOIEV specifies other settings. 0b1: Level detection interrupt 0b0: Edge detection interrupt	RW modify	0x00

7.4. GPIO0_GPIOIBE

GPIO0_GPIOIBE			
Description	GPIO Interrupt Both Edges Register		
Address Region	gpio0	**Type:**	RW
Offset	0x0000 0408		
Physical address View0	0x4004 B408		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	IBE	Sets both-edge interrupt of each GPIO pin. GPIOIEV determines the edge to be used. 0b1: Both-edge interrupt 0b0: Single edge interrupt	RW modify	0x00

7.5. GPIO0_GPIOIEV

GPIO0_GPIOIEV			
Description	GPIO Interrupt Event Register		
Address Region	gpio0	**Type:**	RW
Offset	0x0000 040C		
Physical address View0	0x4004 B40C		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	IEV	Sets the edge interrupt method of each GPIO pin. 0b1: Rising edge interrupt or High-level interrupt 0b0: Falling edge interrupt or low-level interrupt	RW modify	0x00

7.6. GPIO0_GPIOIE

GPIO0_GPIOIE			
Description	GPIO Interrupt Enable Register		
Address Region	gpio0	**Type:**	RW
Offset	0x0000 0410		
Physical address View0	0x4004 B410		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	IE	Sets interrupt enable/mask for each GPIO pin. 0b1: Does not mask the interrupt (interrupt enable) 0b0: Masks the interrupt (interrupt disable)	RW modify	0x00

7.7. GPIO0_GPIORIS

GPIO0_GPIORIS			
Description	GPIO Raw Interrupt Status Register		
Address Region	gpio0	**Type:**	RO
Offset	0x0000 0414		
Physical address View0	0x4004 B414		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	RIS	Interrupt status before masking for each GPIO pin 0b1: Interrupt request available 0b0: No interrupt request	RO	0x00

7.8. GPIO0_GPIOMIS

GPIO0_GPIOMIS			
Description	GPIO Masked Interrupt Status Register		
Address Region	gpio0	**Type:**	RO
Offset	0x0000 0418		
Physical address View0	0x4004 B418		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	MIS	Interrupt status after masking for each GPIO pin 0b1: Interrupt request available 0b0: No interrupt request	RO	0x00

7.9. GPIO0_GPIOIC

GPIO0_GPIOIC				
Description	GPIO Interrupt Clear Register			
Address Region	gpio0	**Type:**	RW	
Offset	0x0000 041C			
Physical address View0	0x4004 B41C			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	IC	Clears an interrupt for each GPIO pin. 0b1: Clears the interrupt. 0b0: Does nothing.	RW oneToClear	0x00

7.10. GPIO0_GPIOITCR

GPIO0_GPIOITCR				
Description	GPIO Integration Test Control Register			
Address Region	gpio0	**Type:**	RW	
Offset	0x0000 0600			
Physical address View0	0x4004 B600			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	ITEN	Integration test enable 0b1: Test mode 0b0: Normal operation	RW modify	0

7.11. GPIO0_GPIOITIP1

GPIO0_GPIOITIP1				
Description	GPIO Integration test input read/set Register 1			
Address Region	gpio0	**Type:**	RW	
Offset	0x0000 0604			
Physical address View0	0x4004 B604			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	GPAFOUT	For ITEM=1(Integration test mode), enables the GPAFOUT input signal to be controlled. At reading: Reads the output status of Mux at the GPAFOUT last stage. At writing: Enables alternate data to be written for GPAFOUT input. For ITEM=0(Normal mod), the GPAFOUT input status can be read intact. No operation for writing.	RW modify	0x00

7.12. GPIO0_GPIOITIP2

GPIO0_GPIOITIP2					
Description	GPIO Integration test input read/set Register 2				
Address Region	gpio0		**Type:**	RW	
Offset	0x0000 0608				
Physical address View0	0x4004 B608				
Physical address View1	-				
Bitfield Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:8	Reserved	-		-	-
7:0	nGPAFEN	For ITEM=1(Integration test mode), enables the nGPAFEN input signal to be controlled. At reading: Reads the output status of Mux at the nGPAFEN last stage. At writing: Enables alternate data to be written for nGPAFEN input. For ITEM=0(Normal mod), the nGPAFEN input status can be read intact. No operation for writing.		RW modify	0x00

7.13. GPIO0_GPIOITOP1

GPIO0_GPIOITOP1					
Description	GPIO Integration test output read/set Register 1				
Address Region	gpio0		**Type:**	RW	
Offset	0x0000 060C				
Physical address View0	0x4004 B60C				
Physical address View1	-				
Bitfield Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:8	Reserved	-		-	-
7:0	GPIOMIS	For ITEM=1(Integration test mode), enables the GPIOMIS output signal to be controlled. At reading: Returns 0. At writing: Writes data to be output to GPIOMIS. For ITEM=0(Normal mod), no operation for writing.		RW modify	0x00

7.14. GPIO0_GPIOITOP2

GPIO0_GPIOITOP2				
Description	GPIO Integration test output read/set Register 2			
Address Region	gpio0	**Type:**	RO	
Offset	0x0000 0610			
Physical address View0	0x4004 B610			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	GPIOINTR	For ITEM=1(Integration test mode), enables the status of the GPIOINTR output signal to be read. At reading: Reads the GPIOINTR status (GPIOINTR is a signal with GPIOMIS[7:0] being ORed).	RO	0

7.15. GPIO0_GPIOITOP3

GPIO0_GPIOITOP3				
Description	GPIO Integration test output read/set Register 3			
Address Region	gpio0	**Type:**	RW	
Offset	0x0000 0614			
Physical address View0	0x4004 B614			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	GPAFIN	For ITEM=1(Integration test mode), enables the GPIOAFIN output signal to be controlled. At reading: Reads the output status of Mux at the GPAFIN last stage. AT writing: Writes data to be output to GPAFIN. For ITEM=0(Normal mod), the GPAFIN output status can be read intact. No operation for writing.	RW modify	0x00

7.16. GPIO0_GPIOPERIPHID0

GPIO0_GPIOPERIPHID0					
Description	GPIO Peripheral ID0 Register				
Address Region	gpio0		**Type:**	RO	
Offset	0x0000 0FE0				
Physical address View0	0x4004 BFE0				
Physical address View1	-				
Bitfield Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:8	Reserved	-		-	-
7:0	Partnumber0	Peripheral ID (this register stores a value from a hardware viewpoint.) Partnumber(Lower) 061=>61		RO	0x61

7.17. GPIO0_GPIOPERIPHID1

GPIO0_GPIOPERIPHID1					
Description	GPIO Peripheral ID1 Register				
Address Region	gpio0		**Type:**	RO	
Offset	0x0000 0FE4				
Physical address View0	0x4004 BFE4				
Physical address View1	-				
Bitfield Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:8	Reserved	-		-	-
7:4	Designer0	Peripheral ID (this register stores a value from a hardware viewpoint.) Designer(Lower) 41=>1		RO	0x1
3:0	Partnumber1	Peripheral ID (this register stores a value from a hardware viewpoint.) Partnumber(Upper) 061=>0		RO	0x0

7.18. GPIO0_GPIOPERIPHID2

GPIO0_GPIOPERIPHID2					
Description	GPIO Peripheral ID2 Register				
Address Region	gpio0		**Type:**	RO	
Offset	0x0000 0FE8				
Physical address View0	0x4004 BFE8				
Physical address View1	-				
Bitfield Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:8	Reserved	-		-	-
7:4	Revision	Peripheral ID (this register stores a value from a hardware viewpoint.) Revision: r1p0=>0		RO	0x0
3:0	Designer1	Peripheral ID (this register stores a value from a hardware viewpoint.) Designer(Upper) 41=>4		RO	0x4

7.19. GPIO0_GPIOPERIPHID3

GPIO0_GPIOPERIPHID3			
Description	GPIO Peripheral ID3 Register		
Address Region	gpio0	**Type:**	RO
Offset	0x0000 0FEC		
Physical address View0	0x4004 BFEC		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:8	Reserved	-	-	-
7:0	Configuration	Peripheral ID (this register stores a value from a hardware viewpoint.) Configuration: 00	RO	0x00

7.20. GPIO0_GPIOPCELLID0

GPIO0_GPIOPCELLID0			
Description	GPIO PrimeCell ID0 Register		
Address Region	gpio0	**Type:**	RO
Offset	0x0000 0FF0		
Physical address View0	0x4004 BFF0		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:8	Reserved	-	-	-
7:0	PCellID0	PrimeCell ID (this register stores a value from a hardware viewpoint). Fixed value.	RO	0x0D

7.21. GPIO0_GPIOPCELLID1

GPIO0_GPIOPCELLID1			
Description	GPIO PrimeCell ID1 Register		
Address Region	gpio0	**Type:**	RO
Offset	0x0000 0FF4		
Physical address View0	0x4004 BFF4		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:8	Reserved	-	-	-
7:0	PCellID1	PrimeCell ID (this register stores a value from a hardware viewpoint). Fixed value.	RO	0xF0

7.22. GPIO0_GPIOPCELLID2

GPIO0_GPIOPCELLID2			
Description	GPIO PrimeCell ID2 Register		
Address Region	gpio0	**Type:**	RO
Offset	0x0000 0FF8		
Physical address View0	0x4004 BFF8		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	PCellID2	PrimeCell ID (this register stores a value from a hardware viewpoint). Fixed value.	RO	0x05

7.23. GPIO0_GPIOPCELLID3

GPIO0_GPIOPCELLID3			
Description	GPIO PrimeCell ID3 Register		
Address Region	gpio0	**Type:**	RO
Offset	0x0000 0FFC		
Physical address View0	0x4004 BFFC		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	PCellID3	PrimeCell ID (this register stores a value from a hardware viewpoint). Fixed value.	RO	0xB1

8. Details of MCU General-Purpose Input/Output Controller 1 Registers

8.1. GPIO1_GPIODATA

GPIO1_GPIODATA					
Description	GPIO Data Register				
Address Region	gpio1		**Type:**	RW	
Offset	0x0000 0000-				
Physical address View0	0x4004 C000- 0x4004 C3FC				
Physical address View1	-				
Bitfield Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:8	Reserved	-		-	-
7:0	DATA	At reading: The logical product of the address to be accessed and terminal status can be read. PADDR[9:2] & GPIN[7:0] At writing: The logical product of the address to be accessed and written data and GPIO output settings is set for the terminal. PADDR[9:2] & PWDATA[7:0] & [GPIO1_GPIODIR].DIR[7:0]		RW modify	0x00

8.2. GPIO1_GPIODIR

GPIO1_GPIODIR					
Description	GPIO Data Direction Register				
Address Region	gpio1		**Type:**	RW	
Offset	0x0000 0400				
Physical address View0	0x4004 C400				
Physical address View1	-				
Bitfield Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:8	Reserved	-		-	-
7:0	DIR	Sets the data direction of each GPIO pin. 0b1: GPIO output 0b0: GPIO input		RW modify	0x00

8.3. GPIO1_GPIOIS

GPIO1_GPIOIS			
Description	GPIO Interrupt Sense Register		
Address Region	gpio1	**Type:**	RW
Offset	0x0000 0404		
Physical address View0	0x4004 C404		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	IS	Sets the interrupt detection method of each GPIO pin. GPIOIEV specifies other settings. 0b1: Level detection interrupt 0b0: Edge detection interrupt	RW modify	0x00

8.4. GPIO1_GPIOIBE

GPIO1_GPIOIBE			
Description	GPIO Interrupt Both Edges Register		
Address Region	gpio1	**Type:**	RW
Offset	0x0000 0408		
Physical address View0	0x4004 C408		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	IBE	Sets both-edge interrupt of each GPIO pin. GPIOIEV determines the edge to be used. 0b1: Both-edge interrupt 0b0: Single edge interrupt	RW modify	0x00

8.5. GPIO1_GPIOIEV

GPIO1_GPIOIEV			
Description	GPIO Interrupt Event Register		
Address Region	gpio1	**Type:**	RW
Offset	0x0000 040C		
Physical address View0	0x4004 C40C		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	IEV	Sets the edge interrupt method of each GPIO pin. 0b1: Rising edge interrupt or High-level interrupt 0b0: Falling edge interrupt or low-level interrupt	RW modify	0x00

8.6. GPIO1_GPIOIE

GPIO1_GPIOIE			
Description	GPIO Interrupt Enable Register		
Address Region	gpio1	**Type:**	RW
Offset	0x0000 0410		
Physical address View0	0x4004 C410		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	IE	Sets interrupt enable/mask for each GPIO pin. 0b1: Does not mask the interrupt (interrupt enable) 0b0: Masks the interrupt (interrupt disable)	RW modify	0x00

8.7. GPIO1_GPIORIS

GPIO1_GPIORIS			
Description	GPIO Raw Interrupt Status Register		
Address Region	gpio1	**Type:**	RO
Offset	0x0000 0414		
Physical address View0	0x4004 C414		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	RIS	Interrupt status before masking for each GPIO pin 0b1: Interrupt request available 0b0: No interrupt request	RO	0x00

8.8. GPIO1_GPIOMIS

GPIO1_GPIOMIS			
Description	GPIO Masked Interrupt Status Register		
Address Region	gpio1	**Type:**	RO
Offset	0x0000 0418		
Physical address View0	0x4004 C418		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	MIS	Interrupt status after masking for each GPIO pin 0b1: Interrupt request available 0b0: No interrupt request	RO	0x00

8.9. GPIO1_GPIOIC

GPIO1_GPIOIC			
Description	GPIO Interrupt Clear Register		
Address Region	gpio1	**Type:**	RW
Offset	0x0000 041C		
Physical address View0	0x4004 C41C		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	IC	Clears an interrupt for each GPIO pin. 0b1: Clears the interrupt. 0b0: Does nothing.	RW oneToClear	0x00

8.10. GPIO1_GPIOITCR

GPIO1_GPIOITCR			
Description	GPIO Integration Test Control Register		
Address Region	gpio1	**Type:**	RW
Offset	0x0000 0600		
Physical address View0	0x4004 C600		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	ITEN	Integration test enable 0b1: Test mode 0b0: Normal operation	RW modify	0

8.11. GPIO1_GPIOITIP1

GPIO1_GPIOITIP1			
Description	GPIO Integration test input read/set Register 1		
Address Region	gpio1	**Type:**	RW
Offset	0x0000 0604		
Physical address View0	0x4004 C604		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	GPAFOUT	For ITEM=1(Integration test mode), enables the GPAFOUT input signal to be controlled. At reading: Reads the output status of Mux at the GPAFOUT last stage. At writing: Enables alternate data to be written for GPAFOUT input. For ITEM=0(Normal mod), the GPAFOUT input status can be read intact. No operation for writing.	RW modify	0x00

8.12. GPIO1_GPIOITIP2

GPIO1_GPIOITIP2					
Description	GPIO Integration test input read/set Register 2				
Address Region	gpio1		**Type:**	RW	
Offset	0x0000 0608				
Physical address View0	0x4004 C608				
Physical address View1	-				
Bitfield Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:8	Reserved	-		-	-
7:0	nGPAFEN	For ITEM=1(Integration test mode), enables the nGPAFEN input signal to be controlled. At reading: Reads the output status of Mux at the nGPAFEN last stage. At writing: Enables alternate data to be written for nGPAFEN input. For ITEM=0(Normal mod), the nGPAFEN input status can be read intact. No operation for writing.		RW modify	0x00

8.13. GPIO1_GPIOITOP1

GPIO1_GPIOITOP1					
Description	GPIO Integration test output read/set Register 1				
Address Region	gpio1		**Type:**	RW	
Offset	0x0000 060C				
Physical address View0	0x4004 C60C				
Physical address View1	-				
Bitfield Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:8	Reserved	-		-	-
7:0	GPIOMIS	For ITEM=1(Integration test mode), enables the GPIOMIS output signal to be controlled. At reading: Returns 0. At writing: Writes data to be output to GPIOMIS. For ITEM=0(Normal mod), no operation for writing.		RW modify	0x00

8.14. GPIO1_GPIOITOP2

GPIO1_GPIOITOP2					
Description	GPIO Integration test output read/set Register 2				
Address Region	gpio1		**Type:**	RO	
Offset	0x0000 0610				
Physical address View0	0x4004 C610				
Physical address View1	-				
Bitfield Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:1	Reserved	-		-	-
0	GPIOINTR	For ITEM=1(Integration test mode), enables the status of the GPIOINTR output signal to be read. At reading: Reads the GPIOINTR status (GPIOINTR is a signal with GPIOMIS[7:0] being ORed).		RO	0

8.15. GPIO1_GPIOITOP3

GPIO1_GPIOITOP3					
Description	GPIO Integration test output read/set Register 3				
Address Region	gpio1		**Type:**	RW	
Offset	0x0000 0614				
Physical address View0	0x4004 C614				
Physical address View1	-				
Bitfield Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:8	Reserved	-		-	-
7:0	GPAFIN	For ITEM=1(Integration test mode), enables the GPIOAFIN output signal to be controlled. At reading: Reads the output status of Mux at the GPAFIN last stage. AT writing: Writes data to be output to GPAFIN. For ITEM=0(Normal mod), the GPAFIN output status can be read intact. No operation for writing.		RW modify	0x00

8.16. GPIO1_GPIOPERIPHID0

GPIO1_GPIOPERIPHID0			
Description	GPIO Peripheral ID0 Register		
Address Region	gpio1	**Type:**	RO
Offset	0x0000 0FE0		
Physical address View0	0x4004 CFE0		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	Partnumber0	Peripheral ID (this register stores a value from a hardware viewpoint.) Partnumber(Lower) 061=>61	RO	0x61

8.17. GPIO1_GPIOPERIPHID1

GPIO1_GPIOPERIPHID1			
Description	GPIO Peripheral ID1 Register		
Address Region	gpio1	**Type:**	RO
Offset	0x0000 0FE4		
Physical address View0	0x4004 CFE4		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:4	Designer0	Peripheral ID (this register stores a value from a hardware viewpoint.) Designer(Lower) 41=>1	RO	0x1
3:0	Partnumber1	Peripheral ID (this register stores a value from a hardware viewpoint.) Partnumber(Upper) 061=>0	RO	0x0

8.18. GPIO1_GPIOPERIPHID2

GPIO1_GPIOPERIPHID2			
Description	GPIO Peripheral ID2 Register		
Address Region	gpio1	**Type:**	RO
Offset	0x0000 0FE8		
Physical address View0	0x4004 CFE8		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:4	Revision	Peripheral ID (this register stores a value from a hardware viewpoint.) Revision: r1p0=>0	RO	0x0
3:0	Designer1	Peripheral ID (this register stores a value from a hardware viewpoint.) Designer(Upper) 41=>4	RO	0x4

8.19. GPIO1_GPIOPERIPHID3

GPIO1_GPIOPERIPHID3			
Description	GPIO Peripheral ID3 Register		
Address Region	gpio1	**Type:**	RO
Offset	0x0000 0FEC		
Physical address View0	0x4004 CFEC		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	Configuration	Peripheral ID (this register stores a value from a hardware viewpoint.) Configuration: 00	RO	0x00

8.20. GPIO1_GPIOPCELLID0

GPIO1_GPIOPCELLID0			
Description	GPIO PrimeCell ID0 Register		
Address Region	gpio1	**Type:**	RO
Offset	0x0000 0FF0		
Physical address View0	0x4004 CFF0		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	PCellID0	PrimeCell ID (this register stores a value from a hardware viewpoint). Fixed value.	RO	0x0D

8.21. GPIO1_GPIOPCELLID1

GPIO1_GPIOPCELLID1			
Description	GPIO PrimeCell ID1 Register		
Address Region	gpio1	**Type:**	RO
Offset	0x0000 0FF4		
Physical address View0	0x4004 CFF4		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	PCellID1	PrimeCell ID (this register stores a value from a hardware viewpoint). Fixed value.	RO	0xF0

8.22. GPIO1_GPIOPCELLID2

GPIO1_GPIOPCELLID2			
Description	GPIO PrimeCell ID2 Register		
Address Region	gpio1	**Type:**	RO
Offset	0x0000 0FF8		
Physical address View0	0x4004 CFF8		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	PCellID2	PrimeCell ID (this register stores a value from a hardware viewpoint). Fixed value.	RO	0x05

8.23. GPIO1_GPIOPCELLID3

GPIO1_GPIOPCELLID3			
Description	GPIO PrimeCell ID3 Register		
Address Region	gpio1	**Type:**	RO
Offset	0x0000 0FFC		
Physical address View0	0x4004 CFFC		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	PCellID3	PrimeCell ID (this register stores a value from a hardware viewpoint). Fixed value.	RO	0xB1

9. Details of MCU General-Purpose Input/Output Controller 2 Registers

9.1. GPIO2_GPIODATA

GPIO2_GPIODATA					
Description	GPIO Data Register				
Address Region	gpio2		**Type:**	RW	
Offset	0x0000 0000-				
Physical address View0	0x4004 D000- 0x4004 D3FC				
Physical address View1	-				
Bitfield Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:8	Reserved	-		-	-
7:0	DATA	At reading: The logical product of the address to be accessed and terminal status can be read. PADDR[9:2] & GPIN[7:0] At writing: The logical product of the address to be accessed and written data and GPIO output settings is set for the terminal. PADDR[9:2] & PWDATA[7:0] & [GPIO2_GPIODIR].DIR[7:0]		RW modify	0x00

9.2. GPIO2_GPIODIR

GPIO2_GPIODIR					
Description	GPIO Data Direction Register				
Address Region	gpio2		**Type:**	RW	
Offset	0x0000 0400				
Physical address View0	0x4004 D400				
Physical address View1	-				
Bitfield Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:8	Reserved	-		-	-
7:0	DIR	Sets the data direction of each GPIO pin. 0b1: GPIO output 0b0: GPIO input		RW modify	0x00

9.3. GPIO2_GPIOIS

GPIO2_GPIOIS			
Description	GPIO Interrupt Sense Register		
Address Region	gpio2	**Type:**	RW
Offset	0x0000 0404		
Physical address View0	0x4004 D404		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	IS	Sets the interrupt detection method of each GPIO pin. GPIOIEV specifies other settings. 0b1: Level detection interrupt 0b0: Edge detection interrupt	RW modify	0x00

9.4. GPIO2_GPIOIBE

GPIO2_GPIOIBE			
Description	GPIO Interrupt Both Edges Register		
Address Region	gpio2	**Type:**	RW
Offset	0x0000 0408		
Physical address View0	0x4004 D408		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	IBE	Sets both-edge interrupt of each GPIO pin. GPIOIEV determines the edge to be used. 0b1: Both-edge interrupt 0b0: Single edge interrupt	RW modify	0x00

9.5. GPIO2_GPIOIEV

GPIO2_GPIOIEV			
Description	GPIO Interrupt Event Register		
Address Region	gpio2	**Type:**	RW
Offset	0x0000 040C		
Physical address View0	0x4004 D40C		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	IEV	Sets the edge interrupt method of each GPIO pin. 0b1: Rising edge interrupt or High-level interrupt 0b0: Falling edge interrupt or low-level interrupt	RW modify	0x00

9.6. GPIO2_GPIOIE

GPIO2_GPIOIE			
Description	GPIO Interrupt Enable Register		
Address Region	gpio2	**Type:**	RW
Offset	0x0000 0410		
Physical address View0	0x4004 D410		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	IE	Sets interrupt enable/mask for each GPIO pin. 0b1: Does not mask the interrupt (interrupt enable) 0b0: Masks the interrupt (interrupt disable)	RW modify	0x00

9.7. GPIO2_GPIORIS

GPIO2_GPIORIS			
Description	GPIO Raw Interrupt Status Register		
Address Region	gpio2	**Type:**	RO
Offset	0x0000 0414		
Physical address View0	0x4004 D414		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	RIS	Interrupt status before masking for each GPIO pin 0b1: Interrupt request available 0b0: No interrupt request	RO	0x00

9.8. GPIO2_GPIOMIS

GPIO2_GPIOMIS			
Description	GPIO Masked Interrupt Status Register		
Address Region	gpio2	**Type:**	RO
Offset	0x0000 0418		
Physical address View0	0x4004 D418		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	MIS	Interrupt status after masking for each GPIO pin 0b1: Interrupt request available 0b0: No interrupt request	RO	0x00

9.9. GPIO2_GPIOIC

GPIO2_GPIOIC			
Description	GPIO Interrupt Clear Register		
Address Region	gpio2	**Type:**	RW
Offset	0x0000 041C		
Physical address View0	0x4004 D41C		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	IC	Clears an interrupt for each GPIO pin. 0b1: Clears the interrupt. 0b0: Does nothing.	RW oneToClear	0x00

9.10. GPIO2_GPIOITCR

GPIO2_GPIOITCR			
Description	GPIO Integration Test Control Register		
Address Region	gpio2	**Type:**	RW
Offset	0x0000 0600		
Physical address View0	0x4004 D600		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	ITEN	Integration test enable 0b1: Test mode 0b0: Normal operation	RW modify	0

9.11. GPIO2_GPIOITIP1

GPIO2_GPIOITIP1			
Description	GPIO Integration test input read/set Register 1		
Address Region	gpio2	**Type:**	RW
Offset	0x0000 0604		
Physical address View0	0x4004 D604		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	GPAFOUT	For ITEM=1(Integration test mode), enables the GPAFOUT input signal to be controlled. At reading: Reads the output status of Mux at the GPAFOUT last stage. At writing: Enables alternate data to be written for GPAFOUT input. For ITEM=0(Normal mod), the GPAFOUT input status can be read intact. No operation for writing.	RW modify	0x00

9.12. GPIO2_GPIOITIP2

GPIO2_GPIOITIP2			
Description	GPIO Integration test input read/set Register 2		
Address Region	gpio2	**Type:**	RW
Offset	0x0000 0608		
Physical address View0	0x4004 D608		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	nGPAFEN	For ITEM=1(Integration test mode), enables the nGPAFEN input signal to be controlled. At reading: Reads the output status of Mux at the nGPAFEN last stage. At writing: Enables alternate data to be written for nGPAFEN input. For ITEM=0(Normal mod), the nGPAFEN input status can be read intact. No operation for writing.	RW modify	0x00

9.13. GPIO2_GPIOITOP1

GPIO2_GPIOITOP1			
Description	GPIO Integration test output read/set Register 1		
Address Region	gpio2	**Type:**	RW
Offset	0x0000 060C		
Physical address View0	0x4004 D60C		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	GPIOMIS	For ITEM=1(Integration test mode), enables the GPIOMIS output signal to be controlled. At reading: Returns 0. At writing: Writes data to be output to GPIOMIS. For ITEM=0(Normal mod), no operation for writing.	RW modify	0x00

9.14. GPIO2_GPIOITOP2

GPIO2_GPIOITOP2			
Description	GPIO Integration test output read/set Register 2		
Address Region	gpio2	**Type:**	RO
Offset	0x0000 0610		
Physical address View0	0x4004 D610		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:1	Reserved	-	-	-
0	GPIOINTR	For ITEM=1(Integration test mode), enables the status of the GPIOINTR output signal to be read. At reading: Reads the GPIOINTR status (GPIOINTR is a signal with GPIOMIS[7:0] being ORed).	RO	0

9.15. GPIO2_GPIOITOP3

GPIO2_GPIOITOP3			
Description	GPIO Integration test output read/set Register 3		
Address Region	gpio2	**Type:**	RW
Offset	0x0000 0614		
Physical address View0	0x4004 D614		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:8	Reserved	-	-	-
7:0	GPAFIN	For ITEM=1(Integration test mode), enables the GPIOAFIN output signal to be controlled. At reading: Reads the output status of Mux at the GPAFIN last stage. AT writing: Writes data to be output to GPAFIN. For ITEM=0(Normal mod), the GPAFIN output status can be read intact. No operation for writing.	RW modify	0x00

9.16. GPIO2_GPIOPERIPHID0

GPIO2_GPIOPERIPHID0			
Description	GPIO Peripheral ID0 Register		
Address Region	gpio2	**Type:**	RO
Offset	0x0000 0FE0		
Physical address View0	0x4004 DFE0		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	Partnumber0	Peripheral ID (this register stores a value from a hardware viewpoint.) Partnumber(Lower) 061=>61	RO	0x61

9.17. GPIO2_GPIOPERIPHID1

GPIO2_GPIOPERIPHID1			
Description	GPIO Peripheral ID1 Register		
Address Region	gpio2	**Type:**	RO
Offset	0x0000 0FE4		
Physical address View0	0x4004 DFE4		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:4	Designer0	Peripheral ID (this register stores a value from a hardware viewpoint.) Designer(Lower) 41=>1	RO	0x1
3:0	Partnumber1	Peripheral ID (this register stores a value from a hardware viewpoint.) Partnumber(Upper) 061=>0	RO	0x0

9.18. GPIO2_GPIOPERIPHID2

GPIO2_GPIOPERIPHID2			
Description	GPIO Peripheral ID2 Register		
Address Region	gpio2	**Type:**	RO
Offset	0x0000 0FE8		
Physical address View0	0x4004 DFE8		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:4	Revision	Peripheral ID (this register stores a value from a hardware viewpoint.) Revision: r1p0=>0	RO	0x0
3:0	Designer1	Peripheral ID (this register stores a value from a hardware viewpoint.) Designer(Upper) 41=>4	RO	0x4

9.19. GPIO2_GPIOPERIPHID3

GPIO2_GPIOPERIPHID3			
Description	GPIO Peripheral ID3 Register		
Address Region	gpio2	**Type:**	RO
Offset	0x0000 0FEC		
Physical address View0	0x4004 DFEC		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:8	Reserved	-	-	-
7:0	Configuration	Peripheral ID (this register stores a value from a hardware viewpoint.) Configuration: 00	RO	0x00

9.20. GPIO2_GPIOPCELLID0

GPIO2_GPIOPCELLID0			
Description	GPIO PrimeCell ID0 Register		
Address Region	gpio2	**Type:**	RO
Offset	0x0000 0FF0		
Physical address View0	0x4004 DFF0		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:8	Reserved	-	-	-
7:0	PCellID0	PrimeCell ID (this register stores a value from a hardware viewpoint). Fixed value.	RO	0x0D

9.21. GPIO2_GPIOPCELLID1

GPIO2_GPIOPCELLID1			
Description	GPIO PrimeCell ID1 Register		
Address Region	gpio2	**Type:**	RO
Offset	0x0000 0FF4		
Physical address View0	0x4004 DFF4		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:8	Reserved	-	-	-
7:0	PCellID1	PrimeCell ID (this register stores a value from a hardware viewpoint). Fixed value.	RO	0xF0

9.22. GPIO2_GPIOPCELLID2

GPIO2_GPIOPCELLID2				
Description	GPIO PrimeCell ID2 Register			
Address Region	gpio2	**Type:**	RO	
Offset	0x0000 0FF8			
Physical address View0	0x4004 DFF8			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	PCellID2	PrimeCell ID (this register stores a value from a hardware viewpoint). Fixed value.	RO	0x05

9.23. GPIO2_GPIOPCELLID3

GPIO2_GPIOPCELLID3				
Description	GPIO PrimeCell ID3 Register			
Address Region	gpio2	**Type:**	RO	
Offset	0x0000 0FFC			
Physical address View0	0x4004 DFFC			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	PCellID3	PrimeCell ID (this register stores a value from a hardware viewpoint). Fixed value.	RO	0xB1

10. Details of MCU General-Purpose Input/Output Controller 3 Registers

10.1. GPIO3_GPIODATA

GPIO3_GPIODATA			
Description	GPIO Data Register		
Address Region	gpio3	**Type:**	RW
Offset	0x0000 0000-		
Physical address View0	0x4004 E000- 0x4004 E3FC		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	DATA	At reading: The logical product of the address to be accessed and terminal status can be read. PADDR[9:2] & GPIN[7:0] At writing: The logical product of the address to be accessed and written data and GPIO output settings is set for the terminal. PADDR[9:2] & PWDATA[7:0] & [GPIO3_GPIODIR].DIR[7:0]	RW modify	0x00

10.2. GPIO3_GPIODIR

GPIO3_GPIODIR			
Description	GPIO Data Direction Register		
Address Region	gpio3	**Type:**	RW
Offset	0x0000 0400		
Physical address View0	0x4004 E400		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	DIR	Sets the data direction of each GPIO pin. 0b1: GPIO output 0b0: GPIO input	RW modify	0x00

10.3. GPIO3_GPIOIS

GPIO3_GPIOIS			
Description	GPIO Interrupt Sense Register		
Address Region	gpio3	**Type:**	RW
Offset	0x0000 0404		
Physical address View0	0x4004 E404		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	IS	Sets the interrupt detection method of each GPIO pin. GPIOIEV specifies other settings. 0b1: Level detection interrupt 0b0: Edge detection interrupt	RW modify	0x00

10.4. GPIO3_GPIOIBE

GPIO3_GPIOIBE			
Description	GPIO Interrupt Both Edges Register		
Address Region	gpio3	**Type:**	RW
Offset	0x0000 0408		
Physical address View0	0x4004 E408		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	IBE	Sets both-edge interrupt of each GPIO pin. GPIOIEV determines the edge to be used. 0b1: Both-edge interrupt 0b0: Single edge interrupt	RW modify	0x00

10.5. GPIO3_GPIOIEV

GPIO3_GPIOIEV			
Description	GPIO Interrupt Event Register		
Address Region	gpio3	**Type:**	RW
Offset	0x0000 040C		
Physical address View0	0x4004 E40C		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	IEV	Sets the edge interrupt method of each GPIO pin. 0b1: Rising edge interrupt or High-level interrupt 0b0: Falling edge interrupt or low-level interrupt	RW modify	0x00

10.6. GPIO3_GPIOIE

GPIO3_GPIOIE			
Description	GPIO Interrupt Enable Register		
Address Region	gpio3	**Type:**	RW
Offset	0x0000 0410		
Physical address View0	0x4004 E410		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	IE	Sets interrupt enable/mask for each GPIO pin. 0b1: Does not mask the interrupt (interrupt enable) 0b0: Masks the interrupt (interrupt disable)	RW modify	0x00

10.7. GPIO3_GPIORIS

GPIO3_GPIORIS			
Description	GPIO Raw Interrupt Status Register		
Address Region	gpio3	**Type:**	RO
Offset	0x0000 0414		
Physical address View0	0x4004 E414		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	RIS	Interrupt status before masking for each GPIO pin 0b1: Interrupt request available 0b0: No interrupt request	RO	0x00

10.8. GPIO3_GPIOMIS

GPIO3_GPIOMIS			
Description	GPIO Masked Interrupt Status Register		
Address Region	gpio3	**Type:**	RO
Offset	0x0000 0418		
Physical address View0	0x4004 E418		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	MIS	Interrupt status after masking for each GPIO pin 0b1: Interrupt request available 0b0: No interrupt request	RO	0x00

10.9. GPIO3_GPIOIC

GPIO3_GPIOIC			
Description	GPIO Interrupt Clear Register		
Address Region	gpio3	**Type:**	RW
Offset	0x0000 041C		
Physical address View0	0x4004 E41C		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	IC	Clears an interrupt for each GPIO pin. 0b1: Clears the interrupt. 0b0: Does nothing.	RW oneToClear	0x00

10.10. GPIO3_GPIOITCR

GPIO3_GPIOITCR			
Description	GPIO Integration Test Control Register		
Address Region	gpio3	**Type:**	RW
Offset	0x0000 0600		
Physical address View0	0x4004 E600		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	ITEN	Integration test enable 0b1: Test mode 0b0: Normal operation	RW modify	0

10.11. GPIO3_GPIOITIP1

GPIO3_GPIOITIP1			
Description	GPIO Integration test input read/set Register 1		
Address Region	gpio3	**Type:**	RW
Offset	0x0000 0604		
Physical address View0	0x4004 E604		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	GPAFOUT	For ITEM=1(Integration test mode), enables the GPAFOUT input signal to be controlled. At reading: Reads the output status of Mux at the GPAFOUT last stage. At writing: Enables alternate data to be written for GPAFOUT input. For ITEM=0(Normal mod), the GPAFOUT input status can be read intact. No operation for writing.	RW modify	0x00

10.12. GPIO3_GPIOITIP2

GPIO3_GPIOITIP2			
Description	GPIO Integration test input read/set Register 2		
Address Region	gpio3	**Type:**	RW
Offset	0x0000 0608		
Physical address View0	0x4004 E608		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	nGPAFEN	For ITEM=1(Integration test mode), enables the nGPAFEN input signal to be controlled. At reading: Reads the output status of Mux at the nGPAFEN last stage. At writing: Enables alternate data to be written for nGPAFEN input. For ITEM=0(Normal mod), the nGPAFEN input status can be read intact. No operation for writing.	RW modify	0x00

10.13. GPIO3_GPIOITOP1

GPIO3_GPIOITOP1			
Description	GPIO Integration test output read/set Register 1		
Address Region	gpio3	**Type:**	RW
Offset	0x0000 060C		
Physical address View0	0x4004 E60C		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	GPIOMIS	For ITEM=1(Integration test mode), enables the GPIOMIS output signal to be controlled. At reading: Returns 0. At writing: Writes data to be output to GPIOMIS. For ITEM=0(Normal mod), no operation for writing.	RW modify	0x00

10.14. GPIO3_GPIOITOP2

GPIO3_GPIOITOP2			
Description	GPIO Integration test output read/set Register 2		
Address Region	gpio3	**Type:**	RO
Offset	0x0000 0610		
Physical address View0	0x4004 E610		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	GPIOINTR	For ITEM=1(Integration test mode), enables the status of the GPIOINTR output signal to be read. At reading: Reads the GPIOINTR status (GPIOINTR is a signal with GPIOMIS[7:0] being ORed).	RO	0

10.15. GPIO3_GPIOITOP3

GPIO3_GPIOITOP3			
Description	GPIO Integration test output read/set Register 3		
Address Region	gpio3	**Type:**	RW
Offset	0x0000 0614		
Physical address View0	0x4004 E614		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	GPAFIN	For ITEM=1(Integration test mode), enables the GPIOAFIN output signal to be controlled. At reading: Reads the output status of Mux at the GPAFIN last stage. AT writing: Writes data to be output to GPAFIN. For ITEM=0(Normal mod), the GPAFIN output status can be read intact. No operation for writing.	RW modify	0x00

10.16. GPIO3_GPIOPERIPHID0

GPIO3_GPIOPERIPHID0			
Description	GPIO Peripheral ID0 Register		
Address Region	gpio3	**Type:**	RO
Offset	0x0000 0FE0		
Physical address View0	0x4004 EFE0		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	Partnumber0	Peripheral ID (this register stores a value from a hardware viewpoint.) Partnumber(Lower) 061=>61	RO	0x61

10.17. GPIO3_GPIOPERIPHID1

GPIO3_GPIOPERIPHID1			
Description	GPIO Peripheral ID1 Register		
Address Region	gpio3	**Type:**	RO
Offset	0x0000 0FE4		
Physical address View0	0x4004 EFE4		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:4	Designer0	Peripheral ID (this register stores a value from a hardware viewpoint.) Designer(Lower) 41=>1	RO	0x1
3:0	Partnumber1	Peripheral ID (this register stores a value from a hardware viewpoint.) Partnumber(Upper) 061=>0	RO	0x0

10.18. GPIO3_GPIOPERIPHID2

GPIO3_GPIOPERIPHID2			
Description	GPIO Peripheral ID2 Register		
Address Region	gpio3	**Type:**	RO
Offset	0x0000 0FE8		
Physical address View0	0x4004 EFE8		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:4	Revision	Peripheral ID (this register stores a value from a hardware viewpoint.) Revision: r1p0=>0	RO	0x0
3:0	Designer1	Peripheral ID (this register stores a value from a hardware viewpoint.) Designer(Upper) 41=>4	RO	0x4

10.19. GPIO3_GPIOPERIPHID3

GPIO3_GPIOPERIPHID3			
Description	GPIO Peripheral ID3 Register		
Address Region	gpio3	**Type:**	RO
Offset	0x0000 0FEC		
Physical address View0	0x4004 EFEC		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:8	Reserved	-	-	-
7:0	Configuration	Peripheral ID (this register stores a value from a hardware viewpoint.) Configuration: 00	RO	0x00

10.20. GPIO3_GPIOPCELLID0

GPIO3_GPIOPCELLID0			
Description	GPIO PrimeCell ID0 Register		
Address Region	gpio3	**Type:**	RO
Offset	0x0000 0FF0		
Physical address View0	0x4004 EFF0		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:8	Reserved	-	-	-
7:0	PCellID0	PrimeCell ID (this register stores a value from a hardware viewpoint). Fixed value.	RO	0x0D

10.21. GPIO3_GPIOPCELLID1

GPIO3_GPIOPCELLID1			
Description	GPIO PrimeCell ID1 Register		
Address Region	gpio3	**Type:**	RO
Offset	0x0000 0FF4		
Physical address View0	0x4004 EFF4		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:8	Reserved	-	-	-
7:0	PCellID1	PrimeCell ID (this register stores a value from a hardware viewpoint). Fixed value.	RO	0xF0

10.22. GPIO3_GPIOPCELLID2

GPIO3_GPIOPCELLID2				
Description	GPIO PrimeCell ID2 Register			
Address Region	gpio3	**Type:**	RO	
Offset	0x0000 0FF8			
Physical address View0	0x4004 EFF8			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	PCellID2	PrimeCell ID (this register stores a value from a hardware viewpoint). Fixed value.	RO	0x05

10.23. GPIO3_GPIOPCELLID3

GPIO3_GPIOPCELLID3				
Description	GPIO PrimeCell ID3 Register			
Address Region	gpio3	**Type:**	RO	
Offset	0x0000 0FFC			
Physical address View0	0x4004 EFFC			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	PCellID3	PrimeCell ID (this register stores a value from a hardware viewpoint). Fixed value.	RO	0xB1

11. Revision History

Table 11.1 Revision History

Revision	Date	Description
0.1	2014-10-14	Newly released
0.2	2015-01-07	Section 1 Added a description of the number of GPIO channel Section 5.2 Added register setting value for the interrupt disable
1.0	2015-01-22	Official version
1.1	2018-02-06	Changed header, footer and the last page. Changed corporate name and descriptions. Modified Arm logo and descriptions.

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