Application Processor Lite *ApP Lite*

TZ1000 Series

Reference Manual

MCU Global Configuration Block

Revision 1.1

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TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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Preface

This document provides the specification for the Global Configuration Block for the TZ1000 Series.

The following chapters may refer to the MCU Global Configuration Block as "gconf."

Intended Audience

This document is intended for the following users.

Driver software developers.

System designers

Conventions in this Document

- The following notational conventions apply to numbers:
  Hexadecimal number: 0xABC
  Decimal number: 123 or 0d123 (only when it should be explicitly indicated that the number is decimal)
  Binary number: 0b111 (It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.)
- Low active signals are indicated with a name suffixed with "_N".
- A signal is asserted when it goes to its active level while it is de-asserted when it goes to its inactive level.
- A set of multiple signals may be referred to as [m:n].
  Example: S[3:0] indicates four signals, S3, S2, S1 and S0, collectively.
- In the text, register names are enclosed in brackets *[ ]*.
  Example:*[ABCD]*
- A set of multiple registers, fields or bits of the same type may be described collectively using "n".
  Example: *[XYZ1], [XYZ2], and [XYZ3] to [XYZn]*
  A range of register bits are referred to as [m:n].
  Example: [3:0] indicates a range from bit 3 to bit 0.
- Values set in registers are indicated using either a hexadecimal or binary number.
- Example: *[ABCD]*.EFG = 0x01 (hexadecimal), *[XYZn]*.VW = 1 (binary)
- Words and bytes are defined as follows:
  Byte: 8 bits
  Halfword: 16 bits
  Word: 32 bits
  Doubleword: 64 bits
- Register bit attributes are defined as follows:
  R: Read-only
  W: Write-only
  W1C: Clear by write of 1 (a write of "1" clears the corresponding bit to 0)
  W1S: Set by write of 1 (a write of "1" sets the corresponding bit to 1)
  R/W: Read/Write
  R/W0C: Read/Clear by write of 0
  R/W1C: Read/Clear by write of 1
  R/W1S: Read/Set by write of 1
  RS/WC: Set by read/Clear by write (set after a read and cleared after a data write)
- Registers only support word access unless otherwise specified.
- Any registers defined as Reserved in the text must not be rewritten. Also, any values read from such registers should not be used.
- Any bits for which default values are defined as "-" would return undefined values if read.
- When a data is written to a register containing both writable and read-only (R) bit fields, its default values should be written to read-only (R) bit fields. For any bit fields with default values defined as "-", refer to the definitions of the relevant register.
- Default values should be written to any reserved bit fields in a write-only register. For any bit fields with default values defined as "-", refer to the definitions of the relevant register.

1. Overview

This module consists of general purpose configuration registers. It outputs the configuration data to the MCU internal modules in the TZ1000 Series. And it also receives the status signals from the MCU internal modules.

The function outlines are shown as follows.

- The following configuration data are output.
  - The TIMCLKEN signal to the TMR module
  - The TIMCLKEN signal to the ADVTMR module
  - The TIMCLKEN signal to the WDT module
  - Ch0 to Ch7 DMA request selection signal to the SDMAC module.
  - The FSIO adjustment signal to the UFB module
  - The setting signals to the CPU module
  - The drivability setting signal to the IO cell
  - The Pull-up or Pull-down setting signal to IO cell
  - The selection signal of the multiple functions to the shared IO (the IOMUX control signal)

- The following status signals are mapped to be read.
  - The status signals of the I2C0/I2C1/I2C2 modules
  - The sleep status signals of the SPIM0/SPIM1/SPIM2/SPIM3 modules.
  - The FPU status signal of the CPU module

The configuration data from the registers can be read and written through the APB0 bus.

The status signals can be read through the APB0 bus.

2. Block Diagram

The block diagram of this module is shown in the following figure.

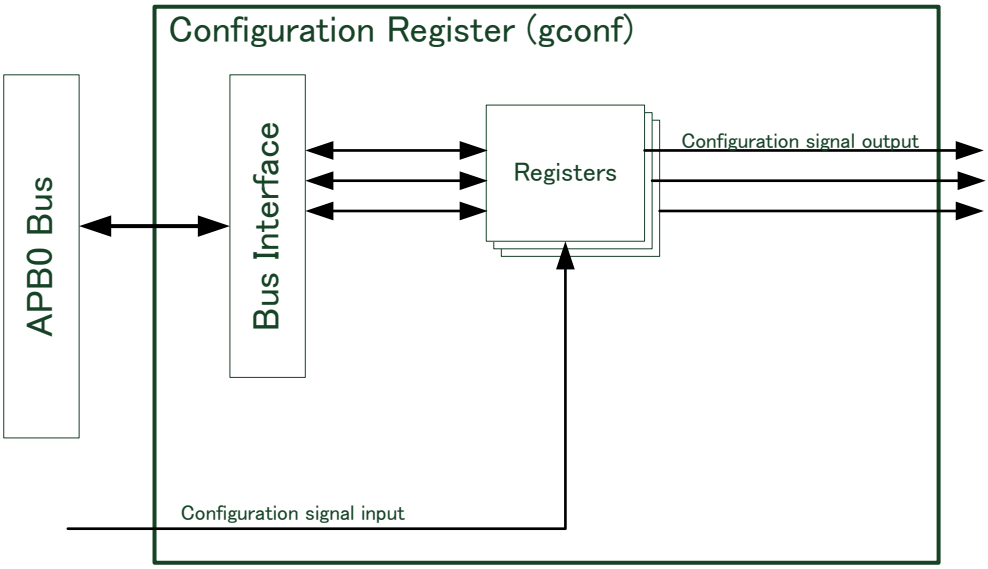

Figure 2.1 Internal block diagram

3. Address Map

Table 3.1 MCU Global Configuration Block Register Map

Register Name	Type	Width	Reset Value	Address Offset
TMR_TIMCLKEN	RW	32	0x0000 0003	0x0000 0000
ADVTMR_TIMCLKEN	RW	32	0x0000 000F	0x0000 0004
WDT_WDTCLKEN	RW	32	0x0000 0001	0x0000 0010
I2C0_STAT	RO	32	0x0000 0000	0x0000 0020
I2C1_STAT	RO	32	0x0000 0000	0x0000 0024
I2C2_STAT	RO	32	0x0000 0000	0x0000 0028
SPIM0_SLEEP	RO	32	0x0000 0001	0x0000 0030
SPIM1_SLEEP	RO	32	0x0000 0001	0x0000 0034
SPIM2_SLEEP	RO	32	0x0000 0001	0x0000 0038
SPIM3_SLEEP	RO	32	0x0000 0001	0x0000 003C
DMACREQ_SEL0	RW	32	0x0000 003F	0x0000 0040
DMACREQ_SEL1	RW	32	0x0000 003F	0x0000 0044
DMACREQ_SEL2	RW	32	0x0000 003F	0x0000 0048
DMACREQ_SEL3	RW	32	0x0000 003F	0x0000 004C
DMACREQ_SEL4	RW	32	0x0000 003F	0x0000 0050
DMACREQ_SEL5	RW	32	0x0000 003F	0x0000 0054
DMACREQ_SEL6	RW	32	0x0000 003F	0x0000 0058
DMACREQ_SEL7	RW	32	0x0000 003F	0x0000 005C
USB_FSIO_TUNE	RW	32	0x0000 0B3E	0x0000 0080
CPU_STCALIB	RW	32	0x0000 0000	0x0000 00C0
CPU_TSENABLE	RW	32	0x0000 0000	0x0000 00C4
CPU_FPUIRQEN	RW	32	0x0000 0000	0x0000 00CC
CPU_DEBUGIN	RW	32	0x0000 0001	0x0000 00D0
IO_CFG0	RW	32	0x1111 1110	0x0000 0100
IO_CFG1	RW	32	0x1111 1111	0x0000 0104
IO_CFG2	RO	32	0x0000 0000	0x0000 0108
IO_CFG3	RW	32	0x1110 1111	0x0000 010C
IO_CFG4	RW	32	0x0000 1111	0x0000 0110
IO_CFG5	RW	32	0x1111 0011	0x0000 0114
IO_CFG6	RW	32	0x0000 1111	0x0000 0118
IO_CFG7	RW	32	0x1111 1111	0x0000 011C
IO_CFG8	RW	32	0x1111 1111	0x0000 0120
IO_CFG9	RW	32	0x00EE EECE	0x0000 0124
IO_CFG10	RW	32	0x0000 0001	0x0000 0128
IO_CFG11	RW	32	0x0000 0000	0x0000 012C
FMODE_CFG0	RW	32	0x0000 0000	0x0000 0140
FMODE_CFG1	RW	32	0x0000 0000	0x0000 0144
FMODE_CFG2	RW	32	0x0000 0000	0x0000 0148
FMODE_CFG3	RW	32	0x0000 0000	0x0000 014C
FMODE_CFG4	RW	32	0x0000 0000	0x0000 0150
FMODE_CFG5	RW	32	0x0000 0000	0x0000 0154
FMODE_CFG6	RW	32	0x0000 0000	0x0000 0158
OE_CTRL	RW	32	0x0000 0000	0x0000 0200

4. Function

4.1. Clock and Reset

The MCU Global Configuration Block operates with a single system clock which is supplied by the PMU. The clock can be stopped unless this module is active (Dynamic clock gating structure) to reduce power dissipation.

The MCU Global Configuration Block receives an asynchronous reset produced by the PMU.

4.2. Operation

4.2.1. Operation of Configuration Register

The MCU Global Configuration Block supports the read and write data only in units of 32-bit. The write and read by the CPU should be done in the 32-bit unit.

4.2.2. Start-up Procedure

The MCU Global Configuration Block becomes the following state after the power-on reset on this product.

- Power supply domain (PM_B): the ON state
- Clock: the stop state
- Reset: the assertion state

Before the MCU Global Configuration Block operates, the PMU registers should be set to supply the clock and deassert the reset.

The following setting supplies the clock to the MCU Global Configuration Block.

- PMU *[CG_OFF_PM_2]*.CG_ppier0clk_gconf_pclk is set to 1.

The following setting deasserts the reset to the gconf.

- PMU *[SRST_OFF_PM_2]*.SRST_asyncrst_gconf_prstn is set to 1.

The dynamic clock gating for the MCU Global Configuration Block clock becomes valid when the following setting is done.

- PMU *[DCG_PM_2]*. DCG_ppier0clk_gconf_pclk is set to 1.

4.2.3. Stop Procedure

When the MCU Global Configuration Block is not used, the PMU register should be set to assert the reset and to stop the clock.

The following setting asserts the reset to the gconf.

- PMU *[SRST_ON_PM_2]*.SRST_asyncrst_gconf_prstn is set to 1.

The following setting stops the clock to the gconf.

- PMU *[CG_ON_PM_2]*.CG_ppier0clk_gconf_pclk is set to 1.

When the MCU Global Configuration Block is reset, the reset also asserts to the setting signals for the change of the multi-function IO and for the configuration data to other modules. So the other modules and the IO states should be checked before the reset asserts to the MCU Global Configuration Block.

If the clock to the MCU Global Configuration Block stops without asserting the reset, the register values and the configuration data in the modules are kept unchanged.

4.3. Power Management

The following shows the gconf state in each power mode.

- SLEEP0/1: Normal operation
- SLEEP2, WAIT, WAIT-RETENTION, and RETENTION: The clock stops to the MCU Global Configuration Block. The register values and the configuration data in the modules are kept unchanged. When returning from one of those modes, no restoration operation is necessary because the gconf has the configuration data before the mode transition.
- RTC and STOP: The clock stops to the MCU Global Configuration Block. The power supply is also shut down. By setting the PMU register, the status of the IO can be kept in the RTC and STOP modes. For detail, refer to Chapter.3. IO Control. When returning from the RTC or STOP mode, the re-setting is necessary because the gconf register is initialized.

5. Details of Registers

5.1. TMR_TIMCLKEN

TMR_TIMCLKEN				
Description				
Address Region	gconf	**Type:**	RW	
Offset	0x0000 0000			
Physical address View0	0x4004 A000			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:2	Reserved	-	-	-
1	TMR_TIMCLKEN1	tmr clock enable 1 1: Enable 0: Disable	RW modify	1
0	TMR_TIMCLKEN0	tmr clock enable 0 1: Enable 0: Disable	RW modify	1

5.2. ADVTMR_TIMCLKEN

ADVTMR_TIMCLKEN				
Description				
Address Region	gconf	**Type:**	RW	
Offset	0x0000 0004			
Physical address View0	0x4004 A004			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:4	Reserved	-	-	-
3	ADVTMR_T3TIMCLKEN	advtmr clock enable 3 1: Enable 0: Disable	RW modify	1
2	ADVTMR_T2TIMCLKEN	advtmr clock enable 2 1: Enable 0: Disable	RW modify	1
1	ADVTMR_T1TIMCLKEN	advtmr clock enable 1 1: Enable 0: Disable	RW modify	1
0	ADVTMR_T0TIMCLKEN	advtmr clock enable 0 1: Enable 0: Disable	RW modify	1

5.3. WDT_WDTCLKEN

WDT_WDTCLKEN				
Description				
Address Region	gconf	**Type:**	RW	
Offset	0x0000 0010			
Physical address View0	0x4004 A010			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	WDT_WDTCLKEN	wdt clock enable 1: Enable 0: Disable	RW modify	1

5.4. I2C0_STAT

I2C0_STAT			
Description			
Address Region	gconf	**Type:**	RO
Offset	0x0000 0020		
Physical address View0	0x4004 A020		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:29	Reserved	-	-	-
28	I2C0_IC_EN	i2c0 status (i2c enable) [I2C0_IC_ENABLE].ENABLE bit is indicated. 1 : I2C0 is enabled. 0 : I2C0 is disabled.	RO	0
27:26	Reserved	-	-	-
25	I2C0_S_GEN	i2c0 status (start condition period) This bit indicates whether I2C0 is generating a START Condition on the I2C bus in the Master Mode. 1 : I2C0 is generating a START Condition. 0 : I2C0 is not generating a START Condition.	RO	0
24	I2C0_P_GEN	i2c0 status (stop condition period) This bit indicates whether I2C0 is generating a STOP Condition on the I2C bus in the Master Mode. 1 : I2C0 is generating a STOP Condition. 0 : I2C0 is not generating a STOP Condition.	RO	0
23:22	Reserved	-	-	-
21	I2C0_DATA	i2c0 status (data communication period) This bit indicates whether I2C0 is in the data phase on the I2C bus. 1 : I2C0 is in the data phase. 0 : I2C0 is not in the data phase.	RO	0
20	I2C0_ADDR	i2c0 status (address communication period) This bit indicates whether I2C0 is in the address phase on the I2C bus. 1 : I2C0 is in the address phase. 0 : I2C0 is not in the address phase.	RO	0
19:18	Reserved	-	-	-
17	I2C0_RD	i2c0 status (i2c read status) This bit indicates whether I2C0 is in a read transaction on the I2C bus in the Master Mode. 1 : I2C0 is in a read transaction. 0 : I2C0 is not in a read transaction.	RO	0
16	I2C0_WR	i2c0 status (i2c write status) This bit indicates whether I2C0 is in a write transaction on the I2C bus in the Master Mode. 1 : I2C0 is in a write transaction. 0 : I2C0 is not in a write transaction.	RO	0

15:14	Reserved	-	-	-
13	I2C0_MASTER_ACT	i2c0 status (master active status) This bit indicates whether I2C0 is active in the Master Mode. 1 : I2C0 is active. 0 : I2C0 is not active.	RO	0
12	I2C0_SLAVE_ACT	i2c0 status (slave active status) This bit indicates whether I2C0 is active in the Slave Mode. 1 : I2C0 is active. 0 : I2C0 is not active.	RO	0
11:9	Reserved	-	-	-
8:4	I2C0_MST_CSTATE	i2c0 status (master status) This bit indicates whether I2C0 is active in the Master Mode. Except 0x00 : I2C0 is active. 0x00 : I2C0 is idle.	RO	0x00
3:0	I2C0_SLV_CSTATE	i2c0 status (slave status) This bit indicates whether I2C0 is active in the Slave Mode. Except 0x0 : I2C0 is active. 0x0 : I2C0 is idle.	RO	0x0

5.5. I2C1_STAT

I2C1_STAT			
Description			
Address Region	gconf	**Type:**	RO
Offset	0x0000 0024		
Physical address View0	0x4004 A024		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:29	Reserved	-	-	-
28	I2C1_IC_EN	i2c1 status (i2c enable) [I2C1_IC_ENABLE].ENABLE bit is indicated. 1 : I2C1 is enabled. 0 : I2C1 is disabled.	RO	0
27:26	Reserved	-	-	-
25	I2C1_S_GEN	i2c1 status (start condition period) This bit indicates whether I2C1 is generating a START Condition on the I2C bus in the Master Mode. 1 : I2C1 is generating a START Condition. 0 : I2C1 is not generating a START Condition.	RO	0
24	I2C1_P_GEN	i2c1 status (stop condition period) This bit indicates whether I2C1 is generating a STOP Condition on the I2C bus in the Master Mode. 1 : I2C1 is generating a STOP Condition. 0 : I2C1 is not generating a STOP Condition.	RO	0
23:22	Reserved	-	-	-

21	I2C1_DATA	i2c1 status (data communication period) This bit indicates whether I2C1 is in the data phase on the I2C bus. 1 : I2C1 is in the data phase. 0 : I2C1 is not in the data phase.	RO	0
20	I2C1_ADDR	i2c1 status (address communication period) This bit indicates whether I2C1 is in the address phase on the I2C bus. 1 : I2C1 is in the address phase. 0 : I2C1 is not in the address phase.	RO	0
19:18	Reserved	-	-	-
17	I2C1_RD	i2c1 status (i2c read status) This bit indicates whether I2C1 is in a read transaction on the I2C bus in the Master Mode. 1 : I2C1 is in a read transaction. 0 : I2C1 is not in a read transaction.	RO	0
16	I2C1_WR	i2c1 status (i2c write status) This bit indicates whether I2C1 is in a write transaction on the I2C bus in the Master Mode. 1 : I2C1 is in a write transaction. 0 : I2C1 is not in a write transaction.	RO	0
15:14	Reserved	-	-	-
13	I2C1_MASTER_ACT	i2c1 status (master active status) This bit indicates whether I2C1 is active in the Master Mode. 1 : I2C1 is active. 0 : I2C1 is not active.	RO	0
12	I2C1_SLAVE_ACT	i2c1 status (slave active status) This bit indicates whether I2C1 is active in the Slave Mode. 1 : I2C1 is active. 0 : I2C1 is not active.	RO	0
11:9	Reserved	-	-	-
8:4	I2C1_MST_CSTATE	i2c1 status (master status) This bit indicates whether I2C1 is active in the Master Mode. Except 0x00 : I2C1 is active. 0x00 : I2C1 is idle.	RO	0x00
3:0	I2C1_SLV_CSTATE	i2c1 status (slave status) This bit indicates whether I2C1 is active in the Slave Mode. Except 0x0 : I2C1 is active. 0x0 : I2C1 is idle.	RO	0x0

5.6. I2C2_STAT

I2C2_STAT			
Description			
Address Region	gconf	**Type:**	RO
Offset	0x0000 0028		
Physical address View0	0x4004 A028		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:29	Reserved	-	-	-
28	I2C2_IC_EN	i2c2 status (i2c enable) [I2C2_IC_ENABLE].ENABLE bit is indicated. 1 : I2C2 is enabled. 0 : I2C2 is disabled.	RO	0
27:26	Reserved	-	-	-
25	I2C2_S_GEN	i2c2 status (start condition period) This bit indicates whether I2C2 is generating a START Condition on the I2C bus in the Master Mode. 1 : I2C2 is generating a START Condition. 0 : I2C2 is not generating a START Condition.	RO	0
24	I2C2_P_GEN	i2c2 status (stop condition period) This bit indicates whether I2C2 is generating a STOP Condition on the I2C bus in the Master Mode. 1 : I2C2 is generating a STOP Condition. 0 : I2C2 is not generating a STOP Condition.	RO	0
23:22	Reserved	-	-	-
21	I2C2_DATA	i2c2 status (data communication period) This bit indicates whether I2C2 is in the data phase on the I2C bus. 1 : I2C2 is in the data phase. 0 : I2C2 is not in the data phase.	RO	0
20	I2C2_ADDR	i2c2 status (address communication period) This bit indicates whether I2C2 is in the address phase on the I2C bus. 1 : I2C2 is in the address phase. 0 : I2C2 is not in the address phase.	RO	0
19:18	Reserved	-	-	-
17	I2C2_RD	i2c2 status (i2c read status) This bit indicates whether I2C2 is in a read transaction on the I2C bus in the Master Mode. 1 : I2C2 is in a read transaction. 0 : I2C2 is not in a read transaction.	RO	0
16	I2C2_WR	i2c2 status (i2c write status) This bit indicates whether I2C2 is in a write transaction on the I2C bus in the Master Mode. 1 : I2C2 is in a write transaction. 0 : I2C2 is not in a write transaction.	RO	0

15:14	Reserved	-	-	-
13	I2C2_MASTER_ACT	i2c2 status (master active status) This bit indicates whether I2C2 is active in the Master Mode. 1 : I2C2 is active. 0 : I2C2 is not active.	RO	0
12	I2C2_SLAVE_ACT	i2c2 status (slave active status) This bit indicates whether I2C2 is active in the Slave Mode. 1 : I2C2 is active. 0 : I2C2 is not active.	RO	0
11:9	Reserved	-	-	-
8:4	I2C2_MST_CSTATE	i2c2 status (master status) This bit indicates whether I2C2 is active in the Master Mode. Except 0x00 : I2C2 is active. 0x00 : I2C2 is idle.	RO	0x00
3:0	I2C2_SLV_CSTATE	i2c2 status (slave status) This bit indicates whether I2C2 is active in the Slave Mode. Except 0x00 : I2C2 is active. 0x00 : I2C2 is idle.	RO	0x0

5.7. SPIM0_SLEEP

SPIM0_SLEEP			
Description			
Address Region	gconf	**Type:**	RO
Offset	0x0000 0030		
Physical address View0	0x4004 A030		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	SPIM0_SLEEP	spim0 sleep status 1: Sleep 0: In operation	RO	1

5.8. SPIM1_SLEEP

SPIM1_SLEEP			
Description			
Address Region	gconf	**Type:**	RO
Offset	0x0000 0034		
Physical address View0	0x4004 A034		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	SPIM1_SLEEP	spim1 sleep status 1: Sleep 0: In operation	RO	1

5.9. SPIM2_SLEEP

SPIM2_SLEEP			
Description			
Address Region	gconf	**Type:**	RO
Offset	0x0000 0038		
Physical address View0	0x4004 A038		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	SPIM2_SLEEP	spim2 sleep status 1: Sleep 0: In operation	RO	1

5.10. SPIM3_SLEEP

SPIM3_SLEEP			
Description			
Address Region	gconf	**Type:**	RO
Offset	0x0000 003C		
Physical address View0	0x4004 A03C		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	SPIM3_SLEEP	spim3 sleep status 1: Sleep 0: In operation	RO	1

5.11. DMACREQ_SEL0

DMACREQ_SEL0			
Description			
Address Region	gconf	**Type:**	RW
Offset	0x0000 0040		
Physical address View0	0x4004 A040		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:6	Reserved	-	-	-
5:0	DMACREQ_SEL0	DMAC request signal selection (ch0) dma_req, dma_single, dma_ack: Set in the range of 0 to 35. dma_finish: Set in the range of 24 to 31. In any setting value other than above, the request signal (dma_req, dma_single) and response signal (dma_ack, dma_finish) cannot be used.	RW modify	0x3F

5.12. DMACREQ_SEL1

DMACREQ_SEL1				
Description				
Address Region	gconf	**Type:**	RW	
Offset	0x0000 0044			
Physical address View0	0x4004 A044			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:6	Reserved	-	-	-
5:0	DMACREQ_SEL1	DMAC request signal selection (ch1) dma_req, dma_single, dma_ack: Set in the range of 0 to 35. dma_finish: Set in the range of 24 to 31. In any setting value other than above, the request signal (dma_req, dma_single) and response signal (dma_ack, dma_finish) cannot be used.	RW modify	0x3F

5.13. DMACREQ_SEL2

DMACREQ_SEL2				
Description				
Address Region	gconf	**Type:**	RW	
Offset	0x0000 0048			
Physical address View0	0x4004 A048			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:6	Reserved	-	-	-
5:0	DMACREQ_SEL2	DMAC request signal selection (ch2) dma_req, dma_single, dma_ack: Set in the range of 0 to 35. dma_finish: Set in the range of 24 to 31. In any setting value other than above, the request signal (dma_req, dma_single) and response signal (dma_ack, dma_finish) cannot be used.	RW modify	0x3F

5.14. DMACREQ_SEL3

DMACREQ_SEL3				
Description				
Address Region	gconf	**Type:**	RW	
Offset	0x0000 004C			
Physical address View0	0x4004 A04C			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:6	Reserved	-	-	-
5:0	DMACREQ_SEL3	DMAC request signal selection (ch3) dma_req, dma_single, dma_ack: Set in the range of 0 to 35. dma_finish: Set in the range of 24 to 31. In any setting value other than above, the request signal (dma_req , dma_single) and response signal (dma_ack,dma_finish) cannot be used.	RW modify	0x3F

5.15. DMACREQ_SEL4

DMACREQ_SEL4				
Description				
Address Region	gconf	**Type:**	RW	
Offset	0x0000 0050			
Physical address View0	0x4004 A050			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:6	Reserved	-	-	-
5:0	DMACREQ_SEL4	DMAC request signal selection (ch4) dma_req, dma_single, dma_ack: Set in the range of 0 to 35. dma_finish: Set in the range of 24 to 31. In any setting value other than above, the request signal (dma_req, dma_single) and response signal (dma_ack, dma_finish) cannot be used.	RW modify	0x3F

5.16. DMACREQ_SEL5

DMACREQ_SEL5				
Description				
Address Region	gconf	**Type:**	RW	
Offset	0x0000 0054			
Physical address View0	0x4004 A054			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:6	Reserved	-	-	-
5:0	DMACREQ_SEL5	DMAC request signal selection (ch5) dma_req, dma_single, dma_ack: Set in the range of 0 to 35. dma_finish: Set in the range of 24 to 31. In any setting value other than above, the request signal (dma_req, dma_single) and response signal (dma_ack, dma_finish) cannot be used.	RW modify	0x3F

5.17. DMACREQ_SEL6

DMACREQ_SEL6				
Description				
Address Region	gconf	**Type:**	RW	
Offset	0x0000 0058			
Physical address View0	0x4004 A058			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:6	Reserved	-	-	-
5:0	DMACREQ_SEL6	DMAC request signal selection (ch6) dma_req, dma_single, dma_ack: Set in the range of 0 to 35. dma_finish: Set in the range of 24 to 31. In any setting value other than above, the request signal (dma_req, dma_single) and response signal (dma_ack, dma_finish) cannot be used.	RW modify	0x3F

5.18. DMACREQ_SEL7

DMACREQ_SEL7					
Description					
Address Region	gconf		**Type:**	RW	
Offset	0x0000 005C				
Physical address View0	0x4004 A05C				
Physical address View1	-				
Bitfield Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:6	Reserved	-		-	-
5:0	DMACREQ_SEL7	DMAC request signal selection (ch7) dma_req, dma_single, dma_ack: Set in the range of 0 to 35. dma_finish: Set in the range of 24 to 31. In any setting value other than above, the request signal (dma_req, dma_single) and response signal (dma_ack, dma_finish) cannot be used.		RW modify	0x3F

5.19. USB_FSIO_TUNE

USB_FSIO_TUNE					
Description					
Address Region	gconf		**Type:**	RW	
Offset	0x0000 0080				
Physical address View0	0x4004 A080				
Physical address View1	-				
Bitfield Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:16	Reserved	-		-	-
15:8	FSIO_XP	USB FSIO Tr/T adjustment (set our specification value.)		RW modify	0x0B
7:0	FSIO_RFM	USB FSIO Crosspoint adjustment (set our specification value.)		RW modify	0x3E

5.20. CPU_STCALIB

CPU_STCALIB					
Description					
Address Region	gconf		**Type:**	RW	
Offset	0x0000 00C0				
Physical address View0	0x4004 A0C0				
Physical address View1	-				
Bitfield Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:26	Reserved	-		-	-
25:0	CPU_STCALIB	System Tick calibration CPU [SYST_CALIB] register is set up by this register.		RW modify	0x000 0000

		[25] : [SYST_CALIB].NOREF [24] : [SYST_CALIB].SKEW [23:0] : [SYST_CALIB].TENMS		

5.21. CPU_TSENABLE

CPU_TSENABLE			
Description			
Address Region	gconf	**Type:**	RW
Offset	0x0000 00C4		
Physical address View0	0x4004 A0C4		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:1	Reserved	-	-	-
0	CPU_TSENABLE	Time Stamp count enable Control of the time stamp counter (48bit) of CPU Trace. It is counted by CPU HCLK. 1 : Count Enable 0 : Count Disable	RW modify	0

5.22. CPU_FPUIRQEN

CPU_FPUIRQEN			
Description			
Address Region	gconf	**Type:**	RW
Offset	0x0000 00CC		
Physical address View0	0x4004 A0CC		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:8	Reserved	-	-	-
7	CPU_FPUIDE	FPU IDC (Input Denormal cumulative) Exception Interrupt Enable 1: Interrupt Enable 0: Interrupt Disable	RW	0
6:5	Reserved	-	-	-
4	CPU_FPUIXE	FPU IXC (Inexact cumulative) Exception Interrupt Enable 1: Interrupt Enable 0: Interrupt Disable	RW	0
3	CPU_FPUUFE	FPU UFC (Underflow cumulative) Exception Interrupt Enable 1: Interrupt Enable 0: Interrupt Disable	RW	0
2	CPU_FPUOFE	FPU OFC (Overflow cumulative) Exception Interrupt Enable 1: Interrupt Enable 0: Interrupt Disable	RW	0
1	CPU_FPUDZE	FPU DZC (Division by Zero cumulative) Exception Interrupt Enable 1: Interrupt Enable 0: Interrupt Disable	RW	0

0	CPU_FPUIOE	FPU IOC(Invalid Operation cumulative) Exception Interrupt Enable 1: Interrupt Enable 0: Interrupt Disable	RW	0

5.23. CPU_DEBUGIN

CPU_DEBUGIN			
Description			
Address Region	gconf	**Type:**	RW
Offset	0x0000 00D0		
Physical address View0	0x4004 A0D0		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CPU_DEBUGIN	Debugger detection 1: Enable 0: Disable	RW modify	1

5.24. IO_CFG0

IO_CFG0			
Description			
Address Region	gconf	**Type:**	RW
Offset	0x0000 0100		
Physical address View0	0x4004 A100		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31	GPIO_7_CTL2	MCU_GPIO_7 IO cell CTL2 setting	RW modify	0
30	GPIO_7_CTL1	MCU_GPIO_7 IO cell CTL1 setting	RW modify	0
29	GPIO_7_PUD	MCU_GPIO_7 IO cell PUD setting	RW modify	0
28	GPIO_7_ENPUD	MCU_GPIO_7 IO cell ENPUD setting	RW modify	1
27	GPIO_6_CTL2	MCU_GPIO_6 IO cell CTL2 setting	RW modify	0
26	GPIO_6_CTL1	MCU_GPIO_6 IO cell CTL1 setting	RW modify	0
25	GPIO_6_PUD	MCU_GPIO_6 IO cell PUD setting	RW modify	0
24	GPIO_6_ENPUD	MCU_GPIO_6 IO cell ENPUD setting	RW modify	1
23	GPIO_5_CTL2	MCU_GPIO_5 IO cell CTL2 setting	RW modify	0
22	GPIO_5_CTL1	MCU_GPIO_5 IO cell CTL1 setting	RW modify	0
21	GPIO_5_PUD	MCU_GPIO_5 IO cell PUD setting	RW modify	0
20	GPIO_5_ENPUD	MCU_GPIO_5 IO cell ENPUD setting	RW	1

			modify	
19	GPIO_4_CTL2	MCU_GPIO_4 IO cell CTL2 setting	RW modify	0
18	GPIO_4_CTL1	MCU_GPIO_4 IO cell CTL1 setting	RW modify	0
17	GPIO_4_PUD	MCU_GPIO_4 IO cell PUD setting	RW modify	0
16	GPIO_4_ENPUD	MCU_GPIO_4 IO cell ENPUD setting	RW modify	1
15	GPIO_3_CTL2	MCU_GPIO_3 IO cell CTL2 setting	RW modify	0
14	GPIO_3_CTL1	MCU_GPIO_3 IO cell CTL1 setting	RW modify	0
13	GPIO_3_PUD	MCU_GPIO_3 IO cell PUD setting	RW modify	0
12	GPIO_3_ENPUD	MCU_GPIO_3 IO cell ENPUD setting	RW modify	1
11	GPIO_2_CTL2	MCU_GPIO_2 IO cell CTL2 setting	RW modify	0
10	GPIO_2_CTL1	MCU_GPIO_2 IO cell CTL1 setting	RW modify	0
9	GPIO_2_PUD	MCU_GPIO_2 IO cell PUD setting	RW modify	0
8	GPIO_2_ENPUD	MCU_GPIO_2 IO cell ENPUD setting	RW modify	1
7	GPIO_1_CTL2	MCU_GPIO_1 IO cell CTL2 setting	RW modify	0
6	GPIO_1_CTL1	MCU_GPIO_1 IO cell CTL1 setting	RW modify	0
5	GPIO_1_PUD	MCU_GPIO_1 IO cell PUD setting	RW modify	0
4	GPIO_1_ENPUD	MCU_GPIO_1 IO cell ENPUD setting	RW modify	1
3:0	Reserved	-	-	-

5.25. IO_CFG1

IO_CFG1			
Description			
Address Region	gconf	**Type:**	RW
Offset	0x0000 0104		
Physical address View0	0x4004 A104		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31	GPIO_15_CTL2	MCU_GPIO_15 IO cell CTL2 setting	RW modify	0
30	GPIO_15_CTL1	MCU_GPIO_15 IO cell CTL1 setting	RW modify	0
29	GPIO_15_PUD	MCU_GPIO_15 IO cell PUD setting	RW modify	0
28	GPIO_15_ENPUD	MCU_GPIO_15 IO cell ENPUD setting	RW modify	1
27	GPIO_14_CTL2	MCU_GPIO_14 IO cell CTL2 setting	RW modify	0
26	GPIO_14_CTL1	MCU_GPIO_14 IO cell CTL1 setting	RW modify	0

25	GPIO_14_PUD	MCU_GPIO_14 IO cell PUD setting	RW modify	0
24	GPIO_14_ENPUD	MCU_GPIO_14 IO cell ENPUD setting	RW modify	1
23	GPIO_13_CTL2	MCU_GPIO_13 IO cell CTL2 setting	RW modify	0
22	GPIO_13_CTL1	MCU_GPIO_13 IO cell CTL1 setting	RW modify	0
21	GPIO_13_PUD	MCU_GPIO_13 IO cell PUD setting	RW modify	0
20	GPIO_13_ENPUD	MCU_GPIO_13 IO cell ENPUD setting	RW modify	1
19	GPIO_12_CTL2	MCU_GPIO_12 IO cell CTL2 setting	RW modify	0
18	GPIO_12_CTL1	MCU_GPIO_12 IO cell CTL1 setting	RW modify	0
17	GPIO_12_PUD	MCU_GPIO_12 IO cell PUD setting	RW modify	0
16	GPIO_12_ENPUD	MCU_GPIO_12 IO cell ENPUD setting	RW modify	1
15	GPIO_11_CTL2	MCU_GPIO_11 IO cell CTL2 setting	RW modify	0
14	GPIO_11_CTL1	MCU_GPIO_11 IO cell CTL1 setting	RW modify	0
13	GPIO_11_PUD	MCU_GPIO_11 IO cell PUD setting	RW modify	0
12	GPIO_11_ENPUD	MCU_GPIO_11 IO cell ENPUD setting	RW modify	1
11	GPIO_10_CTL2	MCU_GPIO_10 IO cell CTL2 setting	RW modify	0
10	GPIO_10_CTL1	MCU_GPIO_10 IO cell CTL1 setting	RW modify	0
9	GPIO_10_PUD	MCU_GPIO_10 IO cell PUD setting	RW modify	0
8	GPIO_10_ENPUD	MCU_GPIO_10 IO cell ENPUD setting	RW modify	1
7	GPIO_9_CTL2	MCU_GPIO_9 IO cell CTL2 setting	RW modify	0
6	GPIO_9_CTL1	MCU_GPIO_9 IO cell CTL1 setting	RW modify	0
5	GPIO_9_PUD	MCU_GPIO_9 IO cell PUD setting	RW modify	0
4	GPIO_9_ENPUD	MCU_GPIO_9 IO cell ENPUD setting	RW modify	1
3	GPIO_8_CTL2	MCU_GPIO_8 IO cell CTL2 setting	RW modify	0
2	GPIO_8_CTL1	MCU_GPIO_8 IO cell CTL1 setting	RW modify	0
1	GPIO_8_PUD	MCU_GPIO_8 IO cell PUD setting	RW modify	0
0	GPIO_8_ENPUD	MCU_GPIO_8 IO cell ENPUD setting	RW modify	1

5.26. IO_CFG2

IO_CFG2			
Description			
Address Region	gconf	**Type:**	RO
Offset	0x0000 0108		
Physical address View0	0x4004 A108		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:0	Reserved	-	-	-

5.27. IO_CFG3

IO_CFG3			
Description			
Address Region	gconf	**Type:**	RW
Offset	0x0000 010C		
Physical address View0	0x4004 A10C		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31	GPIO_31_CTL2	MCU_GPIO_31 IO cell CTL2 setting	RW modify	0
30	GPIO_31_CTL1	MCU_GPIO_31 IO cell CTL1 setting	RW modify	0
29	GPIO_31_PUD	MCU_GPIO_31 IO cell PUD setting	RW modify	0
28	GPIO_31_ENPUD	MCU_GPIO_31 IO cell ENPUD setting	RW modify	1
27	GPIO_30_CTL2	MCU_GPIO_30 IO cell CTL2 setting	RW modify	0
26	GPIO_30_CTL1	MCU_GPIO_30 IO cell CTL1 setting	RW modify	0
25	GPIO_30_PUD	MCU_GPIO_30 IO cell PUD setting	RW modify	0
24	GPIO_30_ENPUD	MCU_GPIO_30 IO cell ENPUD setting	RW modify	1
23	GPIO_29_CTL2	MCU_GPIO_29 IO cell CTL2 setting	RW modify	0
22	GPIO_29_CTL1	MCU_GPIO_29 IO cell CTL1 setting	RW modify	0
21	GPIO_29_PUD	MCU_GPIO_29 IO cell PUD setting	RW modify	0
20	GPIO_29_ENPUD	MCU_GPIO_29 IO cell ENPUD setting	RW modify	1
19	GPIO_28_CTL2	MCU_GPIO_28 IO cell CTL2 setting	RW modify	0
18	GPIO_28_CTL1	MCU_GPIO_28 IO cell CTL1 setting	RW modify	0
17	GPIO_28_PUD	MCU_GPIO_28 IO cell PUD setting	RW modify	0

16	GPIO_28_ENPUD	MCU_GPIO_28 IO cell ENPUD setting	RW modify	0
15	GPIO_27_CTL2	MCU_GPIO_27 IO cell CTL2 setting	RW modify	0
14	GPIO_27_CTL1	MCU_GPIO_27 IO cell CTL1 setting	RW modify	0
13	GPIO_27_PUD	MCU_GPIO_27 IO cell PUD setting	RW modify	0
12	GPIO_27_ENPUD	MCU_GPIO_27 IO cell ENPUD setting	RW modify	1
11	GPIO_26_CTL2	MCU_GPIO_26 IO cell CTL2 setting	RW modify	0
10	GPIO_26_CTL1	MCU_GPIO_26 IO cell CTL1 setting	RW modify	0
9	GPIO_26_PUD	MCU_GPIO_26 IO cell PUD setting	RW modify	0
8	GPIO_26_ENPUD	MCU_GPIO_26 IO cell ENPUD setting	RW modify	1
7	GPIO_25_CTL2	MCU_GPIO_25 IO cell CTL2 setting	RW modify	0
6	GPIO_25_CTL1	MCU_GPIO_25 IO cell CTL1 setting	RW modify	0
5	GPIO_25_PUD	MCU_GPIO_25 IO cell PUD setting	RW modify	0
4	GPIO_25_ENPUD	MCU_GPIO_25 IO cell ENPUD setting	RW modify	1
3	GPIO_24_CTL2	MCU_GPIO_24 IO cell CTL2 setting	RW modify	0
2	GPIO_24_CTL1	MCU_GPIO_24 IO cell CTL1 setting	RW modify	0
1	GPIO_24_PUD	MCU_GPIO_24 IO cell PUD setting	RW modify	0
0	GPIO_24_ENPUD	MCU_GPIO_24 IO cell ENPUD setting	RW modify	1

5.28. IO_CFG4

IO_CFG4			
Description			
Address Region	gconf	**Type:**	RW
Offset	0x0000 0110		
Physical address View0	0x4004 A110		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:24	Reserved	-	-	-
23	I2C2_CLK_CTL2	MCU_I2C2_CLK IO cell CTL2 setting	RW modify	0
22	I2C2_CLK_CTL1	MCU_I2C2_CLK IO cell CTL1 setting	RW modify	0
21:20	Reserved	-	-	-
19	I2C2_DATA_CTL2	MCU_I2C2_DATA IO cell CTL2 setting	RW modify	0
18	I2C2_DATA_CTL1	MCU_I2C2_DATA IO cell CTL1 setting	RW modify	0
17:16	Reserved	-	-	-

15	I2C1_CLK_CTL2	MCU_I2C1_CLK IO cell CTL2 setting	RW modify	0
14	I2C1_CLK_CTL1	MCU_I2C1_CLK IO cell CTL1 setting	RW modify	0
13	I2C1_CLK_PUD	MCU_I2C1_CLK IO cell PUD setting	RW modify	0
12	I2C1_CLK_ENPUD	MCU_I2C1_CLK IO cell ENPUD setting	RW modify	1
11	I2C1_DATA_CTL2	MCU_I2C1_DATA IO cell CTL2 setting	RW modify	0
10	I2C1_DATA_CTL1	MCU_I2C1_DATA IO cell CTL1 setting	RW modify	0
9	I2C1_DATA_PUD	MCU_I2C1_DATA IO cell PUD setting	RW modify	0
8	I2C1_DATA_ENPUD	MCU_I2C1_DATA IO cell ENPUD setting	RW modify	1
7	I2C0_CLK_CTL2	MCU_I2C0_CLK IO cell CTL2 setting	RW modify	0
6	I2C0_CLK_CTL1	MCU_I2C0_CLK IO cell CTL1 setting	RW modify	0
5	I2C0_CLK_PUD	MCU_I2C0_CLK IO cell PUD setting	RW modify	0
4	I2C0_CLK_ENPUD	MCU_I2C0_CLK IO cell ENPUD setting	RW modify	1
3	I2C0_DATA_CTL2	MCU_I2C0_DATA IO cell CTL2 setting	RW modify	0
2	I2C0_DATA_CTL1	MCU_I2C0_DATA IO cell CTL1 setting	RW modify	0
1	I2C0_DATA_PUD	MCU_I2C0_DATA IO cell PUD setting	RW modify	0
0	I2C0_DATA_ENPUD	MCU_I2C0_DATA IO cell ENPUD setting	RW modify	1

5.29. IO_CFG5

IO_CFG5			
Description			
Address Region	gconf	**Type:**	RW
Offset	0x0000 0114		
Physical address View0	0x4004 A114		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31	UA1_CTS_N_CTL2	MCU_UA1_CTS_N IO cell CTL2 setting	RW modify	0
30	UA1_CTS_N_CTL1	MCU_UA1_CTS_N IO cell CTL1 setting	RW modify	0
29	UA1_CTS_N_PUD	MCU_UA1_CTS_N IO cell PUD setting	RW modify	0
28	UA1_CTS_N_ENPUD	MCU_UA1_CTS_N IO cell ENPUD setting	RW modify	1
27	UA1_RTS_N_CTL2	MCU_UA1_RTS_N IO cell CTL2 setting	RW modify	0
26	UA1_RTS_N_CTL1	MCU_UA1_RTS_N IO cell CTL1 setting	RW modify	0
25	UA1_RTS_N_PUD	MCU_UA1_RTS_N IO cell PUD setting	RW modify	0

24	UA1_RTS_N_ENPUD	MCU_UA1_RTS_N IO cell ENPUD setting	RW modify	1
23	UA1_TXD_CTL2	MCU_UA1_TXD IO cell CTL2 setting	RW modify	0
22	UA1_TXD_CTL1	MCU_UA1_TXD IO cell CTL1 setting	RW modify	0
21	UA1_TXD_PUD	MCU_UA1_TXD IO cell PUD setting	RW modify	0
20	UA1_TXD_ENPUD	MCU_UA1_TXD IO cell ENPUD setting	RW modify	1
19	UA1_RXD_CTL2	MCU_UA1_RXD IO cell CTL2 setting	RW modify	0
18	UA1_RXD_CTL1	MCU_UA1_RXD IO cell CTL1 setting	RW modify	0
17	UA1_RXD_PUD	MCU_UA1_RXD IO cell PUD setting	RW modify	0
16	UA1_RXD_ENPUD	MCU_UA1_RXD IO cell ENPUD setting	RW modify	1
15:8	Reserved	-	-	-
7	UA0_TXD_CTL2	MCU_UA0_TXD IO cell CTL2 setting	RW modify	0
6	UA0_TXD_CTL1	MCU_UA0_TXD IO cell CTL1 setting	RW modify	0
5	UA0_TXD_PUD	MCU_UA0_TXD IO cell PUD setting	RW modify	0
4	UA0_TXD_ENPUD	MCU_UA0_TXD IO cell ENPUD setting	RW modify	1
3	UA0_RXD_CTL2	MCU_UA0_RXD IO cell CTL2 setting	RW modify	0
2	UA0_RXD_CTL1	MCU_UA0_RXD IO cell CTL1 setting	RW modify	0
1	UA0_RXD_PUD	MCU_UA0_RXD IO cell PUD setting	RW modify	0
0	UA0_RXD_ENPUD	MCU_UA0_RXD IO cell ENPUD setting	RW modify	1

5.30. IO_CFG6

IO_CFG6			
Description			
Address Region	gconf	**Type:**	RW
Offset	0x0000 0118		
Physical address View0	0x4004 A118		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:16	Reserved	-	-	-
15	UA2_CTS_N_CTL2	MCU_UA2_CTS_N IO cell CTL2 setting	RW modify	0
14	UA2_CTS_N_CTL1	MCU_UA2_CTS_N IO cell CTL1 setting	RW modify	0
13	UA2_CTS_N_PUD	MCU_UA2_CTS_N IO cell PUD setting	RW modify	0
12	UA2_CTS_N_ENPUD	MCU_UA2_CTS_N IO cell ENPUD setting	RW modify	1
11	UA2_RTS_N_CTL2	MCU_UA2_RTS_N IO cell CTL2 setting	RW modify	0

10	UA2_RTS_N_CTL1	MCU_UA2_RTS_N IO cell CTL1 setting	RW modify	0
9	UA2_RTS_N_PUD	MCU_UA2_RTS_N IO cell PUD setting	RW modify	0
8	UA2_RTS_N_ENPUD	MCU_UA2_RTS_N IO cell ENPUD setting	RW modify	1
7	UA2_TXD_CTL2	MCU_UA2_TXD IO cell CTL2 setting	RW modify	0
6	UA2_TXD_CTL1	MCU_UA2_TXD IO cell CTL1 setting	RW modify	0
5	UA2_TXD_PUD	MCU_UA2_TXD IO cell PUD setting	RW modify	0
4	UA2_TXD_ENPUD	MCU_UA2_TXD IO cell ENPUD setting	RW modify	1
3	UA2_RXD_CTL2	MCU_UA2_RXD IO cell CTL2 setting	RW modify	0
2	UA2_RXD_CTL1	MCU_UA2_RXD IO cell CTL1 setting	RW modify	0
1	UA2_RXD_PUD	MCU_UA2_RXD IO cell PUD setting	RW modify	0
0	UA2_RXD_ENPUD	MCU_UA2_RXD IO cell ENPUD setting	RW modify	1

5.31. IO_CFG7

IO_CFG7			
Description			
Address Region	gconf	**Type:**	RW
Offset	0x0000 011C		
Physical address View0	0x4004 A11C		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31	SPIM1_MISO_CTL2	MCU_SPIM1_MISO IO cell CTL2 setting	RW modify	0
30	SPIM1_MISO_CTL1	MCU_SPIM1_MISO IO cell CTL1 setting	RW modify	0
29	SPIM1_MISO_PUD	MCU_SPIM1_MISO IO cell PUD setting	RW modify	0
28	SPIM1_MISO_ENPUD	MCU_SPIM1_MISO IO cell ENPUD setting	RW modify	1
27	SPIM1_MOSI_CTL2	MCU_SPIM1_MOSI IO cell CTL2 setting	RW modify	0
26	SPIM1_MOSI_CTL1	MCU_SPIM1_MOSI IO cell CTL1 setting	RW modify	0
25	SPIM1_MOSI_PUD	MCU_SPIM1_MOSI IO cell PUD setting	RW modify	0
24	SPIM1_MOSI_ENPUD	MCU_SPIM1_MOSI IO cell ENPUD setting	RW modify	1
23	SPIM1_CLK_CTL2	MCU_SPIM1_CLK IO cell CTL2 setting	RW modify	0
22	SPIM1_CLK_CTL1	MCU_SPIM1_CLK IO cell CTL1 setting	RW modify	0
21	SPIM1_CLK_PUD	MCU_SPIM1_CLK IO cell PUD setting	RW modify	0
20	SPIM1_CLK_ENPUD	MCU_SPIM1_CLK IO cell ENPUD setting	RW modify	1

19	SPIM1_CS_N_CTL2	MCU_SPIM1_CS_N IO cell CTL2 setting	RW modify	0
18	SPIM1_CS_N_CTL1	MCU_SPIM1_CS_N IO cell CTL1 setting	RW modify	0
17	SPIM1_CS_N_PUD	MCU_SPIM1_CS_N IO cell PUD setting	RW modify	0
16	SPIM1_CS_N_ENPUD	MCU_SPIM1_CS_N IO cell ENPUD setting	RW modify	1
15	SPIM0_MISO_CTL2	MCU_SPIM0_MISO IO cell CTL2 setting	RW modify	0
14	SPIM0_MISO_CTL1	MCU_SPIM0_MISO IO cell CTL1 setting	RW modify	0
13	SPIM0_MISO_PUD	MCU_SPIM0_MISO IO cell PUD setting	RW modify	0
12	SPIM0_MISO_ENPUD	MCU_SPIM0_MISO IO cell ENPUD setting	RW modify	1
11	SPIM0_MOSI_CTL2	MCU_SPIM0_MOSI IO cell CTL2 setting	RW modify	0
10	SPIM0_MOSI_CTL1	MCU_SPIM0_MOSI IO cell CTL1 setting	RW modify	0
9	SPIM0_MOSI_PUD	MCU_SPIM0_MOSI IO cell PUD setting	RW modify	0
8	SPIM0_MOSI_ENPUD	MCU_SPIM0_MOSI IO cell ENPUD setting	RW modify	1
7	SPIM0_CLK_CTL2	MCU_SPIM0_CLK IO cell CTL2 setting	RW modify	0
6	SPIM0_CLK_CTL1	MCU_SPIM0_CLK IO cell CTL1 setting	RW modify	0
5	SPIM0_CLK_PUD	MCU_SPIM0_CLK IO cell PUD setting	RW modify	0
4	SPIM0_CLK_ENPUD	MCU_SPIM0_CLK IO cell ENPUD setting	RW modify	1
3	SPIM0_CS_N_CTL2	MCU_SPIM0_CS_N IO cell CTL2 setting	RW modify	0
2	SPIM0_CS_N_CTL1	MCU_SPIM0_CS_N IO cell CTL1 setting	RW modify	0
1	SPIM0_CS_N_PUD	MCU_SPIM0_CS_N IO cell PUD setting	RW modify	0
0	SPIM0_CS_N_ENPUD	MCU_SPIM0_CS_N IO cell ENPUD setting	RW modify	1

5.32. IO_CFG8

IO_CFG8			
Description			
Address Region	gconf	**Type:**	RW
Offset	0x0000 0120		
Physical address View0	0x4004 A120		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31	SPIM3_MISO_CTL2	MCU_SPIM3_MISO IO cell CTL2 setting	RW modify	0
30	SPIM3_MISO_CTL1	MCU_SPIM3_MISO IO cell CTL1 setting	RW modify	0
29	SPIM3_MISO_PUD	MCU_SPIM3_MISO IO cell PUD setting	RW modify	0

28	SPIM3_MISO_ENPUD	MCU_SPIM3_MISO IO cell ENPUD setting	RW modify	1
27	SPIM3_MOSI_CTL2	MCU_SPIM3_MOSI IO cell CTL2 setting	RW modify	0
26	SPIM3_MOSI_CTL1	MCU_SPIM3_MOSI IO cell CTL1 setting	RW modify	0
25	SPIM3_MOSI_PUD	MCU_SPIM3_MOSI IO cell PUD setting	RW modify	0
24	SPIM3_MOSI_ENPUD	MCU_SPIM3_MOSI IO cell ENPUD setting	RW modify	1
23	SPIM3_CLK_CTL2	MCU_SPIM3_CLK IO cell CTL2 setting	RW modify	0
22	SPIM3_CLK_CTL1	MCU_SPIM3_CLK IO cell CTL1 setting	RW modify	0
21	SPIM3_CLK_PUD	MCU_SPIM3_CLK IO cell PUD setting	RW modify	0
20	SPIM3_CLK_ENPUD	MCU_SPIM3_CLK IO cell ENPUD setting	RW modify	1
19	SPIM3_CS_N_CTL2	MCU_SPIM3_CS_N IO cell CTL2 setting	RW modify	0
18	SPIM3_CS_N_CTL1	MCU_SPIM3_CS_N IO cell CTL1 setting	RW modify	0
17	SPIM3_CS_N_PUD	MCU_SPIM3_CS_N IO cell PUD setting	RW modify	0
16	SPIM3_CS_N_ENPUD	MCU_SPIM3_CS_N IO cell ENPUD setting	RW modify	1
15	SPIM2_MISO_CTL2	MCU_SPIM2_MISO IO cell CTL2 setting	RW modify	0
14	SPIM2_MISO_CTL1	MCU_SPIM2_MISO IO cell CTL1 setting	RW modify	0
13	SPIM2_MISO_PUD	MCU_SPIM2_MISO IO cell PUD setting	RW modify	0
12	SPIM2_MISO_ENPUD	MCU_SPIM2_MISO IO cell ENPUD setting	RW modify	1
11	SPIM2_MOSI_CTL2	MCU_SPIM2_MOSI IO cell CTL2 setting	RW modify	0
10	SPIM2_MOSI_CTL1	MCU_SPIM2_MOSI IO cell CTL1 setting	RW modify	0
9	SPIM2_MOSI_PUD	MCU_SPIM2_MOSI IO cell PUD setting	RW modify	0
8	SPIM2_MOSI_ENPUD	MCU_SPIM2_MOSI IO cell ENPUD setting	RW modify	1
7	SPIM2_CLK_CTL2	MCU_SPIM2_CLK IO cell CTL2 setting	RW modify	0
6	SPIM2_CLK_CTL1	MCU_SPIM2_CLK IO cell CTL1 setting	RW modify	0
5	SPIM2_CLK_PUD	MCU_SPIM2_CLK IO cell PUD setting	RW modify	0
4	SPIM2_CLK_ENPUD	MCU_SPIM2_CLK IO cell ENPUD setting	RW modify	1
3	SPIM2_CS_N_CTL2	MCU_SPIM2_CS_N IO cell CTL2 setting	RW modify	0
2	SPIM2_CS_N_CTL1	MCU_SPIM2_CS_N IO cell CTL1 setting	RW modify	0
1	SPIM2_CS_N_PUD	MCU_SPIM2_CS_N IO cell PUD setting	RW modify	0
0	SPIM2_CS_N_ENPUD	MCU_SPIM2_CS_N IO cell ENPUD setting	RW modify	1

5.33. IO_CFG9

IO_CFG9			
Description			
Address Region	gconf	**Type:**	RW
Offset	0x0000 0124		
Physical address View0	0x4004 A124		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:24	Reserved	-	-	-
23	SPIC_IO3_CTL2	MCU_SPIC_IO3 IO cell CTL2 setting	RW modify	1
22	SPIC_IO3_CTL1	MCU_SPIC_IO3 IO cell CTL1 setting	RW modify	1
21	SPIC_IO3_PUD	MCU_SPIC_IO3 IO cell PUD setting	RW modify	1
20	SPIC_IO3_ENPUD	MCU_SPIC_IO3 IO cell ENPUD setting	RW modify	0
19	SPIC_IO2_CTL2	MCU_SPIC_IO2 IO cell CTL2 setting	RW modify	1
18	SPIC_IO2_CTL1	MCU_SPIC_IO2 IO cell CTL1 setting	RW modify	1
17	SPIC_IO2_PUD	MCU_SPIC_IO2 IO cell PUD setting	RW modify	1
16	SPIC_IO2_ENPUD	MCU_SPIC_IO2 IO cell ENPUD setting	RW modify	0
15	SPIC_MISO_CTL2	MCU_SPIC_MISO IO cell CTL2 setting	RW modify	1
14	SPIC_MISO_CTL1	MCU_SPIC_MISO IO cell CTL1 setting	RW modify	1
13	SPIC_MISO_PUD	MCU_SPIC_MISO IO cell PUD setting	RW modify	1
12	SPIC_MISO_ENPUD	MCU_SPIC_MISO IO cell ENPUD setting	RW modify	0
11	SPIC_MOSI_CTL2	MCU_SPIC_MOSI IO cell CTL2 setting	RW modify	1
10	SPIC_MOSI_CTL1	MCU_SPIC_MOSI IO cell CTL1 setting	RW modify	1
9	SPIC_MOSI_PUD	MCU_SPIC_MOSI IO cell PUD setting	RW modify	1
8	SPIC_MOSI_ENPUD	MCU_SPIC_MOSI IO cell ENPUD setting	RW modify	0
7	SPIC_CLK_CTL2	MCU_SPIC_CLK IO cell CTL2 setting	RW modify	1
6	SPIC_CLK_CTL1	MCU_SPIC_CLK IO cell CTL1 setting	RW modify	1
5	SPIC_CLK_PUD	MCU_SPIC_CLK IO cell PUD setting	RW modify	0
4	SPIC_CLK_ENPUD	MCU_SPIC_CLK IO cell ENPUD setting	RW modify	0
3	SPIC_CS_N_CTL2	MCU_SPIC_CS_N IO cell CTL2 setting	RW modify	1
2	SPIC_CS_N_CTL1	MCU_SPIC_CS_N IO cell CTL1 setting	RW modify	1
1	SPIC_CS_N_PUD	MCU_SPIC_CS_N IO cell PUD setting	RW modify	1
0	SPIC_CS_N_ENPUD	MCU_SPIC_CS_N IO cell ENPUD setting	RW modify	0

5.34. IO_CFG10

IO_CFG10			
Description			
Address Region	gconf	**Type:**	RW
Offset	0x0000 0128		
Physical address View0	0x4004 A128		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:4	Reserved	-	-	-
3	ADC24_SYNC_CTL2	MCU_ADC24_SYNC IO cell CTL2 setting	RW modify	0
2	ADC24_SYNC_CTL1	MCU_ADC24_SYNC IO cell CTL1 setting	RW modify	0
1	ADC24_SYNC_PUD	MCU_ADC24_SYNC IO cell PUD setting	RW modify	0
0	ADC24_SYNC_ENPUD	MCU_ADC24_SYNC IO cell ENPUD setting	RW modify	1

5.35. IO_CFG11

IO_CFG11			
Description			
Address Region	gconf	**Type:**	RW
Offset	0x0000 012C		
Physical address View0	0x4004 A12C		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:4	Reserved	-	-	-
3	DBG_CTL2	MCU_DBG_* IO cell CTL2 setting	RW modify	0
2	DBG_CTL1	MCU_DBG_* IO cell CTL1 setting	RW modify	0
1:0	Reserved	-	-	-

5.36. FMODE_CFG0

FMODE_CFG0			
Description	For details on Function Mode, see "Datasheet Summary 5.1 Setting Multiple function I/O".		
Address Region	gconf	**Type:**	RW
Offset	0x0000 0140		
Physical address View0	0x4004 A140		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:30	GPIO_15_FMODE	MCU_GPIO_15 Function Mode setting	RW modify	0x0
29:28	GPIO_14_FMODE	MCU_GPIO_14 Function Mode setting	RW modify	0x0
27:26	GPIO_13_FMODE	MCU_GPIO_13 Function Mode setting	RW modify	0x0
25:24	GPIO_12_FMODE	MCU_GPIO_12 Function Mode setting	RW modify	0x0
23:22	GPIO_11_FMODE	MCU_GPIO_11 Function Mode setting	RW modify	0x0
21:20	GPIO_10_FMODE	MCU_GPIO_10 Function Mode setting	RW modify	0x0
19:18	GPIO_9_FMODE	MCU_GPIO_9 Function Mode setting	RW modify	0x0
17:16	GPIO_8_FMODE	MCU_GPIO_8 Function Mode setting	RW modify	0x0
15:14	GPIO_7_FMODE	MCU_GPIO_7 Function Mode setting	RW modify	0x0
13:12	GPIO_6_FMODE	MCU_GPIO_6 Function Mode setting	RW modify	0x0
11:10	GPIO_5_FMODE	MCU_GPIO_5 Function Mode setting	RW modify	0x0
9:8	GPIO_4_FMODE	MCU_GPIO_4 Function Mode setting	RW modify	0x0
7:6	GPIO_3_FMODE	MCU_GPIO_3 Function Mode setting	RW modify	0x0
5:4	GPIO_2_FMODE	MCU_GPIO_2 Function Mode setting	RW modify	0x0
3:2	GPIO_1_FMODE	MCU_GPIO_1 Function Mode setting	RW modify	0x0
1:0	GPIO_0_FMODE	MCU_GPIO_0 Function Mode setting	RW modify	0x0

5.37. FMODE_CFG1

FMODE_CFG1			
Description	For details on Function Mode, see "Datasheet Summary 5.1 Setting Multiple function I/O".		
Address Region	gconf	**Type:**	RW
Offset	0x0000 0144		
Physical address View0	0x4004 A144		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:30	GPIO_31_FMODE	MCU_GPIO_31 Function Mode setting	RW modify	0x0
29:28	GPIO_30_FMODE	MCU_GPIO_30 Function Mode setting	RW modify	0x0
27:26	GPIO_29_FMODE	MCU_GPIO_29 Function Mode setting	RW modify	0x0
25:24	GPIO_28_FMODE	MCU_GPIO_28 Function Mode setting	RW modify	0x0
23:22	GPIO_27_FMODE	MCU_GPIO_27 Function Mode setting	RW modify	0x0
21:20	GPIO_26_FMODE	MCU_GPIO_26 Function Mode setting	RW modify	0x0
19:18	GPIO_25_FMODE	MCU_GPIO_25 Function Mode setting	RW modify	0x0
17:16	GPIO_24_FMODE	MCU_GPIO_24 Function Mode setting	RW modify	0x0
15:0	Reserved	-	-	-

5.38. FMODE_CFG2

FMODE_CFG2			
Description	For details on Function Mode, see "Datasheet Summary 5.1 Setting Multiple function I/O".		
Address Region	gconf	**Type:**	RW
Offset	0x0000 0148		
Physical address View0	0x4004 A148		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:10	Reserved	-	-	-
9:8	I2C2_FMODE	MCU_I2C2_* Function Mode setting	RW modify	0x0
7:6	I2C1_CLK_FMODE	MCU_I2C1_CLK Function Mode setting	RW modify	0x0
5:4	I2C1_DATA_FMODE	MCU_I2C1_DATA Function Mode setting	RW modify	0x0
3:2	I2C0_CLK_FMODE	MCU_I2C0_CLK Function Mode setting	RW modify	0x0
1:0	I2C0_DATA_FMODE	MCU_I2C0_DATA Function Mode setting	RW modify	0x0

5.39. FMODE_CFG3

FMODE_CFG3			
Description	For details on Function Mode, see "Datasheet Summary 5.1 Setting Multiple function I/O".		
Address Region	gconf	**Type:**	RW
Offset	0x0000 014C		
Physical address View0	0x4004 A14C		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:24	Reserved	-	-	-
23:22	UA2_CTS_N_FMODE	MCU_UA2_CTS_N Function Mode setting	RW modify	0x0
21:20	UA2_RTS_N_FMODE	MCU_UA2_RTS_N Function Mode setting	RW modify	0x0
19:18	UA2_TXD_FMODE	MCU_UA2_TXD Function Mode setting	RW modify	0x0
17:16	UA2_RXD_FMODE	MCU_UA2_RXD Function Mode setting	RW modify	0x0
15:14	UA1_CTS_N_FMODE	MCU_UA1_CTS_N Function Mode setting	RW modify	0x0
13:12	UA1_RTS_N_FMODE	MCU_UA1_RTS_N Function Mode setting	RW modify	0x0
11:10	UA1_TXD_FMODE	MCU_UA1_TXD Function Mode setting	RW modify	0x0
9:8	UA1_RXD_FMODE	MCU_UA1_RXD Function Mode setting	RW modify	0x0
7:4	Reserved	-	-	-
3:2	UA0_TXD_FMODE	MCU_UA0_TXD Function Mode setting	RW modify	0x0
1:0	UA0_RXD_FMODE	MCU_UA0_RXD Function Mode setting	RW modify	0x0

5.40. FMODE_CFG4

FMODE_CFG4			
Description	For details on Function Mode, see "Datasheet Summary 5.1 Setting Multiple function I/O".		
Address Region	gconf	**Type:**	RW
Offset	0x0000 0150		
Physical address View0	0x4004 A150		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:26	Reserved	-	-	-
25:24	SPIM3_FMODE	MCU_SPIM3_* Function Mode setting	RW modify	0x0
23:18	Reserved	-	-	-
17:16	SPIM2_FMODE	MCU_SPIM2_* Function Mode setting	RW modify	0x0
15:14	SPIM1_MISO_FMODE	MCU_SPIM1_MISO Function Mode setting	RW modify	0x0

13:12	SPIM1_MOSI_FMODE	MCU_SPIM1_MOSI Function Mode setting	RW modify	0x0
11:10	SPIM1_CLK_FMODE	MCU_SPIM1_CLK Function Mode setting	RW modify	0x0
9:8	SPIM1_CS_N_FMODE	MCU_SPIM1_CS_N Function Mode setting	RW modify	0x0
7:6	SPIM0_MISO_FMODE	MCU_SPIM0_MISO Function Mode setting	RW modify	0x0
5:4	SPIM0_MOSI_FMODE	MCU_SPIM0_MOSI Function Mode setting	RW modify	0x0
3:2	SPIM0_CLK_FMODE	MCU_SPIM0_CLK Function Mode setting	RW modify	0x0
1:0	SPIM0_CS_N_FMODE	MCU_SPIM0_CS_N Function Mode setting	RW modify	0x0

5.41. FMODE_CFG5

FMODE_CFG5			
Description	For details on Function Mode, see "Datasheet Summary 5.1 Setting Multiple function I/O".		
Address Region	gconf	**Type:**	RW
Offset	0x0000 0154		
Physical address View0	0x4004 A154		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:2	Reserved	-	-	-
1:0	SPIC_FMODE	MCU_SPIC_* Function Mode setting	RW modify	0x0

5.42. FMODE_CFG6

FMODE_CFG6			
Description	For details on Function Mode, see "Datasheet Summary 5.1 Setting Multiple function I/O".		
Address Region	gconf	**Type:**	RW
Offset	0x0000 0158		
Physical address View0	0x4004 A158		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:2	Reserved	-	-	-
1:0	ADC24_SYNC_FMODE	MCU_ADC24_SYNC Function Mode setting	RW modify	0x0

5.43. OE_CTRL

OE_CTRL			
Description			
Address Region	gconf	**Type:**	RW
Offset	0x0000 0200		
Physical address View0	0x4004 A200		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:13	Reserved	-	-	-
12	CPU_TRACE_OE	Output Enable for CPU Trace signals 1 : Output Enable 0 : Output Disable	RW modify	0
11:9	Reserved	-	-	-
8	ADC24_OE	Output Enable for ASC24 signals 1 : Output Enable 0 : Output Disable	RW modify	0
7	SPIM3_OE	Output Enable for SPIM3 signals 1 : Output Enable 0 : Output Disable	RW modify	0
6	SPIM2_OE	Output Enable for SPIM2 signals 1 : Output Enable 0 : Output Disable	RW modify	0
5	SPIM1_OE	Output Enable for SPIM1 signals 1 : Output Enable 0 : Output Disable	RW modify	0
4	SPIM0_OE	Output Enable for SPIM0 signals 1 : Output Enable 0 : Output Disable	RW modify	0
3	Reserved	-	-	-
2	UART2_OE	Output Enable for UART2 signals 1 : Output Enable 0 : Output Disable	RW modify	0
1	UART1_OE	Output Enable for UART1 signals 1 : Output Enable 0 : Output Disable	RW modify	0
0	UART0_OE	Output Enable for UART0 signals 1 : Output Enable 0 : Output Disable	RW modify	0

6. Revision History

Table 6.1 Revision History

Revision	Date	Description
0.1	2014-03-13	Newly released
0.2	2014-04-08	Corrected the register details.
0.3	2014-09-29	Revised for rev.2.0: 5. Details of Registers.
1.0	2015-01-22	Official version
1.1	2018-02-02	Changed header, footer and the last page. Changed corporate name and descriptions.

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