Application Processor Lite *ApP Lite*

TZ1000 Series

Reference Manual

MCU Event Control Block

Revision 1.2

2018-02

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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Preface

This specification document describes the specification of MCU Event Control Block which has been developed for the TZ1000 Series.

Intended Audience

This document is intended for the following users.

Driver software developers.

System designers

Conventions in this Document

- The numerical values are expressed as follows.
  Hexadecimal number: 0xABC
  Decimal number: 123 or 0d123 - Only when it needs to be explicitly shown that they are decimal numbers.
  Binary number: 0b111 - It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [3:0].
  [3:0] shows four signal names 3, 2, 1, and 0 together.
- The characters surrounded by [] defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1]***, ***[XYZ2]***, and ***[XYZ3]*** to ***[XYZn]***
- The bit range of a register is written like as [3:0].
  Example: Bit[3:0] expresses the range of bits 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***.EFG = 0x01 (hexadecimal), ***[XYZn]***.VW = 1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8-bit
  Half word: 16-bit
  Word: 32-bit
  Double word: 64-bit
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, don't use the read value.
- Properties of each bit in a register are expressed as follows.
  R: Read only
  W: Write only
  W1C: Write 1 Clear - The corresponding bit is cleared (=0) when "1" is written to this bit.
  W1S: Write 1 Set - The corresponding bit is set (=1) when "1" is written to this bit.
  R/W: Read and Write are possible.
  R/W0C: Read/Write 0 Clear
  R/W1C: Read/Write 1 Clear
  R/W1S: Read/Write 1 Set
  RS/WC: Read Set/Write Clear - Set after read operation, cleared after write operation.
- The value read from the bit having default value of "—" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value. In the cases that default is "—," follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value. In the cases that default is "—," follow the definition of each register.

1. Overview

EVM implements a function to propagate an event occurred in a block as a trigger of another block functions.

The following events are detected in the TZ1000 Series.

- Control signal from built-in devices
  - Control signal from BLE chip (GPIO31, GPIO30, GPIO29)
  - Interrupt signal from sensor (GPIO27, GPIO26, GPIO25, GPIO24)
- Interrupt signal from RTC
  - Alarm interrupt
  - Periodic interrupt
  - Interval interrupt

In the TZ1000 Series, the above events can be detected and selected as a trigger of the following functions:

- AdvTMR capture input
- ADCC12 conversion start

2. Block Diagram

Figure 2.1 is a block diagram of this module.

Event signals are input from the GPIO, RTC block and transmitted to AdvTMR, ADCC12 blocks as trigger signals. Receiving responses to a trigger from ADCC12 makes handshake of trigger signals. At this time, PMU is provided for clock control signals to release ADCC12 DCG.

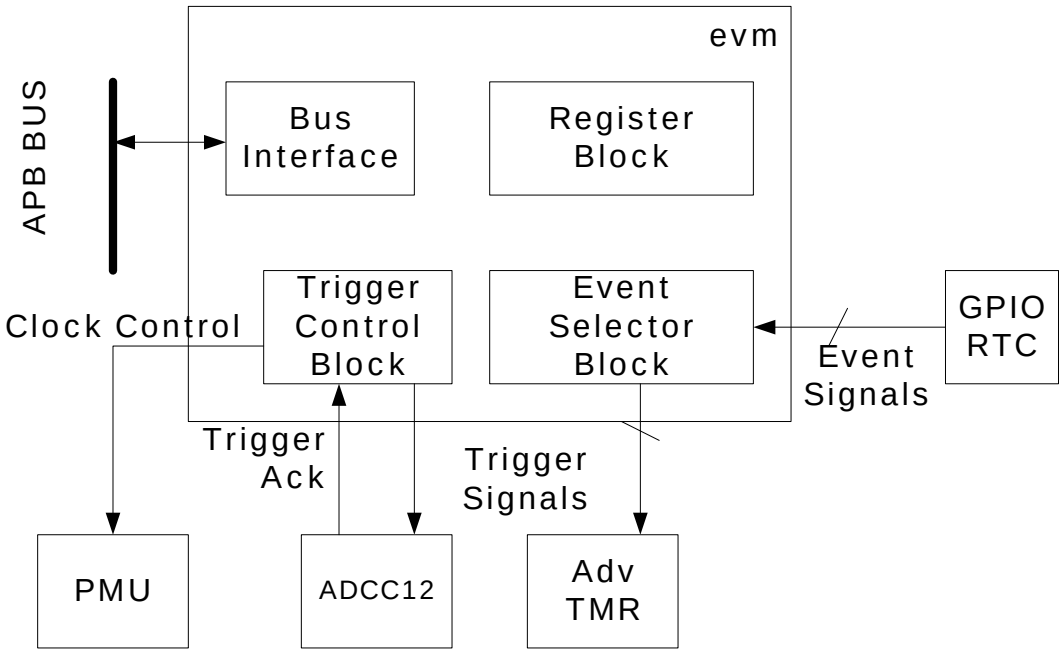

Figure 2.1 Block Diagram

3. Address Map

Table 3.1 MCU Event Control Block Register map

Register Name	Type	Width	Reset Value	Address Offset
EVM_EN	RW	32	0x0000 0000	0x0000 0000
TRIGGER_CH0	RW	32	0x0000 0000	0x0000 0010
TRIGGER_CH1	RW	32	0x0000 0000	0x0000 0014
TRIGGER_CH2	RW	32	0x0000 0000	0x0000 0018
TRIGGER_CH3	RW	32	0x0000 0000	0x0000 001C
TRIGGER_CH4	RW	32	0x0000 0000	0x0000 0020

4. Functional Description

4.1. Trigger operation

EVM will provide an another block with events occurred in each block without involvement by CPU. Event signals are selected by the setting of ***TRIGGER_CHn.***event_sel[3:0].

Table 4.1 and Table 4.2 respectively show event assignment and trigger assignment in the TZ1000 Series.

Table 4.1 Event assignment

Event 0	GPIO24 interrupt
Event 1	GPIO25 interrupt
Event 2	GPIO26 interrupt
Event 3	GPIO27 interrupt
Event 4	GPIO29 interrupt
Event 5	GPIO30 interrupt
Event 6	GPIO31 interrupt
Event 7	RTC alarm interrupt
Event 8	RTC periodic interrupt
Event 9	RTC interval interrupt

Table 4.2 Trigger assignment

Trigger ch0	Capture input to AdvTMR ch0
Trigger ch1	Capture input to AdvTMR ch1
Trigger ch2	Capture input to AdvTMR ch2
Trigger ch3	Capture input to AdvTMR ch3
Trigger ch4	Conversion to ADCC12 start request

4.2. Start/Stop sequence

4.2.1. Start sequence

Below is the EVM start sequence:

(1) Set pmu.*CG_OFF_PM_0*.CG_mpierclk_evm_clk.
(2) Set pmu.*SRST_OFF_PM_0*.SRST_asyncrst_evm_prstn.
(3) Set *EVM_EM*.
(4) Set event which may occur in *TRIGGER_CHn*.eventsel[11:8]
(5) Set *TRIGGER_CHn*.trigger_en to start event detection

4.2.2. Stop sequence

Below is the EVM stop sequence:

(1) Check TRIGGER_CHn.status bit to see if the event has been asserted or not. Clear events if the event still is asserted.
(2) Clear *TRIGGER_CHn*.trigger_en.
(3) Clear EVM_EN
(4) Set pmu.*SRST_ON_PM_0*.SRST_asyncrst_evm_prstn.
(5) Set pmu.*CG_OFF_PM_0*.CG_mpierclk_evm_clk.

4.3. Operation on Powermode

Below shows operation of EVM on each Powermode.

- Sleep0/1:
  Normal operation.
- Sleep2:
  Event detection and trigger generation is not available because the EMV operation clock is stopped. Any event occurred during transition to this Powermode will be processed after recovery. Ensure that *[TRIGGER_CH4]*.status is "0" before transition to this Powermode.
- WAIT:
  Event detection and trigger generation is not available because the EMV operation clock is stopped. Ensure that *[TRIGGER_CH4]*.status is "0" before transition to this Powermode.
- RETENTION:
  Event detection and trigger generation is not available because the EMV operation clock is stopped. Ensure that *[TRIGGER_CH4]*.status is "0" before transition to the same Powermode.
- RTC/STOP:
  EVM is shut off. Ensure that *[TRIGGER_CH4]*.status is "0" before transition to this Powermode.

In case move to WAIT/WAIT-RET/RETENTION/RTC/STOP mode, must check *[TRIGGER_CH4]*.status is ”0” and then do the sequence for ADCC12 mode transition.

4.4. Example of use

4.4.1. AdvTM capture external device interrupts

The interrupt occurrence time can be obtained by AdvTM capture external device interrupts. Below describes the example setting procedure.

- Set High Level interrupt to relevant GPIO3 pin.
- Set signals from EVM to AdvTMR CH capture input, and start capture operation.
- Start EVM trigger operation.
- On the occurrence of relevant external device interrupts, they can be detected as capture signals with AdVTMR.

4.4.2. ADCC12 conversion operation by RTC interrupts

RTC interrupts enable periodic sampling operation of ADCC12. It can be used for periodic sampling of power supply voltage, for example.

- Set RTC periodic interrupts.
- Set desirable sampling operation and interrupt occurrence at the lower-limit voltage to ADCC12.
- Start EVM trigger operation.
- Preset ADCC12 conversion operation begins on the occurrence of RTC periodic interrupts.
- When the above operation repeats periodically and the lower-limit voltage is detected by ADCC12 sampling operation, interrupts occur against CPU.

5. Details of Registers

5.1. EVM_EN

EVM_EN			
Description			
Address Region	evm	**Type:**	RW
Offset	0x0000 0000		
Physical address View0	0x4002 3000		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:1	Reserved	-	-	-
0	evm_enable	Enable signal for this block 0: Stop 1: Operation	RW modify	0

5.2. TRIGGER_CH0

TRIGGER_CH0			
Description			
Address Region	evm	**Type:**	RW
Offset	0x0000 0010		
Physical address View0	0x4002 3010		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31	status	Indicates the trigger status. 0: Trigger signal is Low. 1: Trigger signal is High.	RO	0
30:12	Reserved	-	-	-
11:8	event_sel	Event signal selection Writable only when bit0 (trigger enable) is "L". Ignored if written when the bit is "H". 0000: Selects event 0. 0001: Selects event 1. 0010: Selects event 2. 0011: Selects event 3. 0100: Selects event 4. 0101: Selects event 5. 0110: Selects event 6. 0111: Selects event 7. 1000: Selects event 8. 1001: Selects event 9. If the setting is other than the above, the trigger signal is fixed at Low Level.	RW modify	0x0
7:1	Reserved	-	-	-
0	trigger_enable	Trigger operation enable signal 0: Stop 1: Operation	RW modify	0

5.3. TRIGGER_CH1

TRIGGER_CH1				
Description				
Address Region	evm	**Type:**	RW	
Offset	0x0000 0014			
Physical address View0	0x4002 3014			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31	status	Indicates the trigger status. 0: Trigger signal is Low. 1: Trigger signal is High.	RO	0
30:12	Reserved	-	-	-
11:8	event_sel	Event signal selection Writable only when bit0 (trigger enable) is "L". Ignored if written when the bit is "H". 0000: Selects event 0. 0001: Selects event 1. 0010: Selects event 2. 0011: Selects event 3. 0100: Selects event 4. 0101: Selects event 5. 0110: Selects event 6. 0111: Selects event 7. 1000: Selects event 8. 1001: Selects event 9. If the setting is other than the above, the trigger signal is fixed at Low Level.	RW modify	0x0
7:1	Reserved	-	-	-
0	trigger_enable	Trigger operation enable signal 0: Stop 1: Operation	RW modify	0

5.4. TRIGGER_CH2

TRIGGER_CH2				
Description				
Address Region	evm	**Type:**	RW	
Offset	0x0000 0018			
Physical address View0	0x4002 3018			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31	status	Indicates the trigger status. 0: Trigger signal is Low. 1: Trigger signal is High.	RO	0
30:12	Reserved	-	-	-

11:8	event_sel	Event signal selection Writable only when bit0 (trigger enable) is "L". Ignored if written when the bit is "H". 0000: Selects event 0. 0001: Selects event 1. 0010: Selects event 2. 0011: Selects event 3. 0100: Selects event 4. 0101: Selects event 5. 0110: Selects event 6. 0111: Selects event 7. 1000: Selects event 8. 1001: Selects event 9. If the setting is other than the above, the trigger signal is fixed at Low Level.	RW modify	0x0
7:1	Reserved	-	-	-
0	trigger_enable	Trigger operation enable signal 0: Stop 1: Operation	RW modify	0

5.5. TRIGGER_CH3

TRIGGER_CH3			
Description			
Address Region	evm	**Type:**	RW
Offset	0x0000 001C		
Physical address View0	0x4002 301C		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31	status	Indicates the trigger status. 0: Trigger signal is Low. 1: Trigger signal is High.	RO	0
30:12	Reserved	-	-	-
11:8	event_sel	Event signal selection Writable only when bit0 (trigger enable) is "L". Ignored if written when the bit is "H". 0000: Selects event 0. 0001: Selects event 1. 0010: Selects event 2. 0011: Selects event 3. 0100: Selects event 4. 0101: Selects event 5. 0110: Selects event 6. 0111: Selects event 7. 1000: Selects event 8. 1001: Selects event 9. If the setting is other than the above, the trigger signal is fixed at Low Level.	RW modify	0x0
7:1	Reserved	-	-	-
0	trigger_enable	Trigger operation enable signal 0: Stop 1: Operation	RW modify	0

5.6. TRIGGER_CH4

TRIGGER_CH4			
Description			
Address Region	evm	**Type:**	RW
Offset	0x0000 0020		
Physical address View0	0x4002 3020		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31	status	Indicates the trigger status. 0: Trigger signal is Low. 1: Trigger signal is High.	RO	0
30:12	Reserved	-	-	-
11:8	event_sel	Event signal selection Writable only when bit0 (trigger enable) is "L". Ignored if written when the bit is "H". 0000: Selects event 0. 0001: Selects event 1. 0010: Selects event 2. 0011: Selects event 3. 0100: Selects event 4. 0101: Selects event 5. 0110: Selects event 6. 0111: Selects event 7. 1000: Selects event 8. 1001: Selects event 9. If the setting is other than the above, the trigger signal is fixed at Low Level.	RW modify	0x0
7:1	Reserved	-	-	-
0	trigger_enable	Trigger operation enable signal 0: Stop 1: Operation	RW modify	0

6. Precautions

6.1. Bus access during reset

When accessed while the EVM is in the reset state, the write access is ignored and the read access returns "0".

6.2. Access to Reserved domain

If the reserved area in assigned EVM is accessed, the write access is ignored and the read access returns "0".

6.3. Sampling period

A sampling period of the events in EVM is a clock period of the clock domain CD_MPIER. Because it's frequency may be changed by each power and voltage mode, please care that event signals can be captured by the CD_MPIER clock.

6.4. The CPU access prohibition for ADCC12 conversion

If the trigger CH4 which starting request of ADCC12 conversion enables, the conversion starting by the CPU (setting by ADCC12.*ADCCTL*.Start) must not be asserted.

7. Revision History

Table 7.1 Revision History

Revision	Date	Description
0.1	2014-03-19	Newly released
0.2	2014-10-07	Change the expression
0.3	2014-12-12	Add the description to “4.3 Operation on Powermode”
1.0	2015-01-23	Official version
1.1	2015-07-02	Revised 1.Overview description
1.2	2018-02-06	Changed header, footer and the last page. Changed corporate name and descriptions. Modified description of the trademark.

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