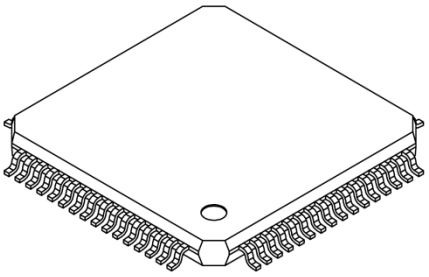
TOSHIBA Bi-CMOS Integrated Circuit Silicon Monolithic

TB9081FG

Automotive GATE-driver for Brushless motor

TB9081FG is Pre-driver IC for automotive brushless motor.
Fail-safe relay pre-drivers are also built in in addition to 3-phase pre-drivers.
The charge pump, the motor current detection circuit, the oscillator, and the SPI communication circuit are built in.
The miscellaneous abnormal detections are carried and the operation after failure detection conditions and failure detections can be set up. About each setup, these can set up through a SPI communication.
Also, it has built-in ABIST / LBIST functions for diagnosing the normal operation of the miscellaneous abnormal detection function.



LQFP64-P-1010-0.50E

Weight: 0.35 g (typ.)

Features

- 3-phase pre-drivers : PWM control to 20kHz
- Build-in fail-safe relay pre-drivers
- Build-in Charge Pump
- High response Current Detection circuit
- Miscellaneous-abnormal-detection circuits
  (Under voltage (VB, VCC) / Over voltage (VCC) / Over temp. / FET short-circuit detection)
- Build-in ABIST/LBIST functions
- Operating voltage range : VB=4.5 to 18V, VCC=3.0 to 5.5V
- Operational temperature range : -40 to 125°C
- Package : LQFP-64pin (0.5mm pitch)

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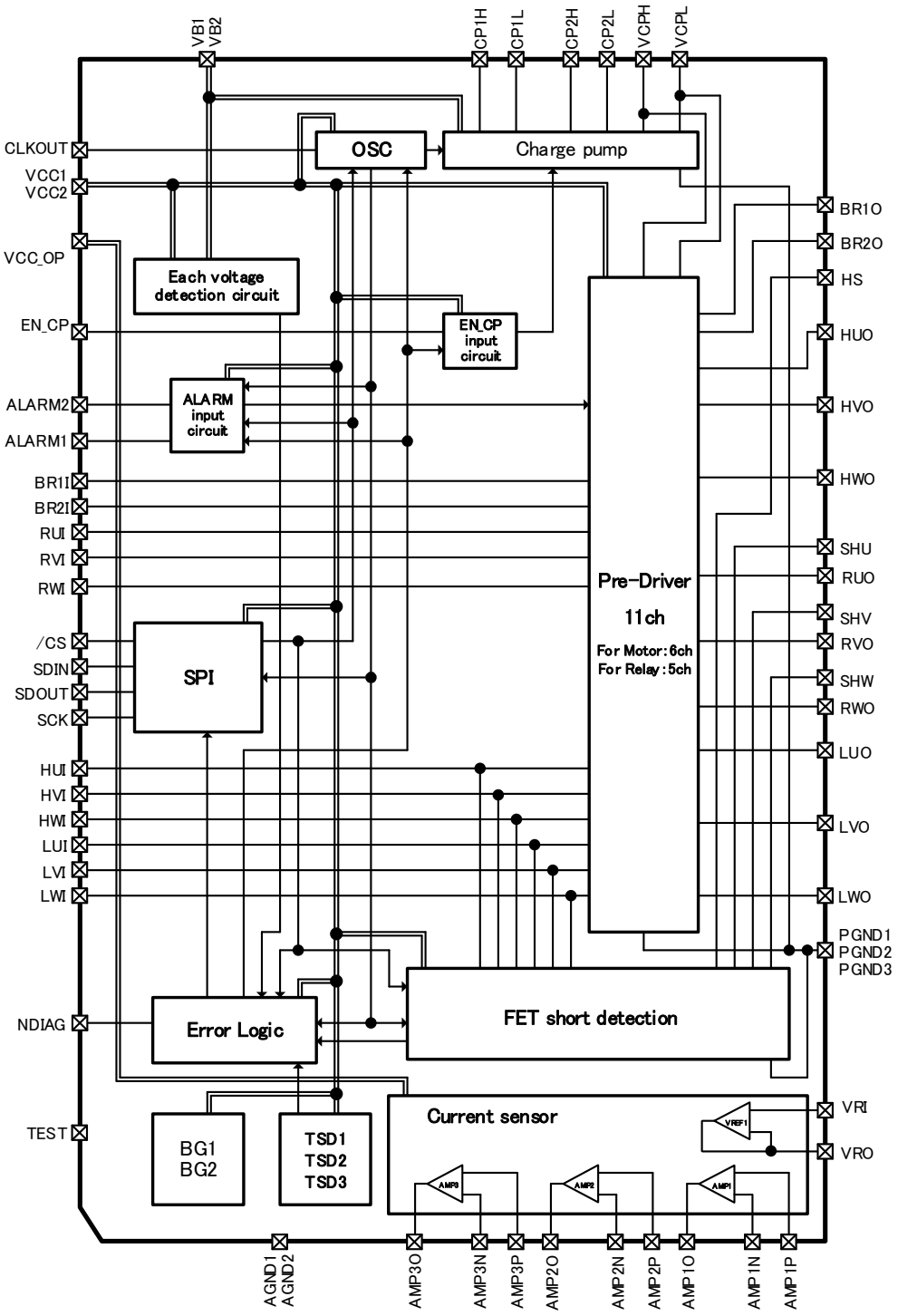
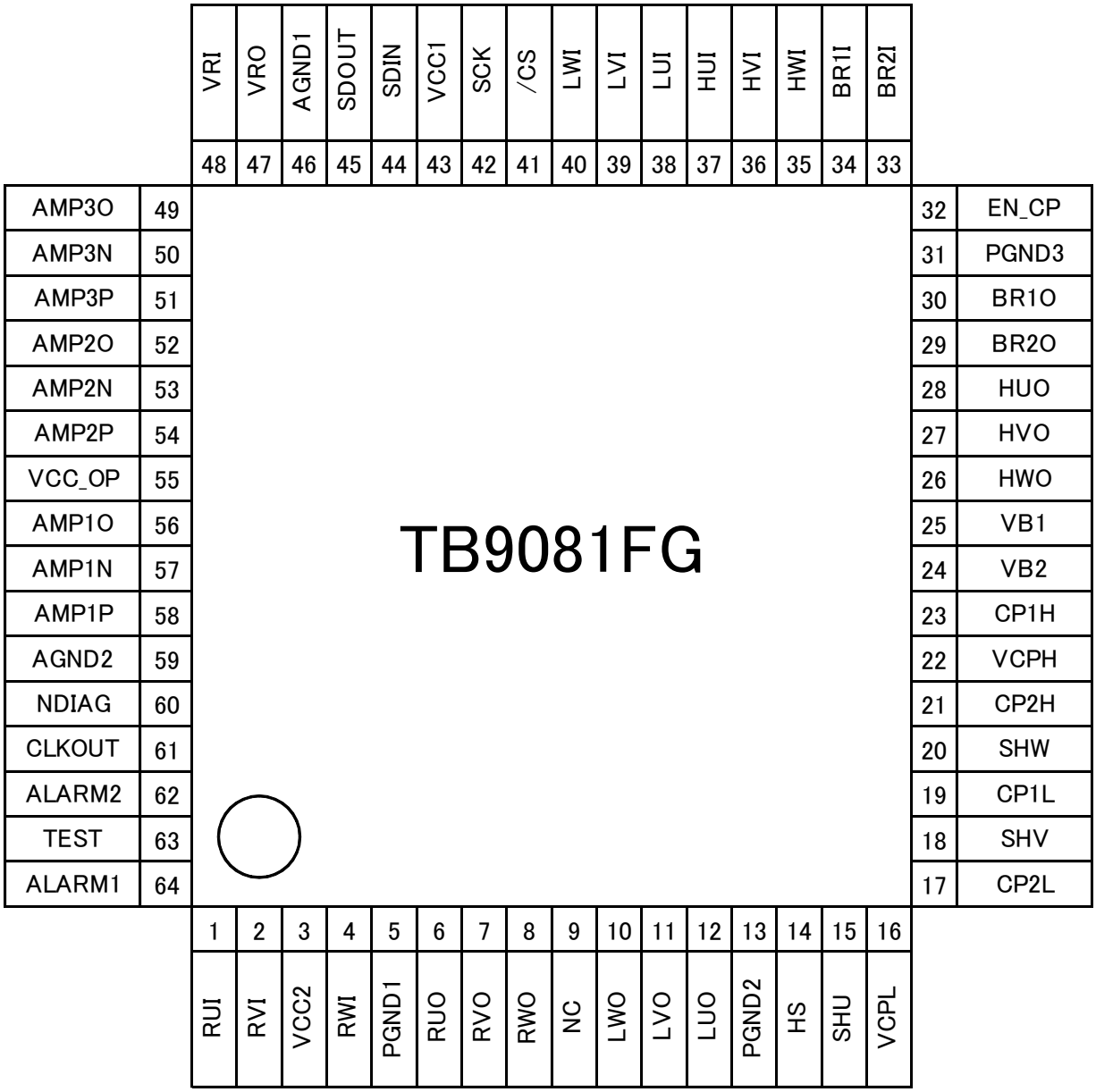
Internal block diagram



Notes 1: Some of the functional blocks, circuit, or constants in the block diagram may be omitted or simplified for explanatory purpose. (including individual block diagram)

Package pin layout (top view)



Pin description

Pin No.	Symbol	Input/output	Definition	Pull-Up/Down		Notes
1	RUI	IN	Pre-Driver Input RU (Motor Relay)	Pull-Down	50kΩ	-
2	RVI	IN	Pre-Driver Input RV (Motor Relay)	Pull-Down	50kΩ	-
3	VCC2	Power supply	Power supply 2 (3.3V or 5V)	-	-	-
4	RWI	IN	Pre-Driver Input RW (Motor Relay)	Pull-Down	50kΩ	-
5	PGND1	GND	Power GND1	-	-	-
6	RUO	OUT	Pre-Driver Output RU (Motor Relay)	-	-	push-pull
7	RVO	OUT	Pre-Driver Output RV (Motor Relay)	-	-	push-pull
8	RWO	OUT	Pre-Driver Output RW (Motor Relay)	-	-	push-pull
9	NC	-	-	-	-	-
10	LWO	OUT	Pre-Driver Output LW	-	-	push-pull
11	LVO	OUT	Pre-Driver Output LV	-	-	push-pull
12	LUO	OUT	Pre-Driver Output LU	-	-	push-pull
13	PGND2	GND	Power GND2	-	-	-
14	HS	IN	Pre-Driver High-side Drain Input	-	-	-
15	SHU	IN	Motor Connect PIN U-phase	-	-	-
16	VCPL	Power supply	Charge-pump voltage (for low sides)	-	-	-
17	CP2L	OUT	2nd Charge Pump Drive Output	-	-	push-pull
18	SHV	IN	Motor Connect PIN V-phase	-	-	-
19	CP1L	OUT	1st Charge Pump Drive Output	-	-	push-pull
20	SHW	IN	Motor Connect PIN W-phase	-	-	-
21	CP2H	IN/OUT	2nd Charge Pump Output	-	-	-
22	VCPH	Power supply	Charge-pump voltage (for high sides)	-	-	-
23	CP1H	IN/OUT	1st Charge Pump Output	-	-	-
24	VB2	Power supply	Power Supply2 (Battery 12V)	-	-	-
25	VB1	Power supply	Power Supply1 (Battery 12V)	-	-	-
26	HWO	OUT	Pre-Driver Output HW	-	-	push-pull
27	HVO	OUT	Pre-Driver Output HV	-	-	push-pull
28	HUO	OUT	Pre-Driver Output HU	-	-	push-pull
29	BR2O	OUT	Pre-Driver Output BR2 (Power supply relay)	-	-	push-pull
30	BR1O	OUT	Pre-Driver Output BR1 (Power supply relay)	-	-	push-pull
31	PGND3	GND	Power GND 3	-	-	-
32	EN_CP	IN	Charge-pump enable signal	Pull-Down	50kΩ	-
33	BR2I	IN	Pre-Driver Input BR2 (Power supply relay)	Pull-Down	50kΩ	-
34	BR1I	IN	Pre-Driver Input BR1 (Power supply relay)	Pull-Down	50kΩ	-
35	HWI	IN	Pre-Driver Input HW	Pull-Down	50kΩ	-
36	HVI	IN	Pre-Driver Input HV	Pull-Down	50kΩ	-
37	HUI	IN	Pre-Driver Input HU	Pull-Down	50kΩ	-
38	LUI	IN	Pre-Driver Input LU	Pull-Down	50kΩ	-
39	LVI	IN	Pre-Driver Input LV	Pull-Down	50kΩ	-
40	LWI	IN	Pre-Driver Input LW	Pull-Down	50kΩ	-
41	/CS	IN	SPI chip select	Pull-Up	50kΩ	-
42	SCK	IN	SPI clock input	Pull-Down	50kΩ	-
43	VCC1	Power supply	Power supply 1 (3.3V or 5V)	-	-	-
44	SDIN	IN	SPI input	Pull-Down	50kΩ	-
45	SDOUT	OUT	SPI Output	-	-	push-pull
46	AGND1	GND	The GND 1 for analog circuits	-	-	-
47	VRO	OUT	Reference voltage amplifier Output	-	-	-
48	VRI	IN	Reference voltage amplifier input	-	-	-
49	AMP3O	OUT	Current-detection amplifier Output 3	-	-	push-pull
50	AMP3N	IN	Current-detection amplifier input 3 (-)	-	-	-
51	AMP3P	IN	Current-detection amplifier input 3 (+)	-	-	-
52	AMP2O	OUT	Current-detection amplifier Output 2	-	-	push-pull
53	AMP2N	IN	Current-detection amplifier input 2 (-)	-	-	-
54	AMP2P	IN	Current-detection amplifier input 2 (+)	-	-	-
55	VCC_OP	Power supply	The power supply for Current-detection amplifier (5V/3.3V)	-	-	-
56	AMP1O	OUT	Current-detection amplifier Output 1	-	-	push-pull
57	AMP1N	IN	Current-detection amplifier input 1 (-)	-	-	-
58	AMP1P	IN	Current-detection amplifier input 1 (+)	-	-	-
59	AGND2	GND	The ground 2 for analog circuits	-	-	-
60	NDIAG	OUT	Error Output Pin	-	-	push-pull
61	CLKOUT	OUT	Clock output	-	-	push-pull
62	ALARM2	IN	Pre-driver enable 2	Pull-Down	50kΩ	-
63	TEST	IN	Test terminal	Pull-Down	50kΩ	-
64	ALARM1	IN	Pre-driver enable 1	Pull-Down	50kΩ	-

●Description of an internal signal name

Internal signal name	Description	State	
		H	L
abst_pass	Normal signal of ABIST	ABIST normal	ABIST abnormal
abst_end	End signal of ABIST	ABIST end	ABIST unfinished
gate_en_u	Pre-driver output enabling signal (U phase)	Enable	Disable
gate_en_v	Pre-driver output enabling signal (V phase)	Enable	Disable
gate_en_w	Pre-driver output enabling signal (W phase)	Enable	Disable
gate_en_r	Pre-driver output enabling signal (relay)	Enable	Disable
gate_off_u	Error output signal (Pre-driver output enabling, U phase)	Enable	Disable
gate_off_v	Error output signal (Pre-driver output enabling, V phase)	Enable	Disable
gate_off_w	Error output signal (Pre-driver output enabling, W phase)	Enable	Disable
gate_off_r	Error output signal (Pre-driver output enabling, relay)	Enable	Disable
cp_en	Enabling signal for charge pump circuit	Enable	Disable
cp_off	Error output signal (charge pump circuit enabling)	Enable	Disable
vbl1	VB1/VB2 under voltage detection signal 1	Detection	Release
vbl2	VB1/VB2 under voltage detection signal 2	Detection	Release
vcl1	VCC1/VCC2 under voltage detection signal 1	Detection	Release
vcl2	VCC1/VCC2 under voltage detection signal 2	Detection	Release
por_x	Internal reset signal	Reset release	Reset
vch	VCC1/VCC2 over voltage detection signal	Detection	Release
vphh	VCPH clamp voltage detection signal	Detection	Release
tsd1det	Over temperature detection signal1	Detection	Release
tsd2det	Over temperature detection signal2	Detection	Release
tsd3det	Over temperature detection signal3	Detection	Release
shuho	Short-circuit detection signal (U phase low side)	Detection	Release
shvho	Short-circuit detection signal (V phase low side)	Detection	Release
shwho	Short-circuit detection signal (W phase low side)	Detection	Release
shulo	Short-circuit detection signal (U phase high side)	Detection	Release
shvlo	Short-circuit detection signal (V phase high side)	Detection	Release
shwlo	Short-circuit detection signal (W phase high side)	Detection	Release

<Usage power supply/GND list>

Symbol	Pin name	Function/Application
Vb	VB1,VB2	Battery power supply
Vcc	VCC1,VCC2	External 5V/3.3V power supply
Vccop	VCC_OP	The power supply for current detection amplifier (5V/3.3V)
Vcph	VCPH	Charge pump voltage (for high sides)
Vcpl	VCPL	Charge pump voltage (for low sides)
AGND	AGND1,AGND2	GND for analog circuitry
PGND	PGND1,PGND2,PGND3	Power GND

Functional descriptions

(1) Charge pump circuit

TB9081FG build in Charge pump for Pre-Drivers and it can control external Nch MOSFETs directly. Two charge pump voltages the object for the high side drive of a motor and the object for the relay drive of a motor, and for the low side drive of a motor is generated.

The charge pump voltage (Vcph) for a high side drive and a relay drive control by an internal circuit, and if Vcph goes up to Vb+12V (Typ.), a charge pump will suspend operation. Furthermore, in consideration of an overvoltage state, if Vcph goes up to 37V, a charge pump will stop, and if Vcph is less than 36.5V, a charge pump will resume operation.

The charge pump voltage (Vcpl) for a low side drive is generated from Vcph. If Vcpl goes up to (16V), a clamp will start and it will not become the voltage more than clamp voltage.

It is possible to build the switching circuit (CP_SW) in the Vb side of a charge pump circuit, to make a transistor turn off by CP_SW, and to stop the supply to Vcph from Vb. Vcc voltage turns off the transistor of CP_SW on condition of the conditions as for which below Vcc voltage detection voltage becomes, or EN_CP=L. For details, please refer to a (7) EN_CP circuit.

Moreover, it is possible to operate or stop a charge pump by terminal EN_CP. The charge pump operates at the time of EN_CP="H",and it stops at the time of EN_CP="L" and also suspends the supply to Vcph from Vb .

A Vcph output voltage is set to 0V at the time of the charge-pump stop by EN_CP="L."

When the charge pump is stopped by the control in the IC, Vcph output voltage will become the "Vb-3VF".

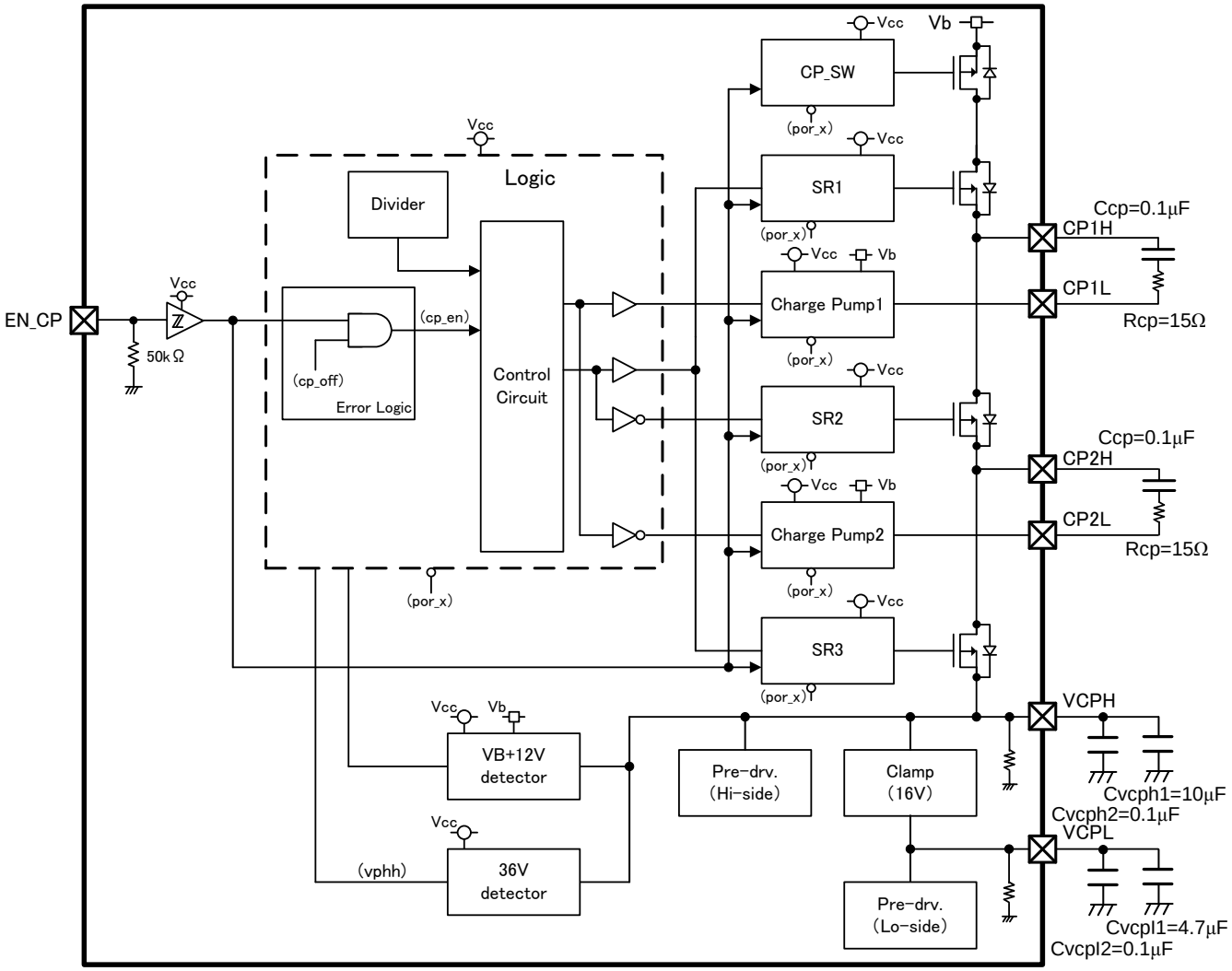


Fig.1- a Charge pump circuit Block Diagram

(2) Pre-drivers

TB9081FG has the pre-driver circuit it is for the motor relay drive, for the power relay drive, for the low-side drive of the motor and for the high-side drive of the motor. Each pre-driver circuit has a respective input and output terminals are controlled by a signal inputted to the input terminals.

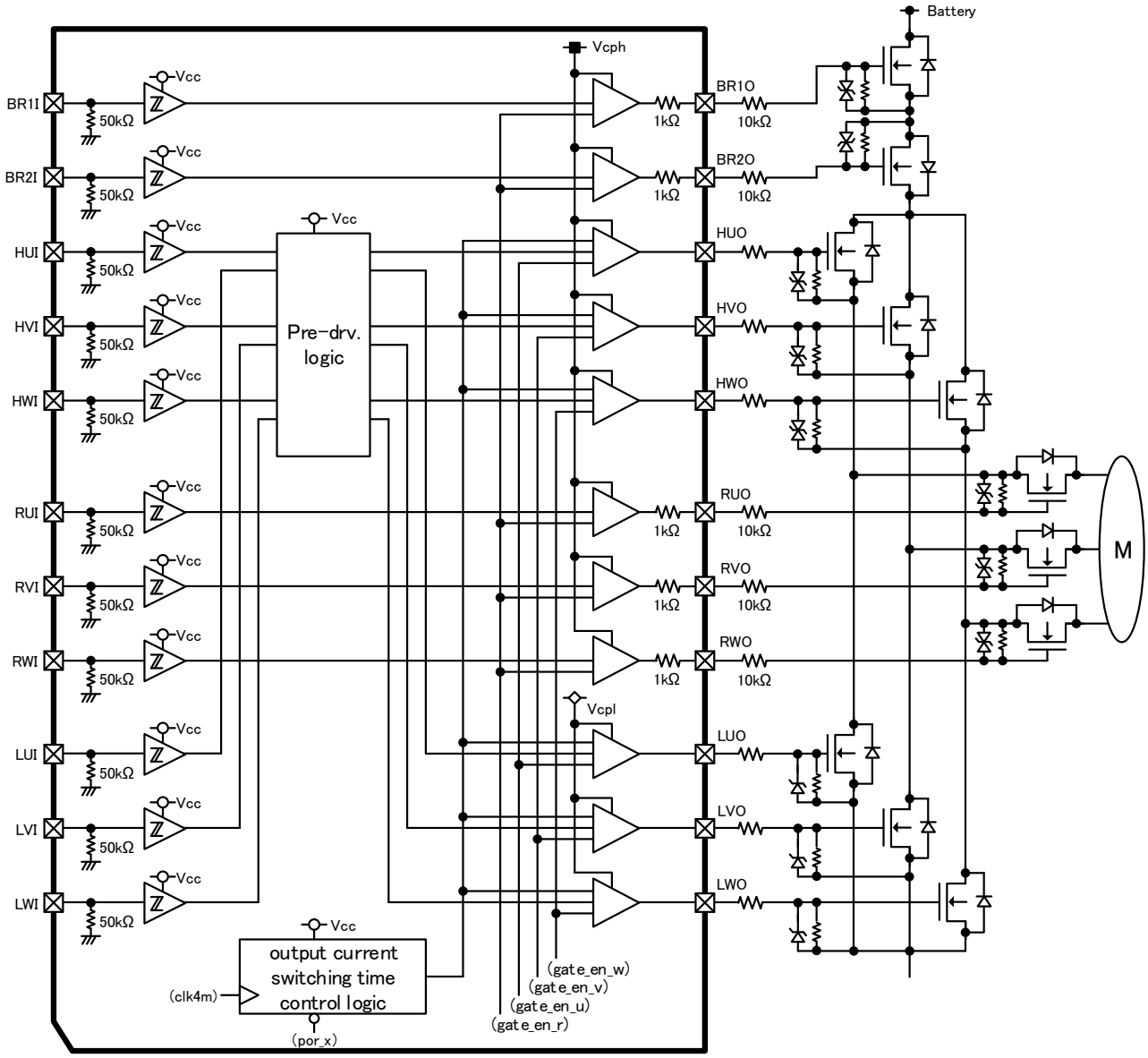


Fig.2- a Pre-driver circuit Block Diagram

<A power supply relay drive circuit, a motor relay drive circuit>

A power supply relay drive circuit is a circuit which controls FET for a relay on the battery power-supply side.

A motor relay drive circuit is a circuit which controls FET for a relay on the motor side.

A truth table is shown in table 2-a and 2-b. Refer to the (6) ALARM input circuit for the details of the internal signal (gate_en_r) in a truth table.

Moreover, resistance 1kΩ is built in the output of a power supply relay drive and a motor relay drive.

Furthermore, the diode for prevention of backflow at the time of reverse connection is built in the output of a power supply relay drive circuit.

- Table 2- a Input/output truth table 1 (power supply relay drive circuit)

- Power supply relay drive circuit 1

Input	Internal signal	Output	Notes
BR1I	(gate_en_r)	BR1O	
L	H	L	-
H	H	H	-
*	L	L	-

*:Don't care

- Power supply relay drive circuit 2

Input	Internal signal	Output	Notes
BR2I	(gate_en_r)	BR2O	
L	H	L	-
H	H	H	-
*	L	L	-

*:Don't care

- Table 2- b Input/output truth table 2 (motor relay drive circuit)

- Motor relay drive circuit 1 (U phase)

Input	Internal signal	Output	Notes
RUI	(gate_en_r)	RUO	
L	H	L	-
H	H	H	-
*	L	L	-

*:Don't care

- Motor relay drive circuit 2 (V phase)

Input	Internal signal	Output	Notes
RVI	(gate_en_r)	RVO	
L	H	L	-
H	H	H	-
*	L	L	-

*:Don't care

- Motor relay drive circuit 3 (W phase)

Input	Internal signal	Output	Notes
RWI	(gate_en_r)	RWO	
L	H	L	-
H	H	H	-
*	L	L	-

*:Don't care

<A high side drive circuit, a low side drive circuit>

A high side drive circuit is a circuit which drives FET of the high side of a motor. A low side drive circuit is a circuit which drives FET of the low side of a motor. A high side drive circuit and a low side drive circuit built in each 3ch.

An input signal (HUI/HVI/HWI, LUI/LVI/LWI) is changed by a control block, and output (HUO/HVO/HWO, LUO/LVO/LWO) is outputted. A truth table is shown in table 2-c. Refer to the (6) ALARM input circuit for the details of the internal signal (gate_en_u, gate_en_v, gate_en_w) in a truth table.

When HUI/LUI, HVI/LVI, and HWI/LWI are H/H, an output will be L/L (prohibition input). The operation at the time of prohibition input detection can be set up through a SPI communication.

Moreover, the current at the time of Turn on/Turn off of a high side drive circuit and a low side drive circuit is the current limit after 8 μs (typ). This current-limiting time can be set up a 3 value or no limit time through a SPI communication.

When gate_en_u, gate_en_v, and gate_en_w switch from “H” to “L” by the failure detection and ALARM1 or ALARM2 outputing low, and then, the high side drive circuit and the low side drive circuit output high, it switches to “L”. At this time, it has an output current capability which is decided by the ON resistance and the gate resistance of the output driver during the current limit time. However, only Vcc under voltage detection, the output current capability will be the output limit current Iolmtl even within the current limit time.

- Table 2- c Input/output truth table 3 (a high side drive circuit, a low side drive circuit)

- FET drive circuit 1 (U phase)

Input		Internal signal	Output		Notes
HUI	LUI	(gate_en_u)	HUO	LUO	
L	L	H	L	L	-
L	H	H	L	H	-
H	L	H	H	L	-
H	H	H	***L***	***L***	Inhibit input mode
*	*	L	L	L	-

*: Don’t care

- FET drive circuit 2 (V phase)

Input		Internal signal	Output		Notes
HVI	LVI	(gate_en_v)	HVO	LVO	
L	L	H	L	L	-
L	H	H	L	H	-
H	L	H	H	L	-
H	H	H	***L***	***L***	Inhibit input mode
*	*	L	L	L	-

*: Don’t care

- FET drive circuit 3 (W phase)

Input		Internal signal	Output		Notes
HWI	LWI	(gate_en_w)	HWO	LWO	
L	L	H	L	L	-
L	H	H	L	H	-
H	L	H	H	L	-
H	H	H	***L***	***L***	Inhibit input mode
*	*	L	L	L	-

*: Don’t care

(3) Current detector

TB9081FG are built three amplifiers for motor-current detection and one amplifier for reference voltage generation (Fig3- a).

The amplifiers for motor-current detection can amplify the difference voltage which produces according to the current which flows through the shunt resistance connected to the motor actuator.

The amplifier for reference voltage generation is used as buffer amplifier for reference voltage generation.

As an external configuration of the current detection, it is available in either 1 shunt configuration or 3 shunt configuration.

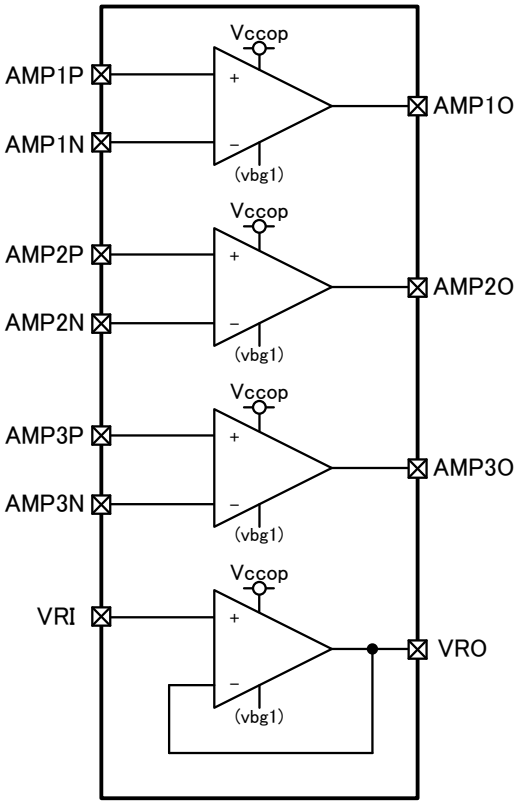


Fig.3- a Motor-current detection circuit Block Diagram

(4) Oscillator /divider

The oscillator has composition with built-in CR, and an Oscillation frequency is Fc=4MHz (typ.). An oscillator will start operation after internal signal (por_x) release.
4 MHz (clk4m) is used as the system clock of a logic circuit, and an operation clock of the digital filter of the short-circuit detector of external FET.
Clock 1MHz (clk1m), it is used as an operation clock of the digital filter of an ALARM detector.
Clock 500kHz (clk500k), it is used as an operation clock of a charge pump.
Clock 16kHz (clk16k), it is used as an operation clock of ABIST.
CLKOUT output (terminal) will output a clock set by the SPI (clk4m, clk500k, clk16k).

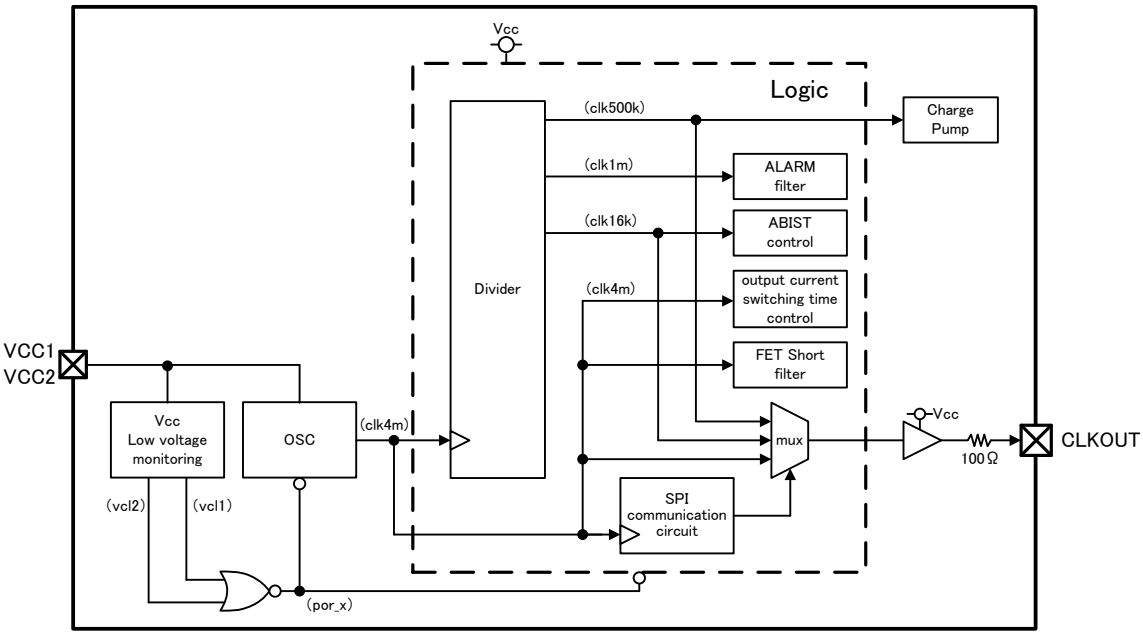


Fig.4- a Oscillator, divider Block Diagram

(5) Abnormal detection circuit

TB9081FG is built in miscellaneous abnormal detection circuit, such as the under voltage detection (VB1, VB2, VCC1, VCC2), over voltage detection (VCC1, VCC2), over temperature detection, external FET short-circuit detection and frequency abnormal detection.

(6) ALARM input circuit

As an input terminal of an ALARM signal, TB9081FG have two terminals of ALARM1 and ALARM2.
An ALARM signal controls Enable/Disable of the Pre-drivers (a FET drive circuit, a motor relay drive circuit, a power supply relay drive circuit).
In the case of ALARM1= "L" or ALARM2= "L", the Pre-drivers will be Disable. In the case of ALARM1="H" and ALARM2="H", Enable/Disable is decided by the input and internal signal of each Pre-drivers.
Also, the input side of the ALARM1 and ALARM2 terminal has a built-in digital filter (DF) for noise removal. Digital filter time can be set through the SPI communication.
If ALARM1="L" or ALARM2="L" is detected, the short-circuit detection function is enabled.

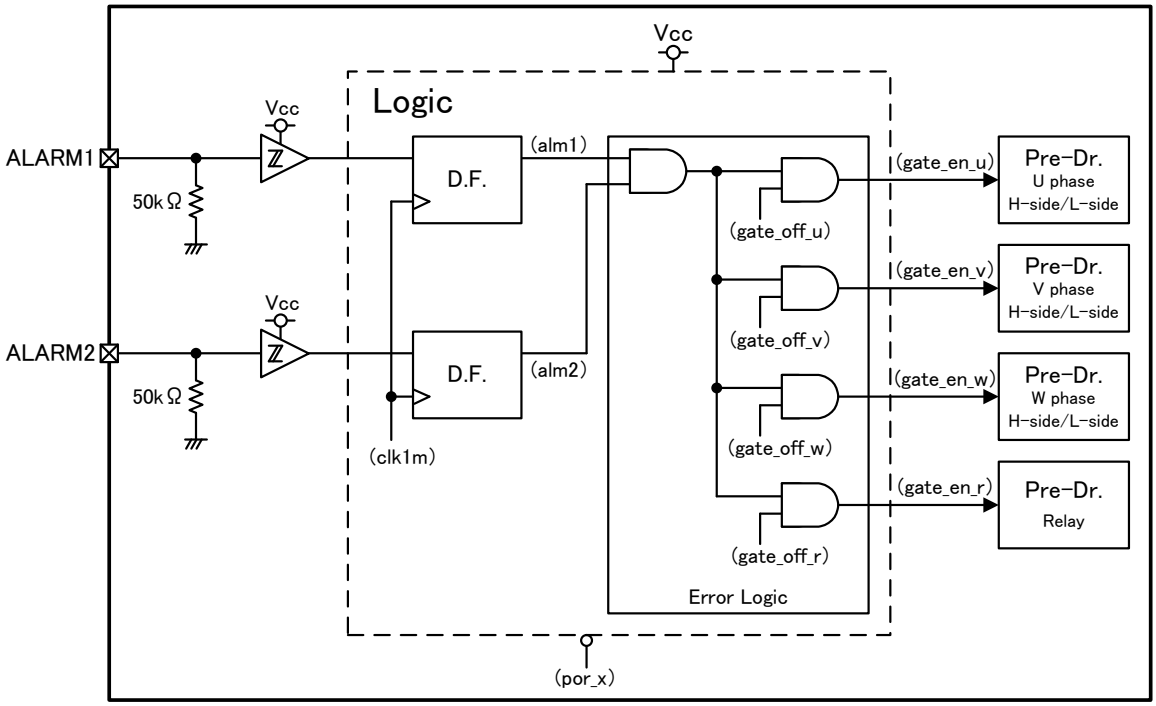


Fig.6-a FET drive circuit control Block Diagram

Table 6-a FET drive circuit control truth table

Input signal		Internal input signal					Internal control signal				FETdrive circuit
ALARM1	ALARM2	(por_x)	(gate_off_u)	(gate_off_v)	(gate_off_w)	(gate_off_r)	(gate_en_u)	(gate_en_v)	(gate_en_w)	(gate_en_r)	
L	*	*	*	*	*	*	L	L	L	L	Disable
*	L	*	*	*	*	*	L	L	L	L	Disable
*	*	L	*	*	*	*	L	L	L	L	Disable
H	H	H	L	-	-	-	L	-	-	-	U phase Disable
H	H	H	H	-	-	-	H	-	-	-	U phase Enable
H	H	H	-	L	-	-	-	L	-	-	V phase Disable
H	H	H	-	H	-	-	-	H	-	-	V phase Enable
H	H	H	-	-	L	-	-	-	L	-	W phase Disable
H	H	H	-	-	H	-	-	-	H	-	W phase Enable
H	H	H	-	-	-	L	-	-	-	L	Relay Disable
H	H	H	-	-	-	H	-	-	-	H	Relay Enable

(Note 1) “*”: Don’t care

(Note 2) Although "-":gate_off_* and gate_en_* have logic dependence in phase, the logic dependence to other phase is nothing.

(7) EN_CP input circuit

EN_CP signal controls Enable/Disable of a charge pump circuit.
In the case of input signal EN_CP= "L", the charge pump circuit will be Disable. In the case of EN_CP="H", Enable/Disable of the charge pump circuit is decided by an internal signal.
Also, the charge pump SW circuit (CP_SW) will be Disable in case of input signal EN_CP = "L" or the internal signal (por_x) = "L". In the case of EN_CP = (por_x) = "H", it will be Enable.

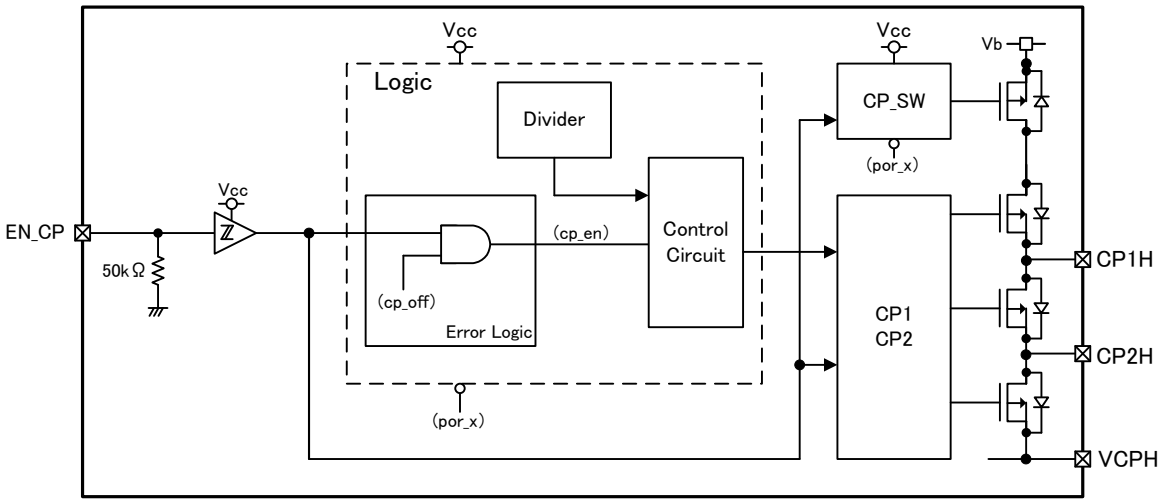


Fig.7-a EN_CP input circuit Block Diagram

Table 7-a Charge-pump-circuit control truth table

Input signal	Internal input signal		Internal control signal	Charge pump circuit	Charge pump SW circuit
EN_CP	(por_x)	(cp_off)	(cp_en)		
L	*	*	L	Disable	Disable
H	L	*	L	Disable	Disable
H	H	L	L	Disable	Enable
H	H	H	H	Enable	Enable

(Note) "*":Don't care

(8) ABIST function

At the time of IC starting, it is diagnosed whether miscellaneous abnormal detection is functioning normally. At the time of IC starting, a divider starts operation after VCC1/VCC2 under voltage release, and it starts diagnosis of ABIST after LBIST completion. Diagnosis of ABIST is performed even when a judgment of LBIST is NG.
A diagnostic part is as follows.
VCC1/VCC2 over voltage detection, VCPH clamp voltage detection, over temperature detection, and frequency abnormal detection (low frequency side)

(9) SPI Communication circuit

The SPI communication circuit consists of an SPI core circuit and a register read circuit block.
Only when /CS is L, communication with a microcomputer is attained. A microcomputer writes data in SDIN at the rising edge of a clock, and IC reads data at the following falling edges. Moreover, IC writes data in SDOUT at the rising edge of a clock, and a microcomputer reads data at the following falling edges. SDIN receives the data bit from a microcomputer in order from MSB to LSB. SDOUT transmits a data bit to a microcomputer in order from MSB to LSB. An output is push-pull composition and will be a Hi-Z at the time of /CS="H". Moreover, inside IC, the /CS terminal have pull-up by resistance, and the SDIN and SCK terminal have pull-down by resistance.

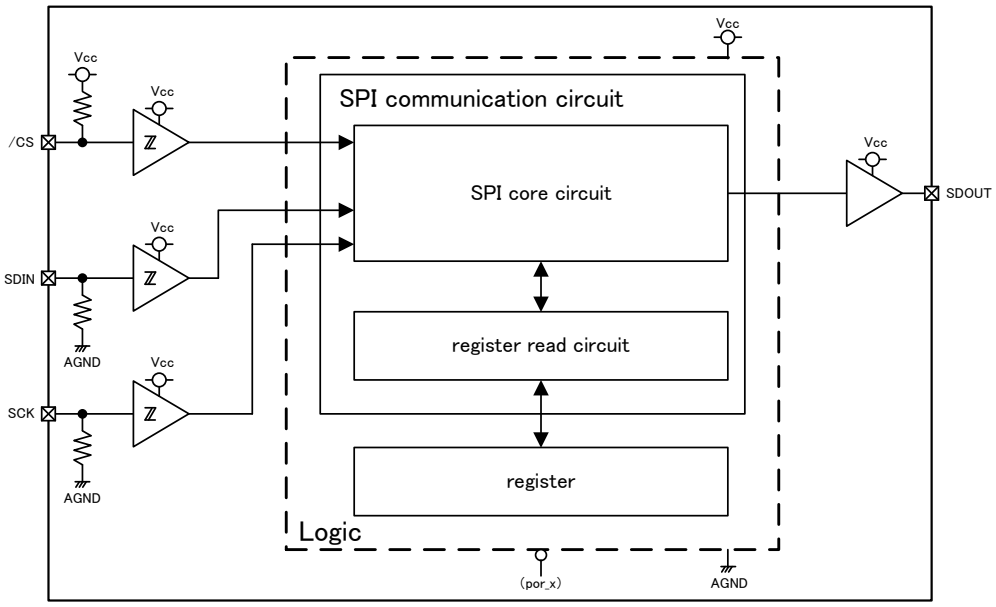
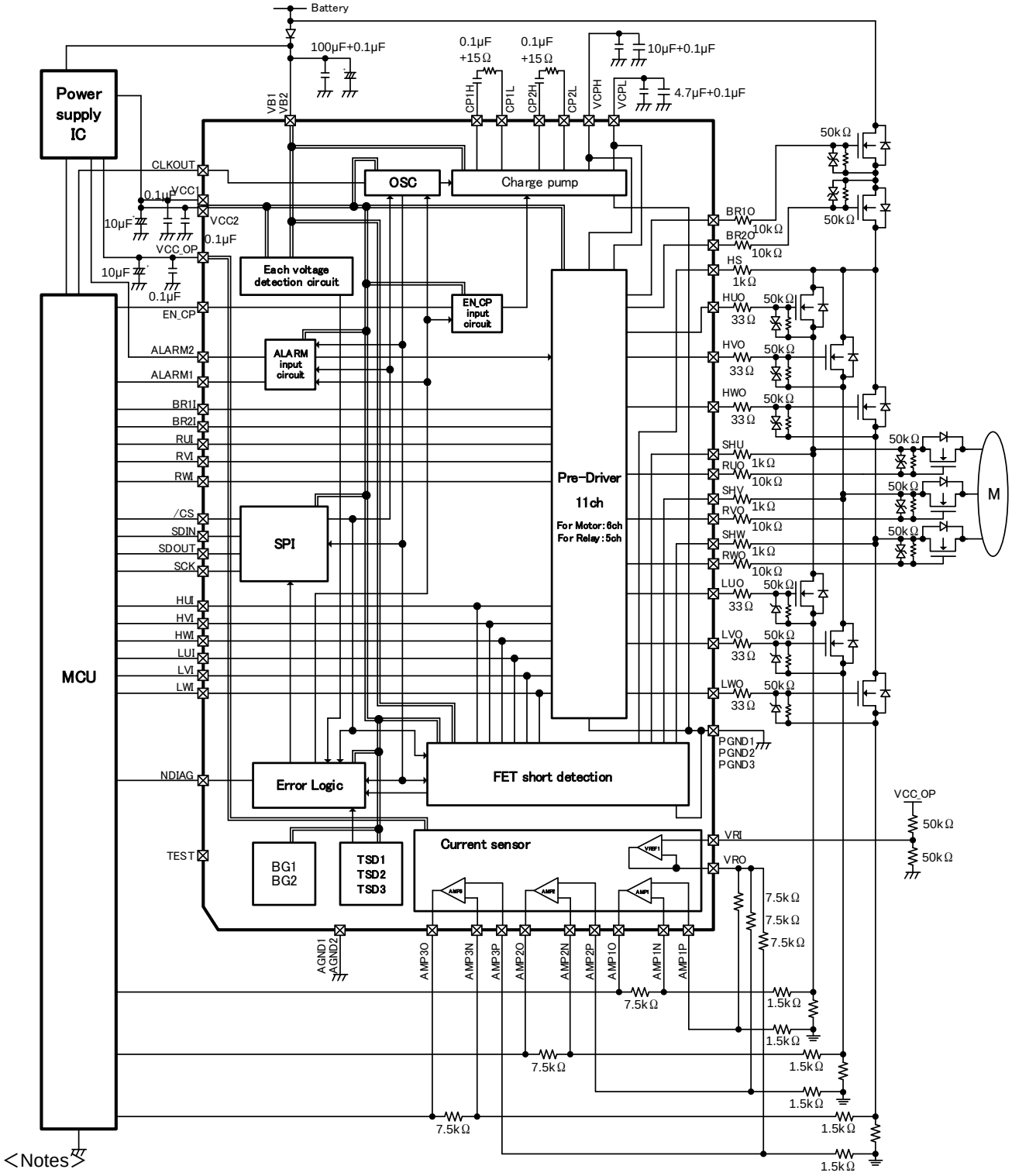


Fig.9-a SPI Communication circuit Block Diagram

Reference circuit diagram



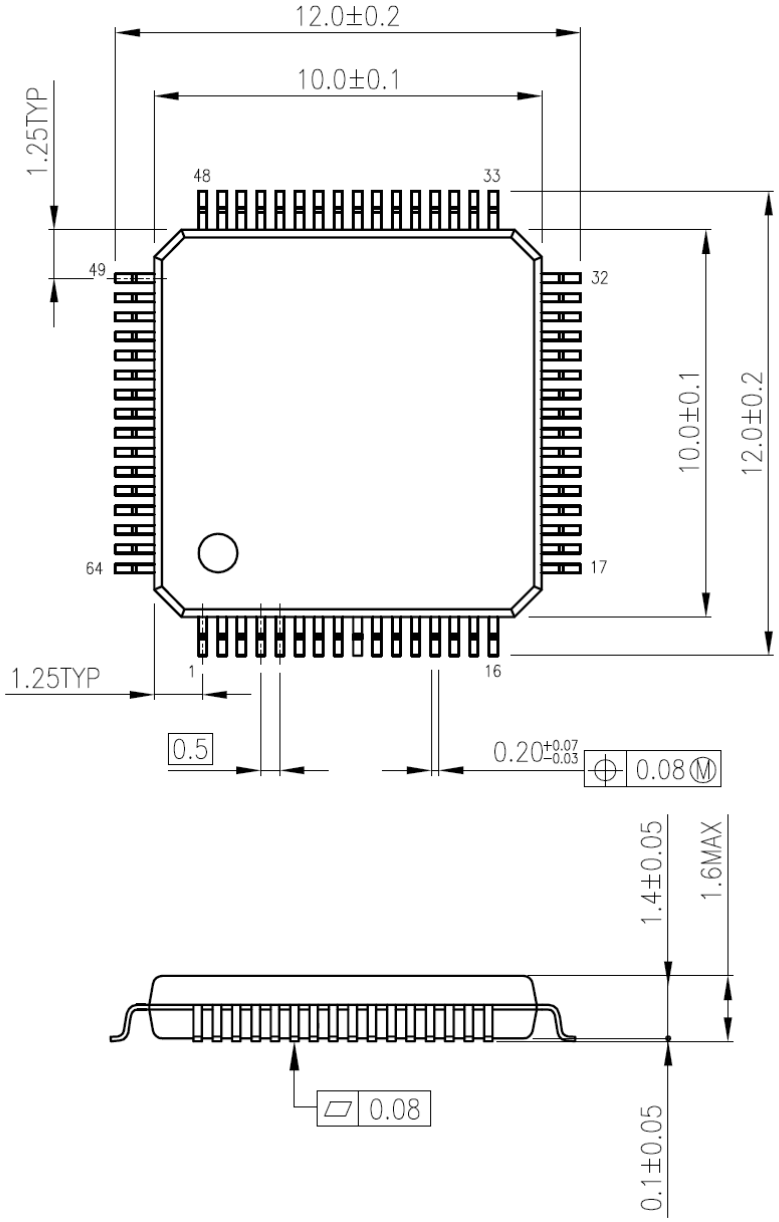
＜Notes＞

* These circuit constants are reference circuit examples, and are not guaranteed.
The external circuit should be decided after certainly evaluating and confirming on the unit board supposing the usage environment.
* The smoothing capacitor connected externally to the power supply terminals (VB1, VB2, VCC1, VCC2 and VCC_OP) should be the layout on the IC as close as possible.
*The power supply of the resistance partial pressure connected to the VRI terminal should be used as the same power supply as VCC_OP.
* AGND1, 2 and PGND1, 2, and 3 should be the solid GND (potential ±0.3V) on the unit board.
*Consider notes of each block at the time of a unit design.
* Do not implement incorrectly. The destruction of the ICs or the damage to the devices may occur.

PACKAGE

LQFP64-P-1010-0.50E

Unit: mm



Weight: 0.35 g (typ.)

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