

TLP7920,TLP7920F

1. Applications

- Motor phase and rail current sensing
- Power inverter current and voltage sensing

2. General

The TLP7920 and TLP7920F of isolation amplifiers is designed for current sensing in electronic motor drives. In a typical implementation, motor currents flow through an external resistor and the resulting analog voltage drop is sensed by the TLP7920 or TLP7920F.

3. Features

- (1) Output side supply voltage: 3.0 to 5.5 V
- (2) Output side supply current: 6.2 mA (typ.)
- (3) Operating temperature range: -40 to 105 °C
- (4) Common-mode transient immunity: 15 kV/μs (min)
- (5) Safety standards

UL-recognized: UL 1577, File No.E67349

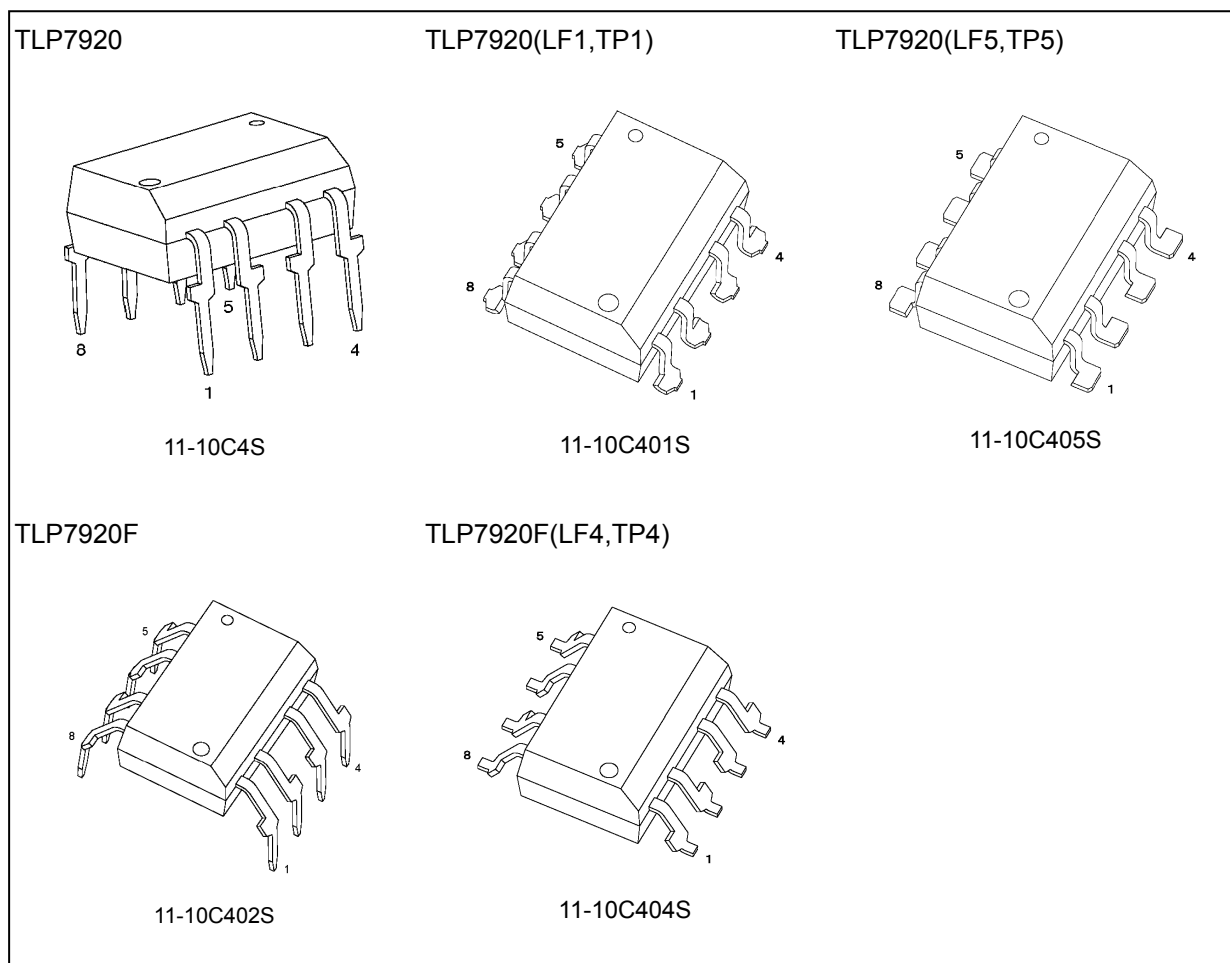
cUL-recognized: CSA Component Acceptance Service No.5A File No.E67349

VDE-approved: EN IEC 60747-5-5 (**Note 1**)

Note 1: When a VDE approved type is needed, please designate the **Option (D4)**.

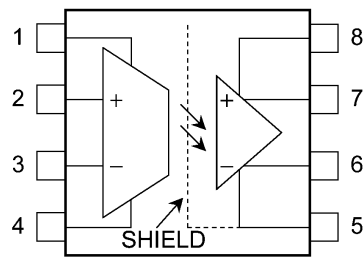
Start of commercial production
2015-09

4. Packaging (Note)



Note: Through-hole type: TLP7920, TLP7920F
 Lead forming option: (LF1),(LF4),(LF5)
 Taping option: (TP1),(TP4),(TP5)

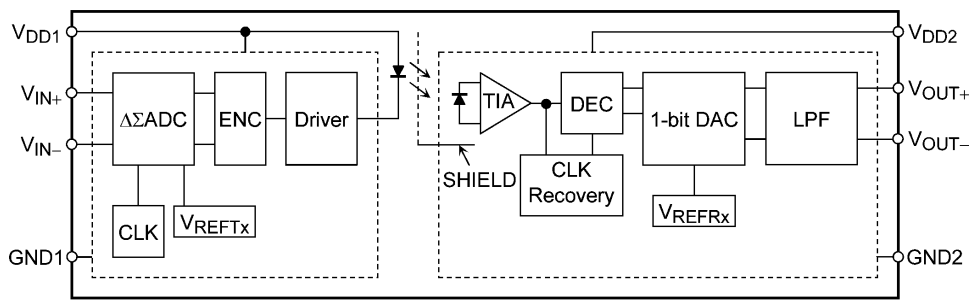
5. Pin Assignment



5.1. Pin Functions

Pin No.	Symbol	Description
1	V_{DD1}	Input side supply voltage
2	V_{IN+}	Positive input
3	V_{IN-}	Negative input
4	GND1	Input side ground
5	GND2	Output side ground
6	V_{OUT-}	Negative output
7	V_{OUT+}	Positive output
8	V_{DD2}	Output side supply voltage

6. Internal Circuit (Note)



Note: A 0.1 μ F bypass capacitor must be connected between 1 and 4 pins and between 5 and 8 pins.

7. Principle of Operation

7.1. Mechanical Parameters

Characteristics	7.62-mm Pitch TLP7920	10.16-mm Pitch TLP7920F	Unit
Creepage distances	7.0 (min)	8.0 (min)	mm
Clearance	7.0 (min)	8.0 (min)	
Internal isolation thickness	0.4 (min)	0.4 (min)	

8. Absolute Maximum Ratings (Note) (Unless otherwise specified, $T_a = 25\text{ }^{\circ}\text{C}$)

Characteristics	Symbol	Note	Rating	Unit
Supply voltages	V_{DD1}, V_{DD2}		-0.5 to 6	V
Steady-state input voltages	V_{IN+}, V_{IN-}		-0.5 to $V_{DD1} + 0.5$	
Two-second transient input voltages	V_{IN+}, V_{IN-}		-0.5 to 6	
Input power dissipation	P_D	(Note 1)	72	mW
Output voltages	V_{OUT+}, V_{OUT-}		-0.5 to 6	V
Output power dissipation	P_O	(Note 1)	60	mW
Operating temperature	T_{opr}		-40 to 105	$^{\circ}\text{C}$
Storage temperature	T_{stg}		-55 to 125	$^{\circ}\text{C}$
Lead soldering temperature (10 s)	T_{sol}	(Note 2)	260	$^{\circ}\text{C}$
Isolation voltage AC, 60 s, R.H. $\leq 60\%$	BV_S	(Note 3)	5000	Vrms

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note: Ceramic capacitors (0.1 μF) should be connected between 1 and 4 pins and between 5 and 8 pins to stabilize the operation. Otherwise, this photocoupler may not switch properly. The bypass capacitors should be placed as close as possible to each pin.

Note 1: Input power dissipation derating($T_a \geq 114.2\text{ }^{\circ}\text{C}$): -6.7 mW/ $^{\circ}\text{C}$

Output power dissipation derating($T_a \geq 116.0\text{ }^{\circ}\text{C}$): -6.7 mW/ $^{\circ}\text{C}$

Note 2: $\geq 2\text{ mm}$ below seating plane.

Note 3: This device is considered as a two-terminal device: Pins 1, 2, 3 and 4 are shorted together, and pins 5, 6, 7 and 8 are shorted together.

9. Recommended Operating Conditions (Note)

Characteristics	Symbol	Note	Min	Typ.	Max	Unit
Input side supply voltage	V_{DD1}		4.5	5	5.5	V
Output side supply voltage	V_{DD2}		3.0	—	5.5	
Analog input voltage	V_{IN+}, V_{IN-}	(Note 1), (Note 2)	-200	—	200	mV
Ambient temperature	T_a		-40	—	105	$^{\circ}\text{C}$

Note: The recommended operating conditions are given as a design guide necessary to obtain the intended performance of the device. Each parameter is an independent value. When creating a system design using this device, the electrical characteristics specified in this data sheet should also be considered.

Note 1: FSR = $\pm 300\text{ mV}$

Note 2: When either V_{IN+} or V_{IN-} or both are equal to or greater than $V_{DD1} - 2\text{ V}$ (e.g., if $V_{DD1} = 5\text{ V}$, when V_{IN+} and/or V_{IN-} are equal to or greater than $5\text{ V} - 2\text{ V} = 3\text{ V}$), isolation amplifiers go into one of the test modes. Do not raise either V_{IN+} or V_{IN-} above this voltage to keep the device in functional mode.

10. Electrical Characteristics

10.1. DC Characteristics (Unless otherwise specified, $T_a = -40$ to $105\text{ }^{\circ}\text{C}$, $V_{DD1} = 4.5$ to 5.5 V , $V_{DD2} = 3.0$ to 5.5 V , $V_{IN+} = -200$ to 200 mV , $V_{IN-} = 0\text{ V}$)

Characteristics	Symbol	Note	Test Condition	Min	Typ.	Max	Unit
Input offset voltage	V_{OS}		$T_a = 25\text{ }^{\circ}\text{C}$	-0.7	0.73	2.1	mV
Input offset voltage drift vs ambient temperature	$ dV_{OS}/dT_a $			—	3	10	$\mu\text{V}/^{\circ}\text{C}$
Input offset voltage drift vs input side supply voltage	$ dV_{OS}/dV_{DD1} $			—	120	—	$\mu\text{V}/\text{V}$
Gain (Rank B)	G_0	(Note 1)	$T_a = 25\text{ }^{\circ}\text{C}$	—	—	—	V/V
Gain (Rank A)	G_1	(Note 1)	$T_a = 25\text{ }^{\circ}\text{C}$	—	—	—	
Gain (None)	G_3	(Note 1)	$T_a = 25\text{ }^{\circ}\text{C}$	—	—	—	
Gain drift vs ambient temperature	$ dG/dT_a $			—	0.00012	—	$\text{V}/\text{V}/^{\circ}\text{C}$
V_{OUT} non-linearity ($\pm 200\text{ mV}$)	NL_{200}	(Note 2)	$V_{IN+} = -200$ to 200 mV , $T_a = 25\text{ }^{\circ}\text{C}$	—	0.02	0.13	%
V_{OUT} non-linearity ($\pm 200\text{ mV}$) drift vs ambient temperature	$ dNL_{200}/dT_a $			—	0.00007	—	$\%/^{\circ}\text{C}$
V_{OUT} non-linearity ($\pm 100\text{ mV}$)	NL_{100}	(Note 2)	$V_{IN+} = -100$ to 100 mV , $T_a = 25\text{ }^{\circ}\text{C}$	—	0.01	0.06	%
High-level output voltage	V_{OH}		$V_{IN+} = 400\text{ mV}$, $T_a = 25\text{ }^{\circ}\text{C}$	—	2.497	—	V
Low-level output voltage	V_{OL}		$V_{IN+} = -400\text{ mV}$, $T_a = 25\text{ }^{\circ}\text{C}$	—	0.0009	—	
Input common-mode rejection ratio	$CMRR_{IN}$			—	80	—	dB
Input bias current	I_{IN+}		$V_{IN+} = 0\text{ V}$, $T_a = 25\text{ }^{\circ}\text{C}$	-1	-0.055	—	μA
Input side supply current (V_{DD1})	I_{DD1}		$V_{IN+} = 0\text{ V}$	—	8.6	12	mA
Output side supply current (V_{DD2})	I_{DD2}		$V_{IN+} = 0\text{ V}$	—	6.2	10	mA
Equivalent input resistance	R_{IN}			—	80	—	$\text{k}\Omega$

Note 1: See Chapter 10.1.1 for gain rank values.

Note 2: The slope of the optimum line is derived by the method of least squares between differential input voltage ($V_{IN+} - V_{IN-}$) and differential output voltage ($V_{OUT+} - V_{OUT-}$). Nonlinearity is defined as a fraction of the half of the peak-to-peak value of differential output voltage deviation divided by the full-scale differential output voltage (OVR).

10.1.1. Gain Rank (Note) (Unless otherwise specified, $T_a = 25\text{ }^{\circ}\text{C}$)

Rank	Gain Rank Marking	Gain			Unit
		(Min)	(Typ.)	(Max)	
None ($\pm 3\%$)	Blank, A, B	7.95	8.2	8.44	V/V
Rank A ($\pm 1\%$)	A, B	8.12	8.2	8.28	
Rank B ($\pm 0.5\%$)	B	8.16	8.2	8.24	

Note: The gain is defined as the slope of the optimum line derived by the method of least squares between differential input voltage ($V_{IN+} - V_{IN-}$) and differential output voltage ($V_{OUT+} - V_{OUT-}$) in the recommended voltage range.

Note: Specify both the part number and a rank in this format when ordering.

Example: TLP7920(B,F(O

For safety standard certification, however, specify the part number alone.

Example: TLP7920(B,F(O \rightarrow TLP7920

10.2. AC Characteristics (Note) (Unless otherwise specified, $T_a = -40$ to $105\text{ }^\circ\text{C}$, $V_{DD1} = 4.5$ to 5.5 V , $V_{DD2} = 3.0$ to 5.5 V)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
V_{OUT} bandwidth (-3 dB)	f_{-3dB}	$V_{IN+} = 400\text{ mV}_{p-p}$, sine wave	140	230	—	kHz
V_{IN} to V_{OUT} propagation delay time (10 %-10 %)	t_{pD10}	$V_{IN+} = 0$ to $200\text{ mV}/\mu\text{s}$ step $C_L = 15\text{ pF}$	—	1.9	2.3	μs
V_{IN} to V_{OUT} propagation delay time (50 %-50 %)	t_{pD50}		—	2.3	2.6	
V_{IN} to V_{OUT} propagation delay time (90 %-90 %)	t_{pD90}		—	2.8	3.3	
V_{OUT} rise time	t_r		—	1.7	—	
V_{OUT} fall time	t_f		—	1.7	—	
Common-mode transient immunity	CMTI	$V_{CM} = 1\text{ kV}$, $T_a = 25\text{ }^\circ\text{C}$	15	20	—	kV/ μs

Note: All typical values are at $T_a = 25\text{ }^\circ\text{C}$.

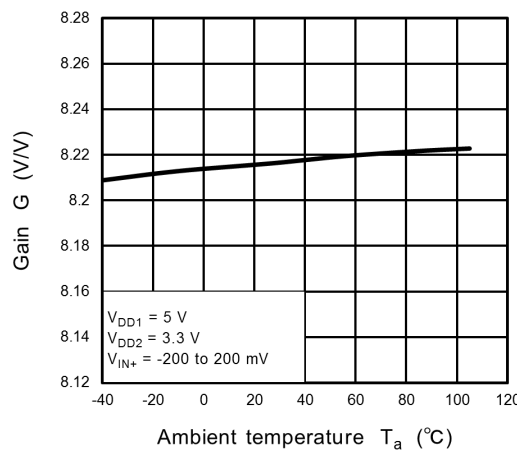
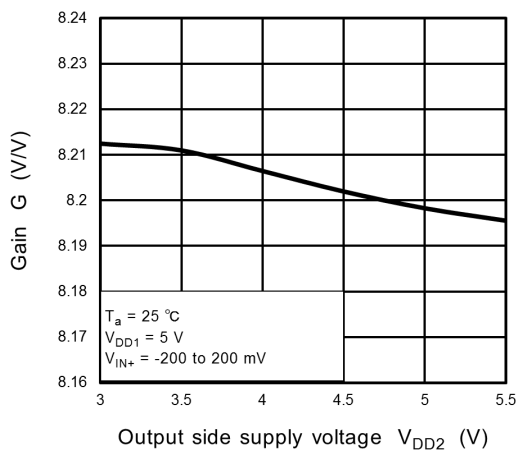
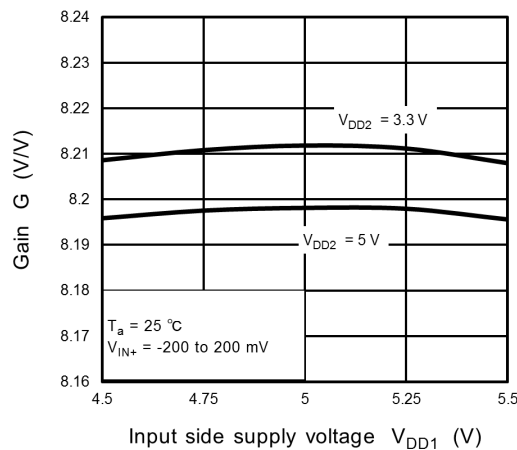
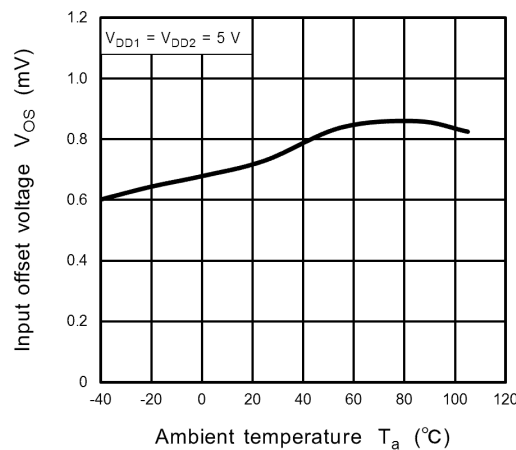
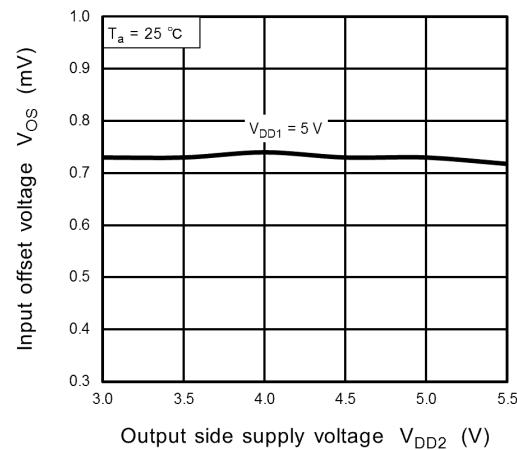
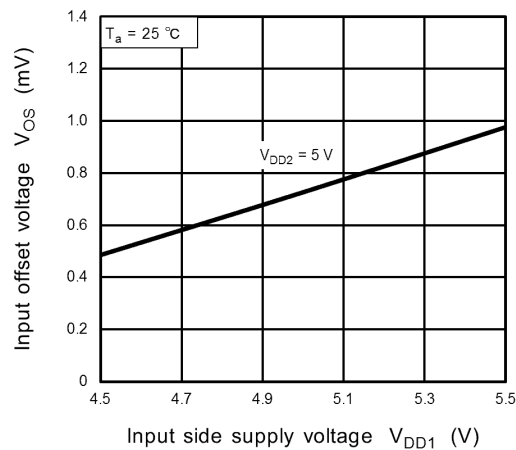
C_L is approximately 15 pF which includes probe and stray wiring capacitance.

11. Isolation Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$)

Characteristics	Symbol	Note	Test Condition	Min	Typ.	Max	Unit
Total capacitance (input to output)	C_S	(Note 1)	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$	—	1.0	—	pF
Isolation resistance	R_S	(Note 1)	$V_S = 500\text{ V}$, R.H. $\leq 60\%$	1×10^{12}	10^{14}	—	Ω
Isolation voltage	BV_S	(Note 1)	AC, 60 s	5000	—	—	V_{rms}
			AC, 1 s in oil	—	10000	—	
			DC, 60 s in oil	—	10000	—	Vdc

Note 1: This device is considered as a two-terminal device: Pins 1, 2, 3 and 4 are shorted together, and pins 5, 6, 7 and 8 are shorted together.

12. Characteristics Curves (Note)



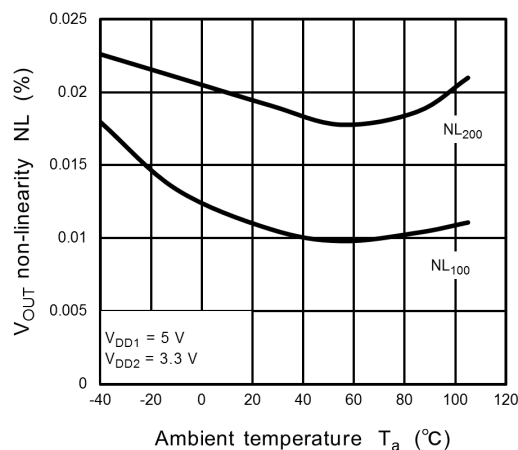


Fig. 12.7 NL - T_a

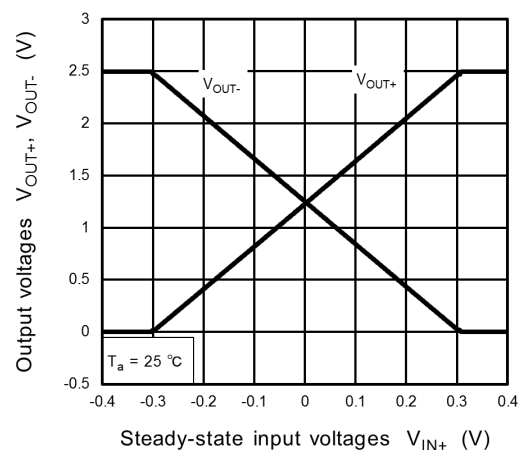


Fig. 12.8 $V_{OUT} - V_{IN+}$

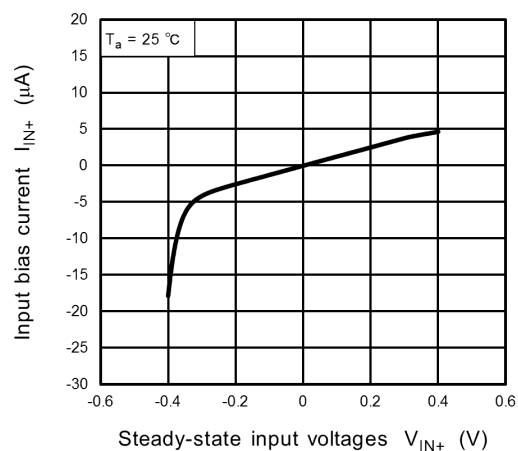


Fig. 12.9 $I_{IN+} - V_{IN+}$

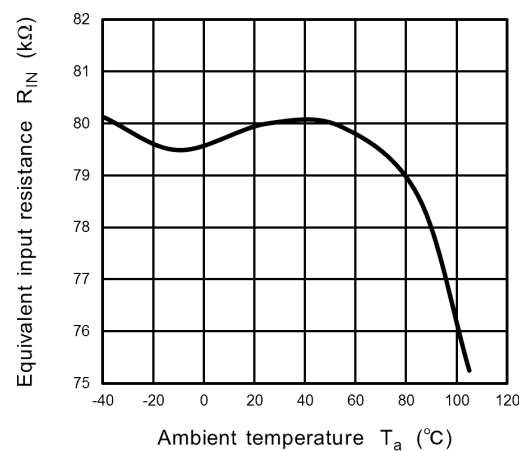


Fig. 12.10 $R_{IN} - T_a$

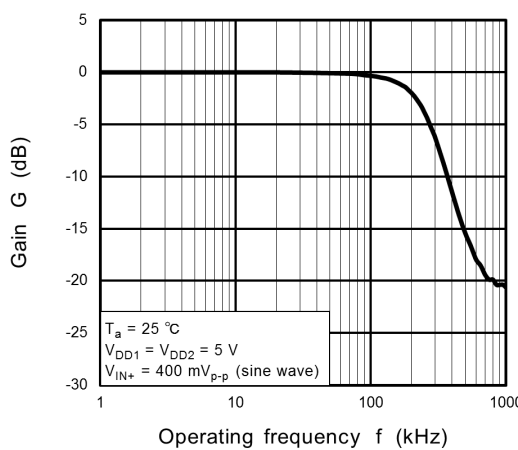


Fig. 12.11 $G[\text{dB}] - f$

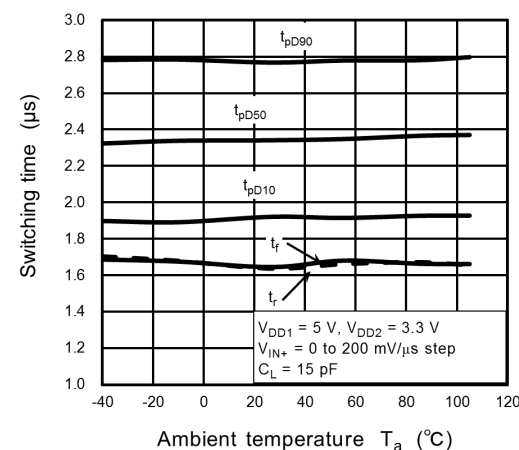


Fig. 12.12 Switching time - T_a

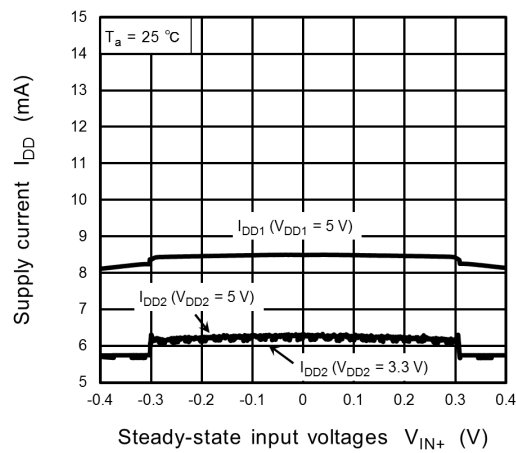


Fig. 12.13 $I_{DD} - V_{IN+}$

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

13. Soldering and Storage

13.1. Precautions for Soldering

The soldering temperature should be controlled as closely as possible to the conditions shown below, irrespective of whether a soldering iron or a reflow soldering method is used.

- When using soldering reflow.

The soldering temperature profile is based on the package surface temperature.

(See the figure shown below, which is based on the package surface temperature.)

Reflow soldering must be performed once or twice.

The mounting should be completed with the interval from the first to the last mountings being 2 weeks.

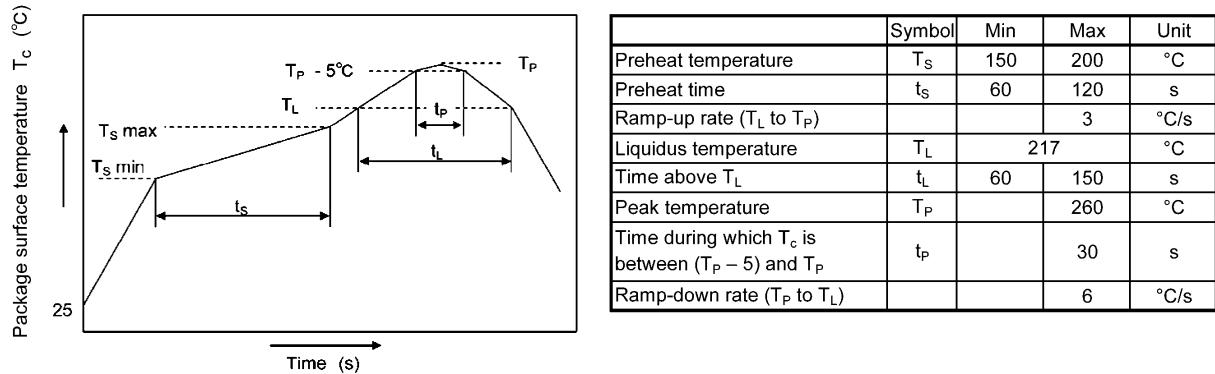


Fig. 13.1.1 An Example of a Temperature Profile When Lead(Pb)-Free Solder Is Used

- When using soldering flow

Preheat the device at a temperature of 150 °C (package surface temperature) for 60 to 120 seconds.

Mounting condition of 260 °C within 10 seconds is recommended.

Flow soldering must be performed once.

- When using soldering Iron

Complete soldering within 10 seconds for lead temperature not exceeding 260 °C or within 3 seconds not exceeding 350 °C

Heating by soldering iron must be done only once per lead.

13.2. Precautions for General Storage

- Avoid storage locations where devices may be exposed to moisture or direct sunlight.
- Follow the precautions printed on the packing label of the device for transportation and storage.
- Keep the storage location temperature and humidity within a range of 5 °C to 35 °C and 45 % to 75 %, respectively.
- Do not store the products in locations with poisonous gases (especially corrosive gases) or in dusty conditions.
- Store the products in locations with minimal temperature fluctuations. Rapid temperature changes during storage can cause condensation, resulting in lead oxidation or corrosion, which will deteriorate the solderability of the leads.
- When restoring devices after removal from their packing, use anti-static containers.
- Do not allow loads to be applied directly to devices while they are in storage.
- If devices have been stored for more than two years under normal storage conditions, it is recommended that you check the leads for ease of soldering prior to use.

14. Land Pattern Dimensions (for reference only)

Unit : mm

TLP7920

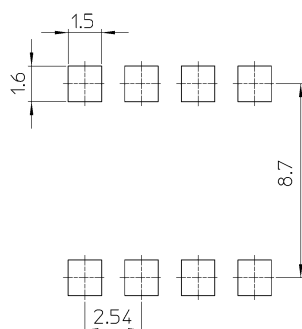


Fig. 14.1 Lead forming and taping option (LF1), (TP1), (LF5), (TP5)

TLP7920F

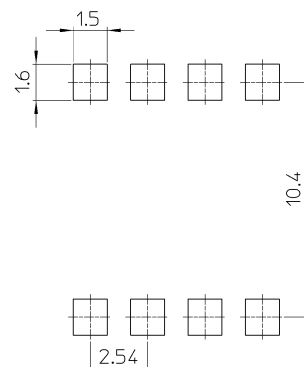
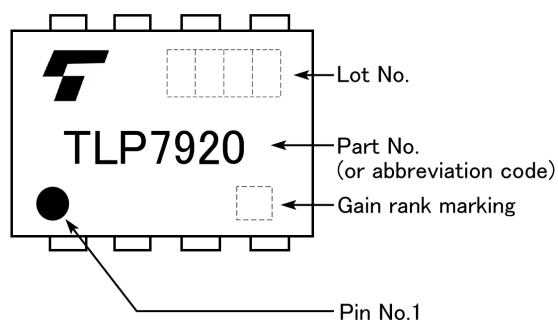


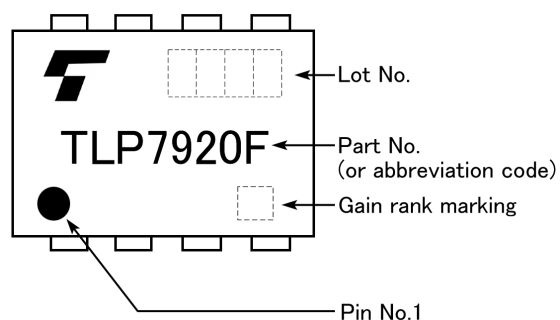
Fig. 14.2 Lead forming and taping option (LF4), (TP4)

15. Marking

TLP7920



TLP7920F



Note: A different marking is used for photocouplers that have been qualified according to option (D4) of EN IEC 60747. See Fig.16.3 and Fig.16.4.

16. EN IEC 60747-5-5 Option (D4) Specification

- Example: TLP7920 (Note 1)
- The following part naming conventions are used for the devices that have been qualified according to option (D4) of EN IEC 60747.

Example: TLP7920(D4ATP1,F(O

D4: EN IEC 60747 option

A: Gain Rank

TP1: Tape type

F: [[G]]/RoHS COMPATIBLE (Note 2)

(O: Domestic ID (Country / Region of origin: Japan)

Note 1: Use TOSHIBA standard type number for safety standard application.



e.g., TLP7920(D4ATP1,F(O → TLP7920

Note 2: Please contact your Toshiba sales representative for details on environmental information such as the product's RoHS compatibility.

RoHS is the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

Description		Symbol	Rating	Unit
Application classification				
for rated mains voltage ≤ 600 Vrms			I-IV	—
for rated mains voltage ≤ 1000 Vrms			I-III	—
Climatic classification			40 / 105 / 21	—
Pollution degree			2	—
Maximum operating insulation voltage	TLPxxx type	VIORM	890	Vpeak
	TLPxxxF type		1140	
Input to output test voltage, Method A $V_{pr} = 1.6 \times VIORM$, type and sample test $t_p = 10$ s, partial discharge < 5 pC	TLPxxx type	Vpr	1424	Vpeak
	TLPxxxF type		1824	
Input to output test voltage, Method B $V_{pr} = 1.875 \times VIORM$, 100 % production test $t_p = 1$ s, partial discharge < 5 pC	TLPxxx type	Vpr	1670	Vpeak
	TLPxxxF type		2140	
Highest permissible overvoltage (transient overvoltage, $t_{pr} = 60$ s)		VTR	8000	Vpeak
Safety limiting values (max. permissible ratings in case of fault, also refer to thermal derating curve)				
current (input current I_F , $P_{SO} = 0$)		Isi	400	mA
power (output or total power dissipation)		Pso	700	mW
temperature		Ts	150	°C
Insulation resistance $V_{IO} = 500$ V, $T_a = 25$ °C $V_{IO} = 500$ V, $T_a = 100$ °C $V_{IO} = 500$ V, $T_a = T_s$		Rsi	$\geq 10^{12}$ $\geq 10^{11}$ $\geq 10^9$	Ω

Fig. 16.1 EN IEC 60747 Insulation Characteristics

		 7.62 mm pitch TLPxxx type	 10.16 mm pitch TLPxxxF type
Minimum creepage distance	Cr	7.0 mm	8.0 mm
Minimum clearance	Cl	7.0 mm	8.0 mm
Minimum insulation thickness	ti	0.4 mm	
Comparative tracking index	CTI	175	

Insulation Related Specifications (Note)

- Note: If a printed circuit is incorporated, the creepage distance and clearance may be reduced below this value. (e.g., at a standard distance between soldering eye centers of 7.5 mm). If this is not permissible, the user shall take suitable measures.
- Note: This photocoupler is suitable for **safe electrical isolation** only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits.



Fig. 16.2 Marking on Packing for EN IEC 60747

TLP7920

TLP7920F

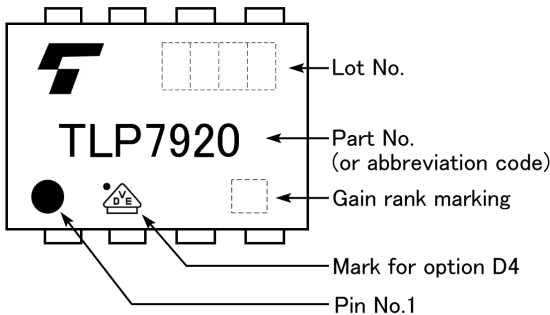


Fig. 16.3 Marking Example (Note)

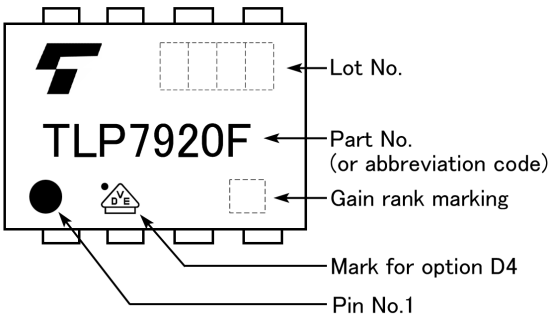
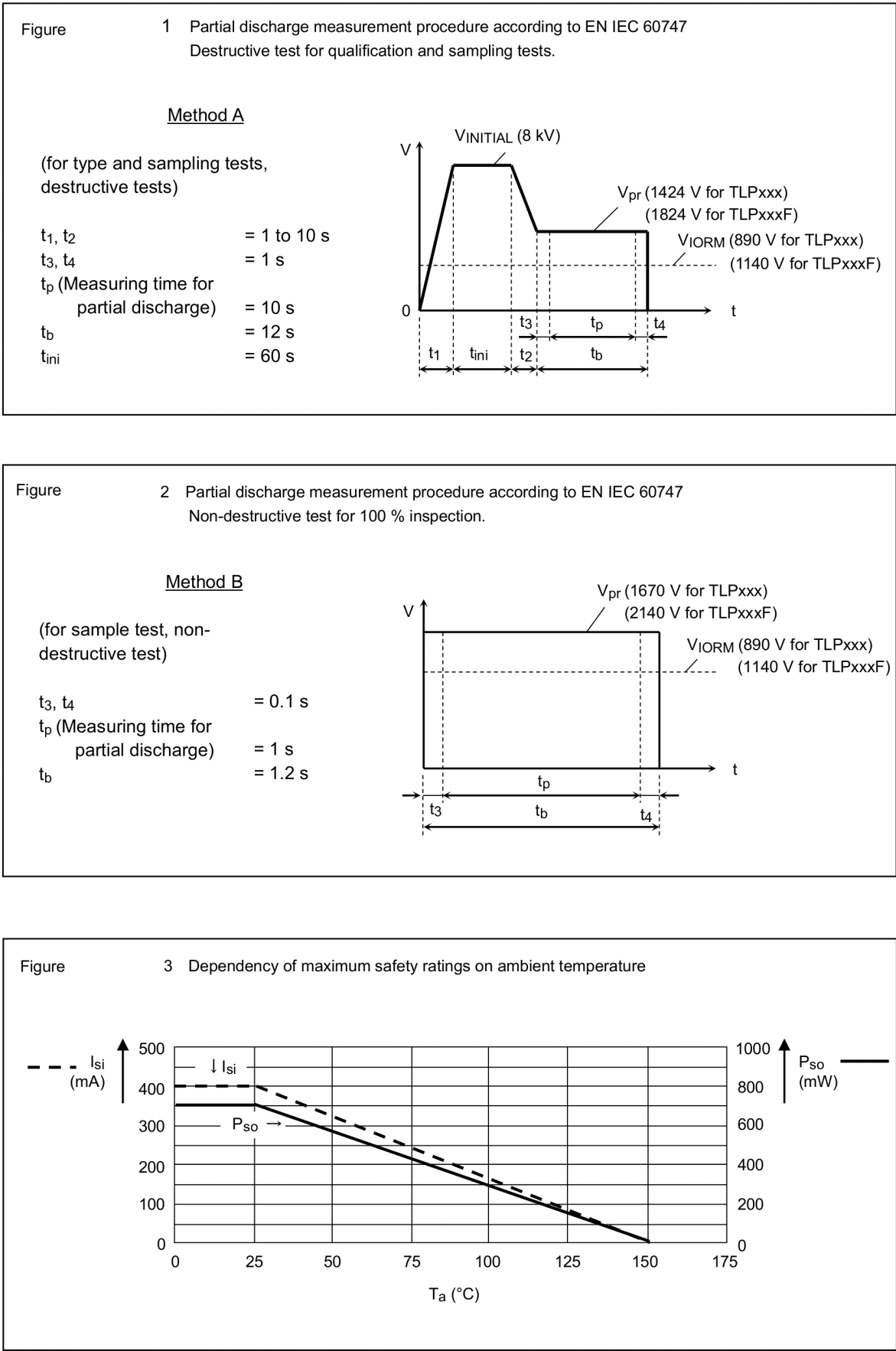


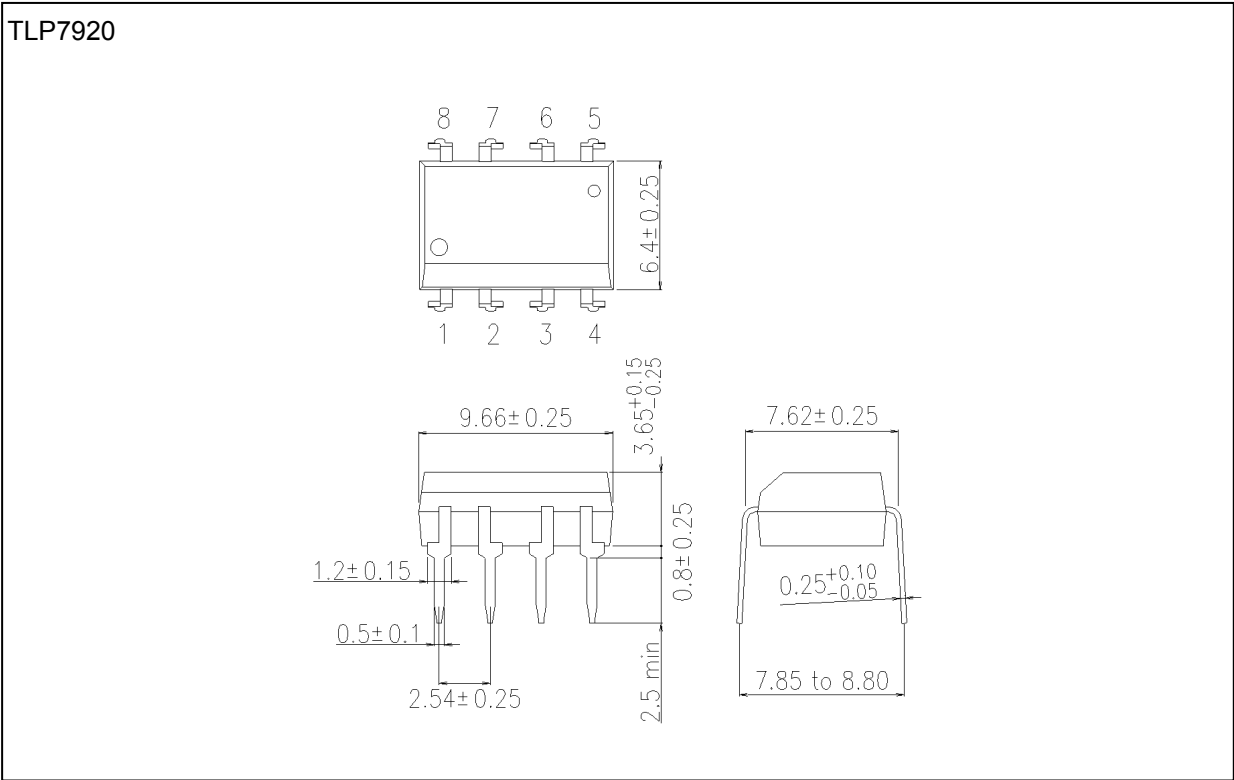
Fig. 16.4 Marking Example (Note)

- Note: The above marking is applied to the photocouplers that have been qualified according to option (D4) of EN IEC 60747.



Package Dimensions

Unit: mm

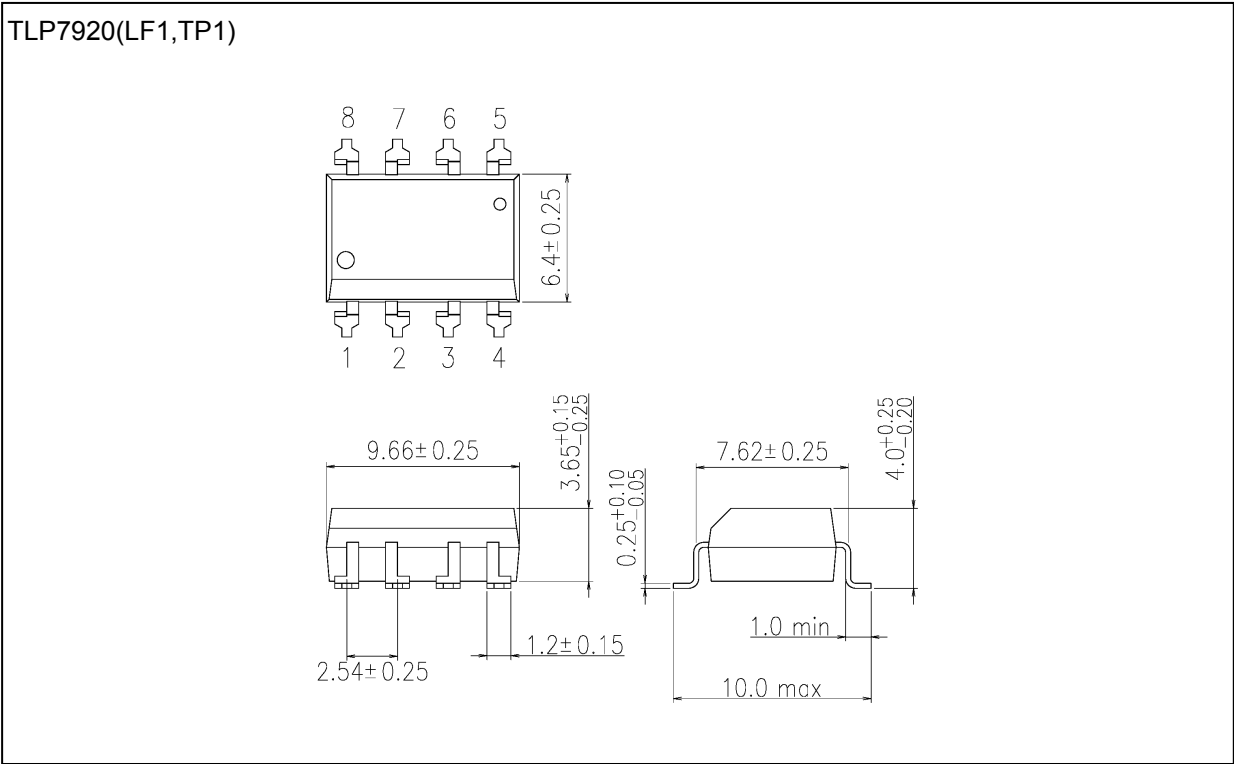


Weight: 0.54 g (typ.)

Package Name(s)
TOSHIBA: 11-10C4S

Package Dimensions

Unit: mm

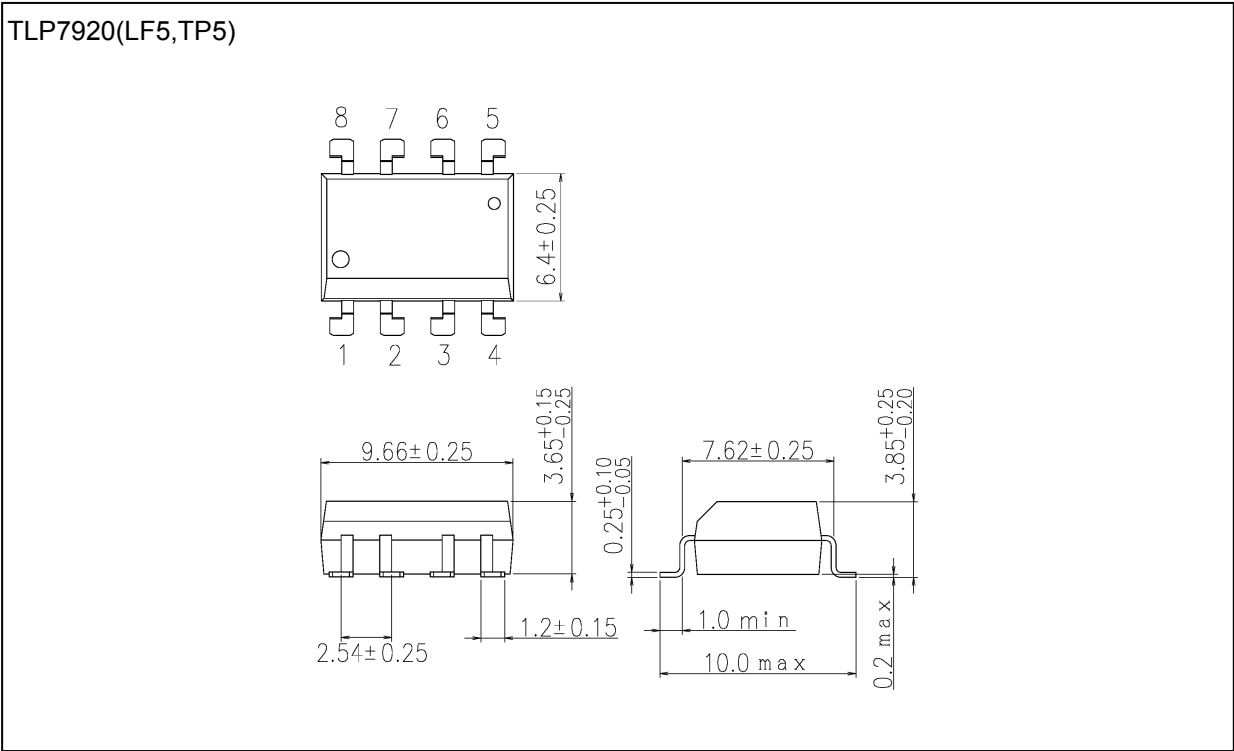


Weight: 0.53 g (typ.)

Package Name(s)
TOSHIBA: 11-10C401S

Package Dimensions

Unit: mm

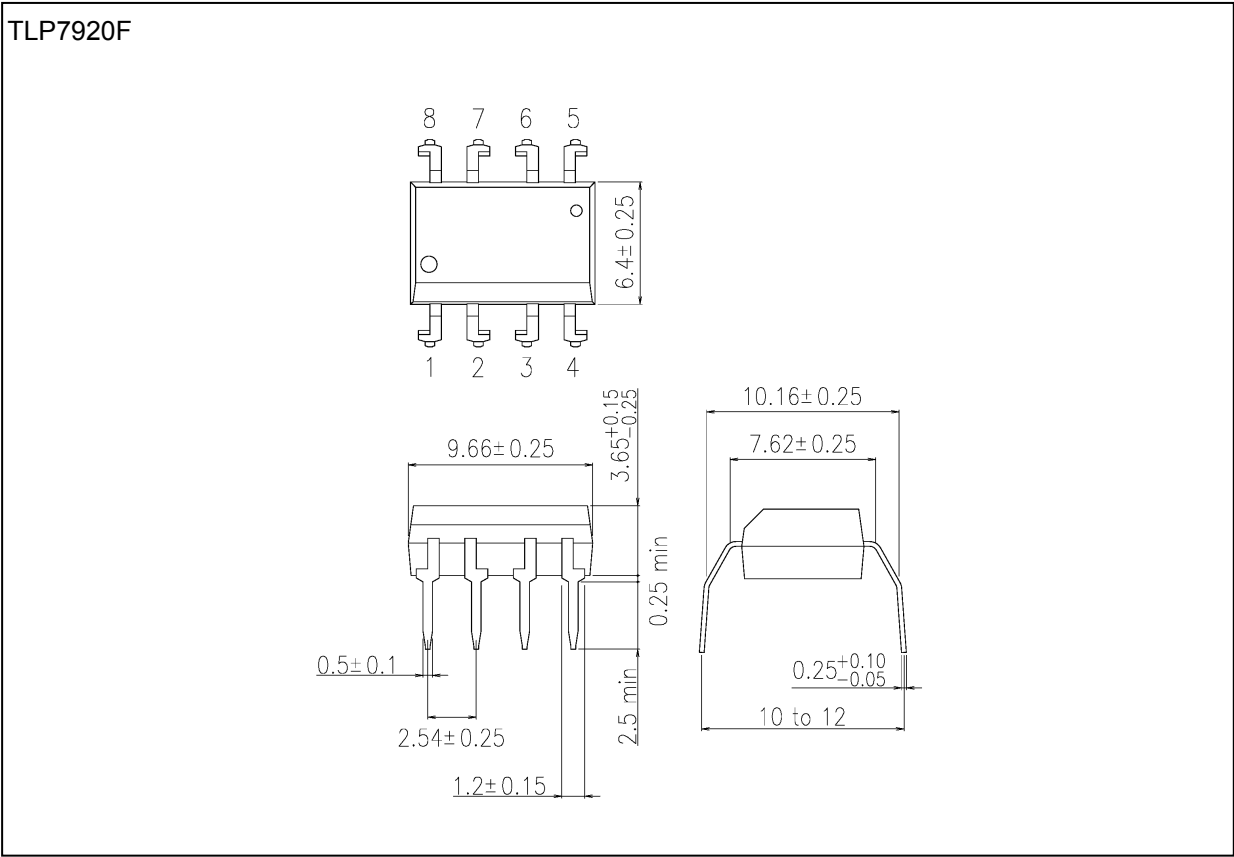


Weight: 0.53 g (typ.)

Package Name(s)
TOSHIBA: 11-10C405S

Package Dimensions

Unit: mm

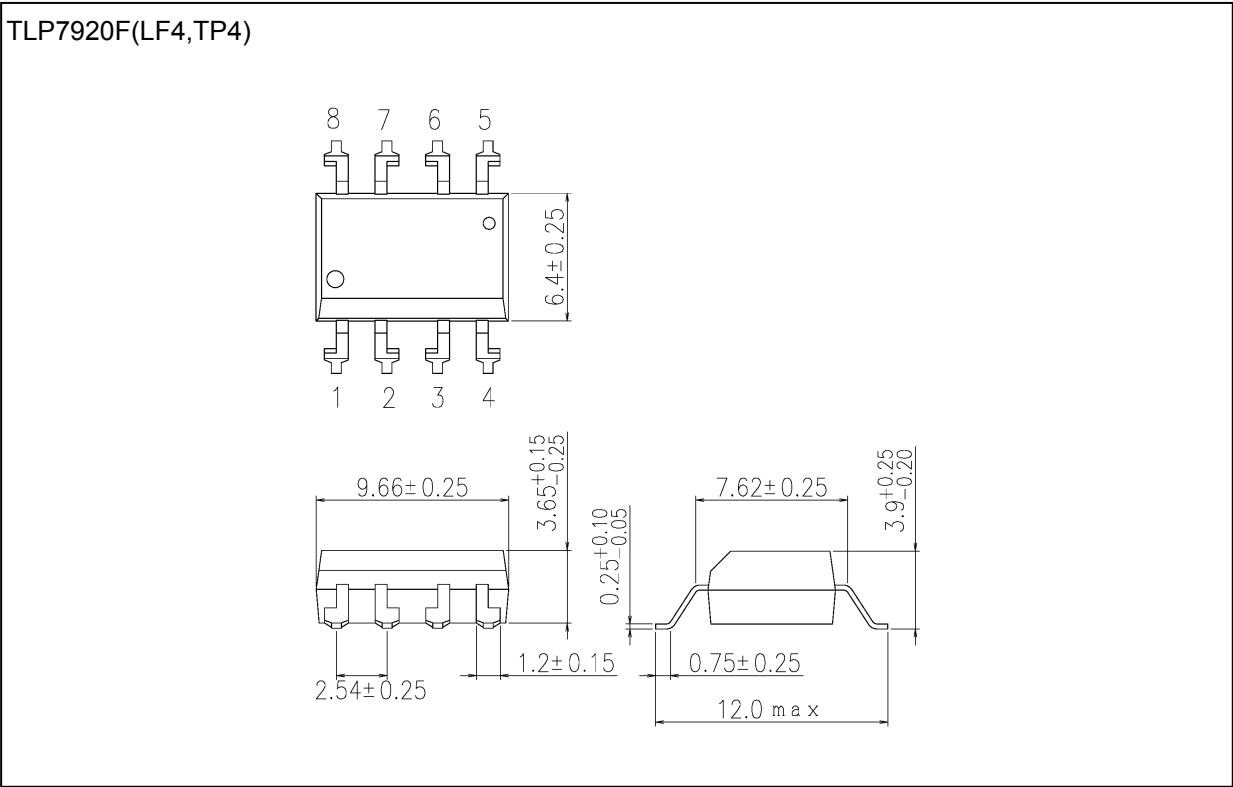


Weight: 0.54 g (typ.)

Package Name(s)
TOSHIBA: 11-10C402S

Package Dimensions

Unit: mm



Weight: 0.53 g (typ.)

Package Name(s)
TOSHIBA: 11-10C404S

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