Application Processor Lite *ApP Lite*

TZ1000 Series

Reference Manual

MCU Watchdog Timer

Revision 1.3

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TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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Preface

This document provides the specification for the MCU Watchdog Timer designed for the TZ1000 Series.

Intended Audience

This document is intended for the following users.

Driver software developers.

System designers

Conventions in this document

- The following notational conventions apply to numbers:
  Hexadecimal number: 0xABC
  Decimal number: 123 or 0d123 - Only when it should be explicitly indicated that the number is decimal.
  Binary number: 0b111 - It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- Low active signals are indicated with a name suffixed with "_N."
- A signal is asserted when it goes to its active level while it is deasserted when it goes to its inactive level.
- A set of multiple signals may be referred to as [m:n].
  Example: S[3:0] indicates four signals, S3, S2, S1 and S0, collectively.
- In the text, register names are enclosed in brackets *[ ]*.
  Example:*[ABCD]*
- A set of multiple registers, fields or bits of the same type may be described collectively using "n."
  Example: *[XYZ1]*, *[XYZ2]*, and *[XYZ3]* to *[XYZn]*
- A range of register bits are referred to as [m:n].
  Example: [3:0] indicates a range from bit 3 to bit 0.
- Values set in registers are indicated using either a hexadecimal or binary number.
- Example: *[ABCD]*.EFG = 0x01 (hexadecimal), *[XYZn]*.VW = 1 (binary)
- Words and bytes are defined as follows:
  Byte: 8 bits
  Halfword: 16 bits
  Word: 32 bits
  Doubleword: 64 bits
- Register bit attributes are defined as follows:
  R: Read-only
  W: Write-only
  W1C: Clear by write of 1 - A write of "1" clears the corresponding bit to 0.
  W1S: Set by write of 1 - A write of "1" sets the corresponding bit to 1.
  R/W: Read/Write
  R/W0C: Read/Clear by write of 0
  R/W1C: Read/Clear by write of 1
  R/W1S: Read/Set by write of 1
  RS/WC: Set by read/Clear by write - Set after a read and cleared after a data write.
- Registers only support word access unless otherwise specified.
- Any registers defined as Reserved in the text must not be rewritten. Also, any values read from such registers should not be used.
- Any bits for which default values are defined as "—" would return undefined values if read.
- When a data is written to a register containing both writable and read-only (R) bit fields, its default values should be written to read-only (R) bit fields. For any bit fields with default values defined as "—," refer to the definitions of the relevant register.
- Default values should be written to any reserved bit fields in a write-only register. For any bit fields with default values defined as "—," refer to the definitions of the relevant register.

Abbreviation

These specifications introduce a part of the abbreviation which they used

APB	Arm® AMBA® Peripheral Bus
RIS	Raw Interrupt Status
MIS	Masked Interrupt Status
PMU	Power Management Unit

1. Overview

This module is a watchdog timer and its features are as follows.

- Compliant with the AMBA® (2.0) protocol. The APB slave.
- 32-bit down counter with programmable timeout function
- Operation with the WDOGTCLK which synchronizes the APB clock PCLK
- Timeout interrupt output
- Timeout reset request output
- Register protection function by a lock register
- Interrupt output control and reset request output control by a test register

2. Block Diagram

The block diagram of this module is in the following figure.

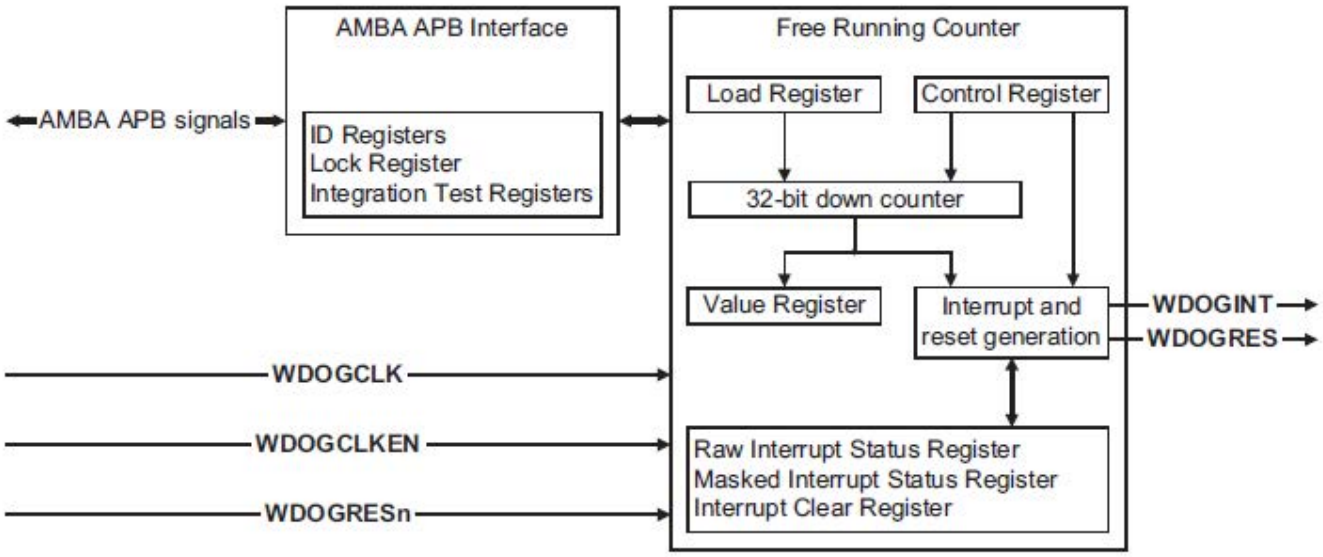

Figure 2.1 Watchdog timer internal block diagram

The outlines of the internal blocks of the watchdog timer (WDT) are as follows.

-AMBA® APB interfaces
- This block supports the APB slave interface to the CPU. It is used to access registers which are allocated in 4 KB address space.

-Free Running Counter
- A 32-bit down counter and circuits generating an interrupt signal and a reset request signal.

3. Address Map

Table 3.1 MCU Watchdog Timer Register Map

Register Name	Type	Width	Reset Value	Address Offset
WDT_WDOGLOAD	RW	32	0xFFFF FFFF	0x0000 0000
WDT_WDOGVALUE	RO	32	0xFFFF FFFF	0x0000 0004
WDT_WDOGCONTROL	RW	32	0x0000 0000	0x0000 0008
WDT_WDOGINTCLR	RW	32	0x0000 0000	0x0000 000C
WDT_WDOGRIS	RO	32	0x0000 0000	0x0000 0010
WDT_WDOGMIS	RO	32	0x0000 0000	0x0000 0014
WDT_WDOGLOCK	RW	32	0x0000 0000	0x0000 0C00
WDT_WDOGITCR	RW	32	0x0000 0000	0x0000 0F00
WDT_WDOGITOP	RW	32	0x0000 0000	0x0000 0F04
WDT_WDOGPERIPHID0	RO	32	0x0000 0005	0x0000 0FE0
WDT_WDOGPERIPHID1	RO	32	0x0000 0018	0x0000 0FE4
WDT_WDOGPERIPHID2	RO	32	0x0000 0014	0x0000 0FE8
WDT_WDOGPERIPHID3	RO	32	0x0000 0000	0x0000 0FEC
WDT_WDOGPCELLID0	RO	32	0x0000 000D	0x0000 0FF0
WDT_WDOGPCELLID1	RO	32	0x0000 00F0	0x0000 0FF4
WDT_WDOGPCELLID2	RO	32	0x0000 0005	0x0000 0FF8
WDT_WDOGPCELLID3	RO	32	0x0000 00B1	0x0000 0FFC

4. Input and Output Signals

4.1. Function Signals and WDT Signals

The function signals and the corresponding WDT signals are shown in the following table. The function signals are used in Section 5.

Table 4.1 Function signals and WDT signals

function signal name	WDT signal name	Description
PCLK	PCLK	Bus clock
WDOGCLK	WDOGCLK	WDT clock
PRESETn	PRESETn	Bus reset
WDOGRESn	WDOGRESn	WDT reset
WDOGCLKEN	WDOGCLKEN	WDT clock enable
PADDR	PADDR	APB signals
PENABLE	PENABLE	
PSEL	PSEL	
PWDATA	PWDATA	
PWRITE	PWRITE	
PRDATA	PRDATA	
WDOGINT	WDOGINT	Interrupt
WDOGRES	WDOGRES	System reset request

5. Function

In this section the function signal names are used. For the correspondence between the function signal names and the module signal names, refer to Table 4.1.

5.1. Clock

5.1.1. Clock and clock enable

The **PCLK, WDOGCLK,** and **WDOGCLKEN** are shown in the following figure. The count number is the watchdog timer count. The **WDOGCLK** and **WDOGCLKEN** synchronize the **PCLK.**

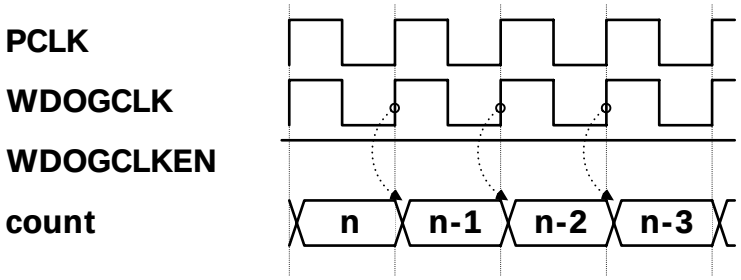

Figure 5.1 PCLK and WDOGCLK synchronization (WDOGCLKEN=1)

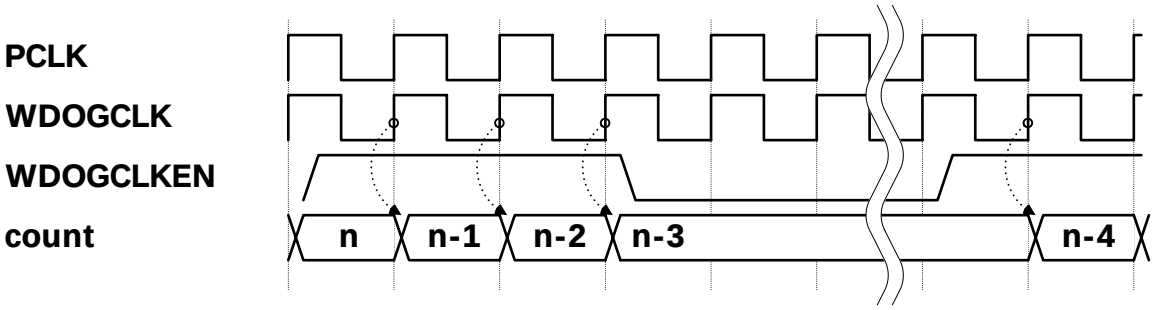

Figure 5.2 PCLK and WDOGCLK synchronization (WDOGCLKEN changes)

5.2. Watchdog Timer

5.2.1. Watchdog timer operation

The watchdog timer consists of a 32-bit down counter, a load register, an interrupt generator, and a system reset request generator.

After the reset is deasserted, the watchdog timer is disabled and it stops. When the period count of the watchdog timer is set to the load register ***[WDT_WDOGLOAD]*** and the INTEN bit (interrupt enable) in the control register ***[WDT_WDOGCONTROL]*** is set to 1, the down counter starts to operate. When the counter becomes 0x00000000, the watchdog timer issues an interrupt request to the CPU. At the same time, the watchdog timer loads the load register value and continues the down count. Usually, before the down counter becomes 0x00000000 again, the interrupt request is cleared. This interrupt request generation and clear procedure repeats.

If the RESETEN bit (system reset request enable) in the control register ***[WDT_WDOGCONTROL]*** is set to 1, the watchdog timer issues a system reset request to the PMU when the counter becomes 0x00000000 again without the clear of the interrupt request. (This request is received by the PMU, and the PMU decides whether to assert the system reset, or not. For detail, refer to the PMU specification.)

5.2.2. Lock register

The watchdog timer has a lock register *[WDT_WDOGLOCK]* which disables the other register writes. When the reset is deasserted, it enables the writes (unlock state).

Change to Lock state:
A value other than 0x1ACCE551 is written to *[WDT_WDOGLOCK].*
Change to Unlock state:
0x 1ACCE551 is written to *[WDT_WDOGLOCK]*.

The current status can be checked by reading *[WDT_WDOGLOCK]*.
0x00000001: Lock state
0x00000000: Unlock state

In the lock state, a write to all registers except *[WDT_WDOGLOCK] is disabled.*

5.2.3. Interrupt operation

The outline diagram of the interrupt generator is shown in Figure 5.4. The interrupt generation is controlled by a normal mode and a test mode. The mode selection is done by the ITEN bit in *[WDT_WDOGITCR]*. The normal mode is selected when the ITEN bit is set to 0.
In the normal mode, the INTEN bit in the control register *[WDT_WDOGCONTROL]* is set to 1, and when the down counter becomes 0x00000000, the interrupt request is generated. The interrupt generation and its clear timings are shown in Figure 5.3.
The interrupt request **WDOGINT** is asserted at the rising edge of the **WDGCLK** during **WDOGCLKEN**=1. The interrupt request **WDOGINT** is deasserted at the rising edge of the **PCLK** when the interrupt clear register *[WDT_WDOGINTCLR]* is written, regardless of the **WDOGCLKEN**. The internal interrupt cause is cleared at the rising edge of the **WDOGCLK** during **WDOGCLKEN**=1.

In the test mode, the TestWDOGINT in the *[WDT_WDOGITOP]* register controls the interrupt generation and its clear.

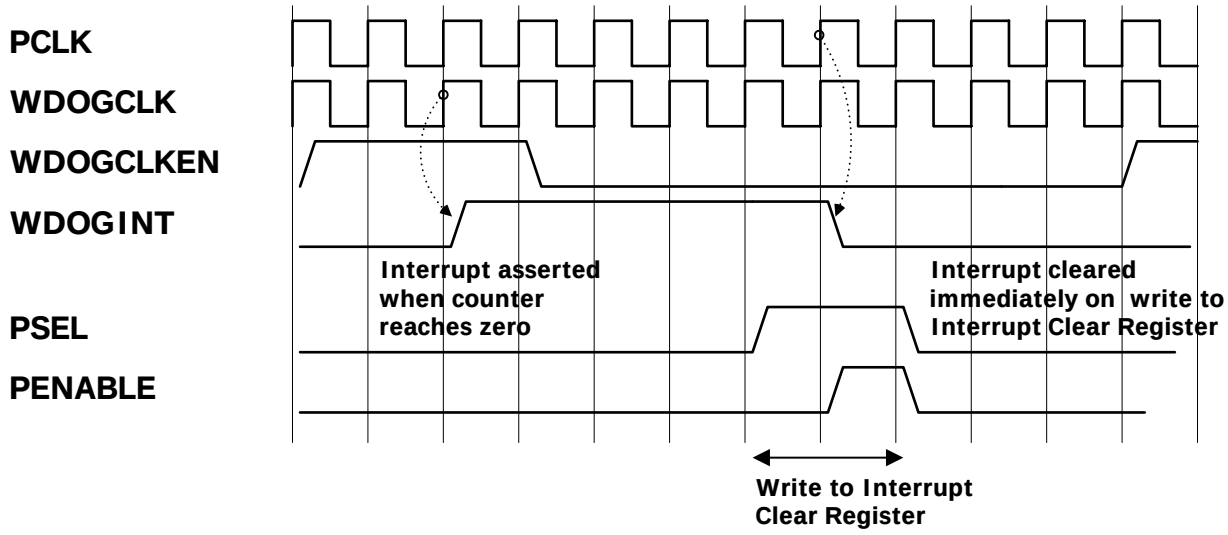

Figure 5.3 Example of interrupt timing chart

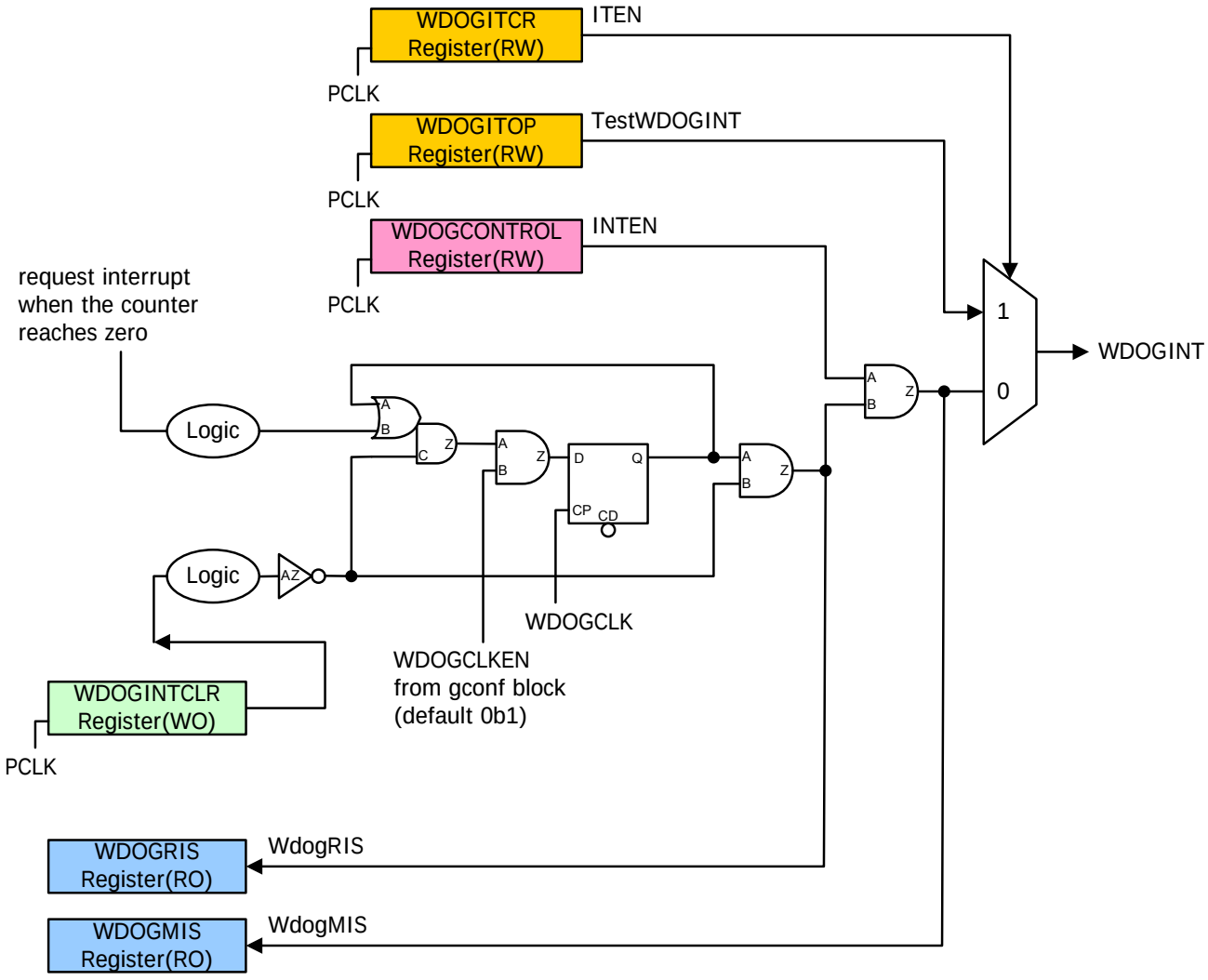

Figure 5.4 Interrupt generator

Interrupt generation interval is calculated with the following formula.

Interrupt generation interval = (WDOGLOAD +1) x (WDOGCLK period)

Table 5.1 Interrupt generation interval setting (WDOGCLK = 1 MHz)

Interrupt interval	WDOGLOAD Register	
	Hex	Decimal
1 ms	0x000003E7	999
5 ms	0x00001387	4999
100 ms	0x0001869F	99999
500 ms	0x0007A11F	499999
1 s	0x000F423F	999999
4294.967 s	0xFFFFFFFF	4294967295

Table 5.2 Interrupt generation interval setting (WDOGCLK = 12 MHz)

Interrupt Interval	WDOGLOAD Register	
	Hex	Decimal
1 ms	0x00002EDF	11999
5 ms	0x0000EA5F	59999
100 ms	0x00124F7F	1199999
500 ms	0x005B8D7F	5999999
1 s	0x00B71AFF	11999999
357.914 s	0xFFFFFFFF	4294967295

5.2.4. System reset request generation

The system reset request is generated when the down counter becomes 0x00000000 with setting the RESEN = 1 in the control register ***[WDT_WDOGCONTROL]***. This occurs the interrupt process has not cleared the counter before. This request is transferred to the PMU and the PMU controls the system reset.

The outline diagram of the system reset request generator is shown in the following figure. The request generation is controlled by a normal mode and a test mode. The mode selection is done by the ITEN bit in ***[WDT_WDOGITCR]***. The normal mode is selected when the ITEN bit is set to 0.

In the normal mode, the following operation generates the system reset request. At first, the INTEN and RESEN bits in the control register ***[WDT_WDOGCONTROL] are*** set to 1. When the down counter becomes 0x00000000, the interrupt request is generated. Unless the down counter is cleared, the counter becomes 0x00000000 again. Then, the system reset request is generated.

In the test mode, the TestWDOGRES in the ***[WDT_WDOGITOP]*** register controls the reset request generation and its clear.

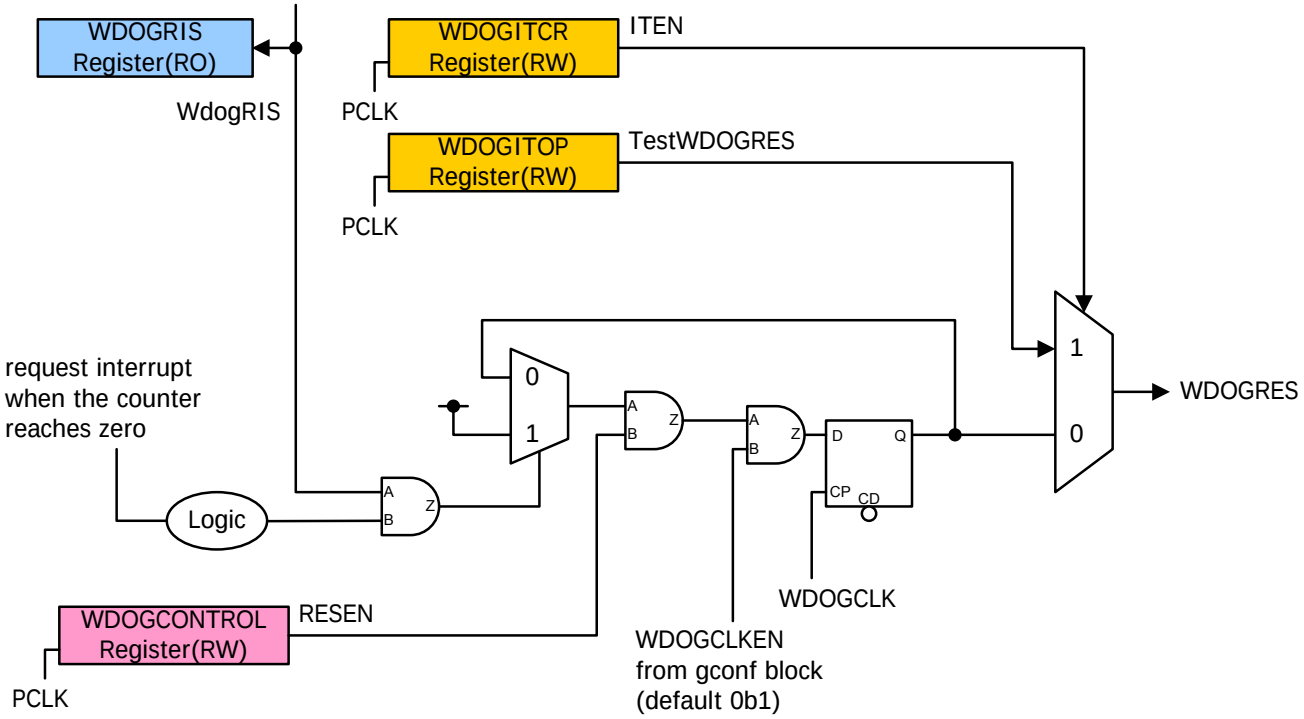

Figure 5.5 System reset request generator

5.3. Power Management

The power modes of the TZ1000 Series are shown in the following table.

Table 5.3 Power mode and operation

Power mode	State of WDT
ACTIVE	Run (Note)
SLEEP0	Run (Note)
SLEEP1	Run (Note)
SLEEP2	Clock gating
WAIT	Clock gating
RETENTION	Retention
RTC	Power Down
STOP	Power Down

Note: The clock can be started or stopped by software.

- ACTIVE/SLEEP0/SLEEP1:
  Normal operation.
  When the clock stop is set by software, the following should be noted. So, if an interrupt is asserted and the clock stops, the interrupt cannot be deasserted because of no clock operation. To prevent that, the clock should be stopped after the interrupt request is disabled in the *[WDT_WDOGCONTROL]* register.
  When the clock start is set, the counter re-starts with the same count where the clock stopped.
- SLEEP2/WAIT/RETENTION:
  The **PCLK** and **WDOGCLK** stop. Every signal holds its own data and the counter stops. if an interrupt is asserted and the clock stops, the interrupt cannot be deasserted because of no clock operation. To prevent that, the clock should be stopped after the interrupt request is disabled in the *[WDT_WDOGCONTROL]* register.
  When returning from this mode, every signal is restored to the data in the previous mode.
- RTC/STOP:
  Before the transition to this mode, it should be checked that each setting is done to disable the corresponding function.
  When returning from this mode, the registers are initialized. So, the operation should re-start after the configuration of the registers completes.

5.4. Start-up and Stop Procedure

5.4.1. Start-up procedure

The start-up procedure after power-on is as follows.
For detail of the PMU registers, refer to the PMU section.
The following setting is supposed that the main bus (the bus connected to the CPU) is supplied with a clock.
("*" shows the signal which also controls another function. The setting should be done together with another setting.)
The order of the setting procedure is a frequency setting at first, then clock supply, and reset deassertion at last.

- WDT clock frequency setting

PMU register	Bit name	Description
CSM_MAIN	CSMSEL_MAIN	0x0000000u u: 0x0: SiOSC4M, 0x1: OSC12M, 0x2: PLL, 0x3: ADPLL, 0x4: SC32K/SIOSC32K 0x5 – 0x7: reserved
PRESCAL_MAIN	PSSEL_CD_PPIER0	0x****u*** u: 0x0: not generate clock 0x1: divided by 1, 0x2: divided by 2, 0x3: divided by 3, 0x4: divided by 4, 0x5: divided by 5, 0x6: divided by 6, 0x7: divided by 7, 0x8: divided by 8, 0x9: divided by 9, 0xA: divided by 10, 0xB: divided by 12, 0xC: divided by 18, 0xD: divided by 24, 0xE: divided by 36, 0xF: divided by 48

Note: CSM_MAIN sets the source of the clock. The PLL is set by another register and the frequency is changed by the setting. (For detail, refer to the PMU section.)

Note: PRESCAL_MAIN has a setting to another power domain.

Note: PSSEL_CD_PPIER0 setting specifies all circuits in the PPIER0 power domain.

Note: The clock frequency setting can be changed even if the counter is operating. In this case, note that the period count is also changed.

The start-up sequence of the WDT is as follows.
Clock supply, then deassertion of the reset.

- WDT bus clock supply

PMU register	Bit name	value
CG_OFF_POWERDOMAIN	CG_PM	0x00000001
CG_OFF_PM_1	CG_ppier0clk_wdt_pclk	0x00000013
	CG_mpierclk_h2hp0_hclk	
	CG_ppier0clk_h2pp0_hclk	

Note: Bit 4 in the CG_OFF_PM_1 register corresponds to the WDT bus clock.

- WDT count clock supply

PMU register	Bit name	value
CG_OFF_PM_1	CG_ppier0clk_wdt_wdtclk	0x00000020

Note: Bit 5 in the CG_OFF_PM_1 register corresponds to the WDT count clock.

- Reset deassertion of the WDT

PMU register	Bit name	value
SRST_OFF_POWERDOMAIN	SRST_PM	0x00000001
SRST_OFF_PM_1	SRST_asyncrst_wdt_prstn	0x00000013
	SRST_asyncrst_h2pp0_hrstn	
	SRST_asyncrst_h2hp0_hrstn	

Note: Bit 4 in the SRST_OFF_PM_1 register corresponds to the WDT.

- WDT setting and start of the operation
  -After the reset deassertion, the WDT is disabled.
  The setting of the following registers starts the operation.

  -0x 1ACCE551 is written to the load register ***[WDT_WDOGLOCK]***.

  -Period count is set to the load register ***[WDT_WDOGLOAD]***.
  -The INTEN bit in the control register ***[WDT_WDOGCONTROL]*** is set to 1.
  -When the system reset request is generated, the RESEN bit in the control register ***[WDT_WDOGCONTROL]*** is set to 1.
  -A value other than 0x1ACCE551 is written to the load register ***[WDT_WDOGLOCK]***.

5.4.2. Stop procedure

- In the case that the WDT counter stops;
  The following two ways are used.
  -The WDT interrupt is disabled.
    - The INTEN bit in the control register ***[WDT_WDOGCONTROL]*** is set to 0.
      This stops the counter operation.

  -The period count is set to 0.
    - The load register ***[WDT_WDOGLOAD]*** is set to 0x00000000.
      This stops the counter operation.
- In the case that the WDT is not used (the whole block stops);
  The following two ways are used.
  -No reset assertion
    - Only the clock supply is stopped by the following PMU register setting.
  -Reset assertion
    - The reset assertion and the clock stop are set by the following PMU register.

- WDT reset

PMU register	Bit name	value
SRST_ON_PM_1	SRST_asyncrst_wdt_prstn	0x00000010

Note: Bit 4 in the SRST_ON_PM_1 register corresponds to the WDT.

- WDT counter clock stop

PMU register	Bit name	value
CG_ON_PM_1	CG_ppier0clk_wdt_wdtclk	0x00000020

Note: Bit 5 in the CG_ON_PM_1 register corresponds to the WDT count clock.

- WDT bus clock stop

PMU register	Bit name	value
CG_ON_PM_1	CG_ppier0clk_wdt_pclk	0x00000010

Note: Bit 4 in the CG_ON_PM_1 register corresponds to the WDT bus clock.

5.5. Dynamic Clock Gating Setting Procedure

The TZ1000 Series can be set to stop the clock supply unless the clock is necessary. When it is set, the following operation reduces the power dissipation.

("*" shows the signal which also controls another function. The setting should be done together with another setting.)

- Clock supply only when the bus access to the WDT.
- When the WDT is disabled (INTEN = 0 in the control register ***[WDT_WDOGCONTROL]***), the counter clock supply stops.

- WDT dynamic clock gating setting

PMU register	Bit name	value
DCG_POWERDOMAIN	DCG_PM	0x*******1
DCG_PM_0	DCG_mpierclk_mpier_hclk	0x*******1
DCG_PM_1	DCG_ppier0clk_wdt_wdtclk	0x******33
	DCG_ppier0clk_wdt_pclk	
	DCG_ppier0clk_h2pp0_hclk	
	DCG_mpierclk_h2hp0_hclk	

The setting is applied to all channels in the WDT. If each channel is set separately, the assigned bit should be written to 1.

DCG_PM_1 register: bit 5 the WDT count clock

DCG_PM_1 register: bit 4 the WDT bus clock

The setting of the dynamic clock gating can be cleared by writing 0 to the corresponding bit.

- WDT dynamic clock gating deassertion (WDT only)

PMU register	Bit name	value
DCG_PM_1	DCG_ppier0clk_wdt_wdtclk	0x******03
	DCG_ppier0clk_wdt_pclk	

6. Precaution for Usage

6.1. Access Restriction Associated with Register Access

The registers in this module are assigned to a 4 KB space with 32-bit interval in the little endian format. The bit locations are as follows.

This module is connected to the main data bus (the bus connected to the CPU) with 32-bit wide. When 8-bit or 16-bit data is accessed, the operation is in units of 32-bit only. This means that the 8-bit or 16-bit access causes the wrong write or read of the register bits other than the target bits. So, 32-bit access is recommended. Otherwise, a read error or a write error may occur.

The write to a non-existing bit in a register is ignored. The read of the bit returns 0.

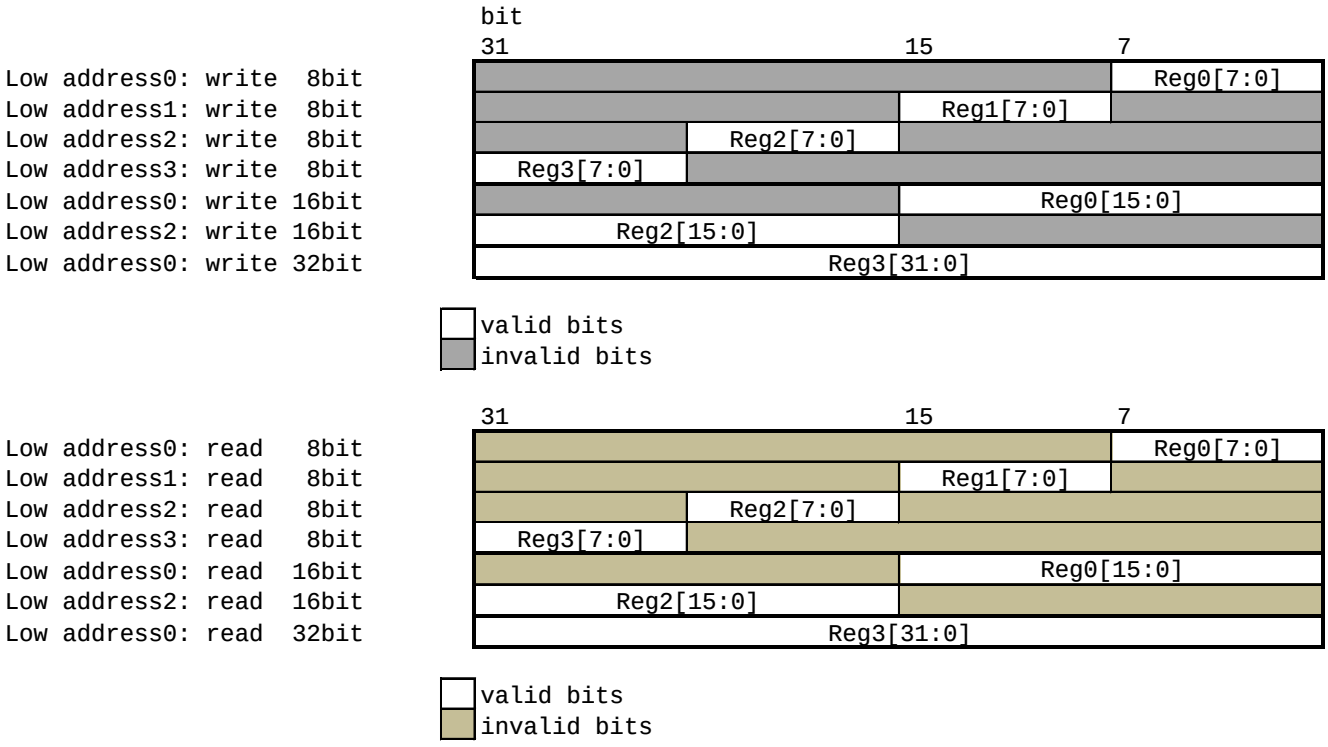

Figure 6.1 Bit allocation of register access

6.2. Precaution for Dynamic Clock Gating

When the dynamic clock gating is set, the following should be noted. When the interrupt generation and the interrupt cause are cleared, the WDT counter clock (**WDOGCLK**) is necessary. The clear can be done only when the operation is enabled (Enable=1 in the register *[WDT_WDOGCONTROL]*.

6.3. Using SIOSC4M as the source clock for WDT clock

Although SIOSC4M can be selected as the source of WDOGCLK, frequency of SIOSC4M may have variation of 4 MHz ± 3.5% due to temperature and/or voltage change. Note that the frequency variation is inherent in WDOGCLK and affect timer operation such as interrupt generation interval when SIOSC4M is used as the source of WDOGCLK.

7. Details of Registers

7.1. WDT_WDOGLOAD

WDT_WDOGLOAD				
Description	Wdog Watchdog load Register			
Address Region	wdt	**Type:**	RW	
Offset	0x0000 0000			
Physical address View0	0x4004 3000			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	Load	Value to be loaded to the Wdog counter (min 0x0000_0001) For the 0x00000000 setting, the counter does not operate. Setting other numeric values enable counting.	RW modify	0xFFFF FFFF

7.2. WDT_WDOGVALUE

WDT_WDOGVALUE				
Description	Wdog The current value for the watchdog counter Register			
Address Region	wdt	**Type:**	RO	
Offset	0x0000 0004			
Physical address View0	0x4004 3004			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	Value	Counter value of the Wdog counter at the current time	RO	0xFFFF FFFF

7.3. WDT_WDOGCONTROL

WDT_WDOGCONTROL				
Description	Wdog Control Register			
Address Region	wdt	**Type:**	RW	
Offset	0x0000 0008			
Physical address View0	0x4004 3008			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:2	Reserved	-	-	-
1	RESEN	WDOGRES output enable 0b1: Enable 0b0: Disable	RW modify	0
0	INTEN	Wdog interrupt enable 0b1: Enable 0b0: Disable (Note) For the generation timing of WDOGRES and Wdog interrupts, the	RW modify	0

		Wdog interrupt first occurs and then the WDOGRES interrupt occurs when the value of the Wdog counter becomes 0 again with the interrupt not cleared.		

7.4. WDT_WDOGINTCLR

WDT_WDOGINTCLR			
Description	Wdog Interrupt clear Register		
Address Region	wdt	**Type:**	RW
Offset	0x0000 000C		
Physical address View0	0x4004 300C		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:0	IntClr	Interrupt clear After the Wdog interrupt occurs, it can be cleared by write access to this register.	RW clear	0x0000 0000

7.5. WDT_WDOGRIS

WDT_WDOGRIS			
Description	Wdog Raw Interrupt Status Register		
Address Region	wdt	**Type:**	RO
Offset	0x0000 0010		
Physical address View0	0x4004 3010		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:1	Reserved	-	-	-
0	RIS	Wdog interrupt before masking is occurring. 0b1: Interrupt request available 0b0: No interrupt request	RO	0

7.6. WDT_WDOGMIS

WDT_WDOGMIS				
Description	Wdog Masked Interrupt Status Register			
Address Region	wdt	**Type:**	RO	
Offset	0x0000 0014			
Physical address View0	0x4004 3014			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	MIS	Wdog interrupt after masking is occurring. 0b1: Interrupt request available 0b0: No interrupt request	RO	0

7.7. WDT_WDOGLOCK

WDT_WDOGLOCK				
Description	Wdog Lock Register			
Address Region	wdt	**Type:**	RW	
Offset	0x0000 0C00			
Physical address View0	0x4004 3C00			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	WLOCK	Register writing disable control <Write> If 0x1ACCE551 is written in this register, register writing is enabled. If any value other than 0x1ACCE551 is written, register writing is disabled. <Read> Register writing disable status 0b1: Writing disable 0b0: Writing enable	RW modify	0

7.8. WDT_WDOGITCR

WDT_WDOGITCR				
Description	Timer Integration test control Register			
Address Region	wdt	**Type:**	RW	
Offset	0x0000 0F00			
Physical address View0	0x4004 3F00			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-

0	ITEN	Test mode control 0b1: Test mode 0b0: Normal operation	RW modify	0

7.9. WDT_WDOGITOP

WDT_WDOGITOP			
Description	Timer Integration test output set Register		
Address Region	wdt	**Type:**	RW
Offset	0x0000 0F04		
Physical address View0	0x4004 3F04		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:2	Reserved	-	-	-
1	TestWDOGINT	Outputs the WDOGINT signal (only in test mode, write-only) 0b1: WDOGINT="1" 0b0: WDOGINT="0" If this register is read, the WDT_WDOGITCR value appears.	RW modify	0
0	TestWDOGRES	Outputs the WDOGRES signal (only in test mode, write-only) 0b1: WDOGRES="1" 0b0: WDOGRES="0" If this register is read, the WDT_WDOGITCR value appears.	RW modify	0

7.10. WDT_WDOGPERIPHID0

WDT_WDOGPERIPHID0			
Description	Wdog Peripheral ID0 Register		
Address Region	wdt	**Type:**	RO
Offset	0x0000 0FE0		
Physical address View0	0x4004 3FE0		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:8	Reserved	-	-	-
7:0	Partnumber0	Peripheral ID (this register stores a value from a hardware viewpoint.) Partnumber(Lower) 804=>04	RO	0x05

7.11. WDT_WDOGPERIPHID1

WDT_WDOGPERIPHID1			
Description	Wdog Peripheral ID1 Register		
Address Region	wdt	**Type:**	RO
Offset	0x0000 0FE4		
Physical address View0	0x4004 3FE4		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:4	Designer0	Peripheral ID (this register stores a value from a hardware viewpoint.) Designer(Lower) 41=>1	RO	0x1
3:0	Partnumber1	Peripheral ID (this register stores a value from a hardware viewpoint.) Partnumber(Lower) 805=>8	RO	0x8

7.12. WDT_WDOGPERIPHID2

WDT_WDOGPERIPHID2			
Description	Wdog Peripheral ID2 Register		
Address Region	wdt	**Type:**	RO
Offset	0x0000 0FE8		
Physical address View0	0x4004 3FE8		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:4	Revision_number	Peripheral ID (this register stores a value from a hardware viewpoint.) Revision: 1st=>1	RO	0x1
3:0	Designer1	Peripheral ID (this register stores a value from a hardware viewpoint.) Designer(Upper) 41=>4	RO	0x4

7.13. WDT_WDOGPERIPHID3

WDT_WDOGPERIPHID3			
Description	Wdog Peripheral ID3 Register		
Address Region	wdt	**Type:**	RO
Offset	0x0000 0FEC		
Physical address View0	0x4004 3FEC		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	Configuration	Peripheral ID (this register stores a value from a hardware viewpoint.) Configuration: 00	RO	0x00

7.14. WDT_WDOGPCELLID0

WDT_WDOGPCELLID0			
Description	Wdog PrimeCell ID0 Register		
Address Region	wdt	**Type:**	RO
Offset	0x0000 0FF0		
Physical address View0	0x4004 3FF0		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	PCellID0	Peripheral ID (this register stores a value from a hardware viewpoint.)	RO	0x0D

7.15. WDT_WDOGPCELLID1

WDT_WDOGPCELLID1			
Description	Wdog PrimeCell ID1 Register		
Address Region	wdt	**Type:**	RO
Offset	0x0000 0FF4		
Physical address View0	0x4004 3FF4		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	PCellID1	Peripheral ID (this register stores a value from a hardware viewpoint.)	RO	0xF0

7.16. WDT_WDOGPCELLID2

WDT_WDOGPCELLID2			
Description	Wdog PrimeCell ID2 Register		
Address Region	wdt	**Type:**	RO
Offset	0x0000 0FF8		
Physical address View0	0x4004 3FF8		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	PCellID2	Peripheral ID (this register stores a value from a hardware viewpoint.)	RO	0x05

7.17. WDT_WDOGPCELLID3

WDT_WDOGPCELLID3			
Description	Wdog PrimeCell ID3 Register		
Address Region	wdt	**Type:**	RO
Offset	0x0000 0FFC		
Physical address View0	0x4004 3FFC		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:8	Reserved	-	-	-
7:0	PCellID3	Peripheral ID (this register stores a value from a hardware viewpoint.)	RO	0xB1

8. Revision History

Table 8.1 Revision History

Revision	Date	Description
0.1	2014-03-14	Newly released
0.2	2014-10-07	Modified copyright notation.
0.3	2014-11-17	Added the constraint about the clock frequency setting change.
1.0	2015-01-22	Official version
1.1	2015-02-18	Section 5**:** Revised Interrupt interval in Table 5.1 and Table 5.2 Interrupt generation interval setting
1.2	2015-11-24	Added Section 6.3
1.3	2018-02-05	Changed header, footer and the last page. Changed corporate name and descriptions. Modified Arm logo and descriptions.

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