Application Processor Lite *ApP Lite*™

TZ1000 Series

Reference Manual

MCU Advanced Timer/Counter

Revision 1.3

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TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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Preface

This document provides the specification for the MCU Advanced Timer/Counter designed for the TZ1000 Series.

Intended Audience

This document is intended for the following users.

Driver software developers.

System designers

Conventions in this Document

- The following notational conventions apply to numbers:
  Hexadecimal number: 0xABC
  Decimal number: 123 or 0d123 - Only when it should be explicitly indicated that the number is decimal.
  Binary number: 0b111 - It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- Low active signals are indicated with a name suffixed with "_N".
- A signal is asserted when it goes to its active level while it is deasserted when it goes to its inactive level.
- A set of multiple signals may be referred to as [m:n].
  Example: S[3:0] indicates four signals, S3, S2, S1 and S0, collectively.
- In the text, register names are enclosed in brackets *[ ]*.
  Example:*[ABCD]*
- A set of multiple registers, fields or bits of the same type may be described collectively using "n".
  Example: *[XYZ1], [XYZ2], and [XYZ3] to [XYZn]*
- A range of register bits are referred to as [m:n].
  Example: [3:0] indicates a range from bit 3 to bit 0.
- Values set in registers are indicated using either a hexadecimal or binary number.
- Example: *[ABCD]*.EFG = 0x01 (hexadecimal), *[XYZn]*.VW = 1 (binary)
- Words and bytes are defined as follows:
  Byte: 8 bits
  Halfword: 16 bits
  Word: 32 bits
  Doubleword: 64 bits
- Register bit attributes are defined as follows:
  R: Read-only
  W: Write-only
  W1C: Clear by write of 1 - A write of "1" clears the corresponding bit to 0.
  W1S: Set by write of 1 - A write of "1" sets the corresponding bit to 1.
  R/W: Read/Write
  R/W0C: Read/Clear by write of 0
  R/W1C: Read/Clear by write of 1
  R/W1S: Read/Set by write of 1
  RS/WC: Set by read/Clear by write (set after a read and cleared after a data write)
- Registers only support word access unless otherwise specified.
- Any registers defined as Reserved in the text must not be rewritten. Also, any values read from such registers should not be used.
- Any bits for which default values are defined as "—" would return undefined values if read.
- When a data is written to a register containing both writable and read-only (R) bit fields, its default values should be written to read-only (R) bit fields. For any bit fields with default values defined as "—," refer to the definitions of the relevant register.
- Default values should be written to any reserved bit fields in a write-only register. For any bit fields with default values defined as "—," refer to the definitions of the relevant register.

1. Overview

This module is a multi-purpose 16-bit timer.

The feature is as follows.

- 4 timer channels. (Each channel has identical specification.)
- Compliant to the Arm® AMBA® (2.0) interface. The APB slave.
- 16-bit down counter.
- Changeable between 16-bit and 8-bit.
- Operating clock, TIMCLK, synchronized with the APB clock, PCLK.
- Each channel can be controlled independently by each timer enable.
- 3 operation modes.
  - One shot timer mode
  - Constant period timer mode
  - Free run timer mode
- Prescaler to divide the TIMCLK frequency (the period: ×1, ×2, ×4, ×8, ×32, ×128, ×512, and ×1024).
- An interrupt per channel and an interrupt of ORed output of ch0, ch1, cha2, and ch3.
- Each interrupt is controlled by each channel interrupt enable bit.
- Setting value (Load Value) can be changed while the timer is operating by a background register.
- Input capture function per channel: ×1.
- Output comparison function per channel: ×1.
- Interrupt generation at an input capture.
- Interrupt generation at an output comparison.
- Selection of CLK synchronization of an input capture per channel (set by a register).
- Fetch timing setting of an input capture.
  - (a pulse, a rising edge, a falling edge, and both edges)
- Event counter (the count is controlled by the Enable bit or the external enable signal).
- Selection of a delay time of the count start in the event counter.
- A pulse width measurement and a frequency measurement using the input capture function.
- Safe change of a comparison value by a background comparison register during the timer operation.
- TFF (Toggle Flip-Flop) control.
- PWM (Pulse Width Modulation) output using an output comparison function.
- Selection function that the period of the PWM wave is determined by the output comparison or the terminal count of the timer.
- The interval time of a base counter interrupt is counted (to measure a longer period than the timer's maximum count).
- Synchronization with other timers. (Synchronization signal generation)
- Timer control signal selection by an external pin assignment register.
- The timer interrupt output is controlled by a test register.
- The capture/comparison interrupts are controlled by a test register.
- DMA request and clear control.
- CLK synchronization selection of the DMA clear signal (set by a register).
- Selection function that the DMA request is generated at the output comparison or at the terminal count of the timer.

2. Block Diagram

The internal blocks of this module is shown in the following figures.

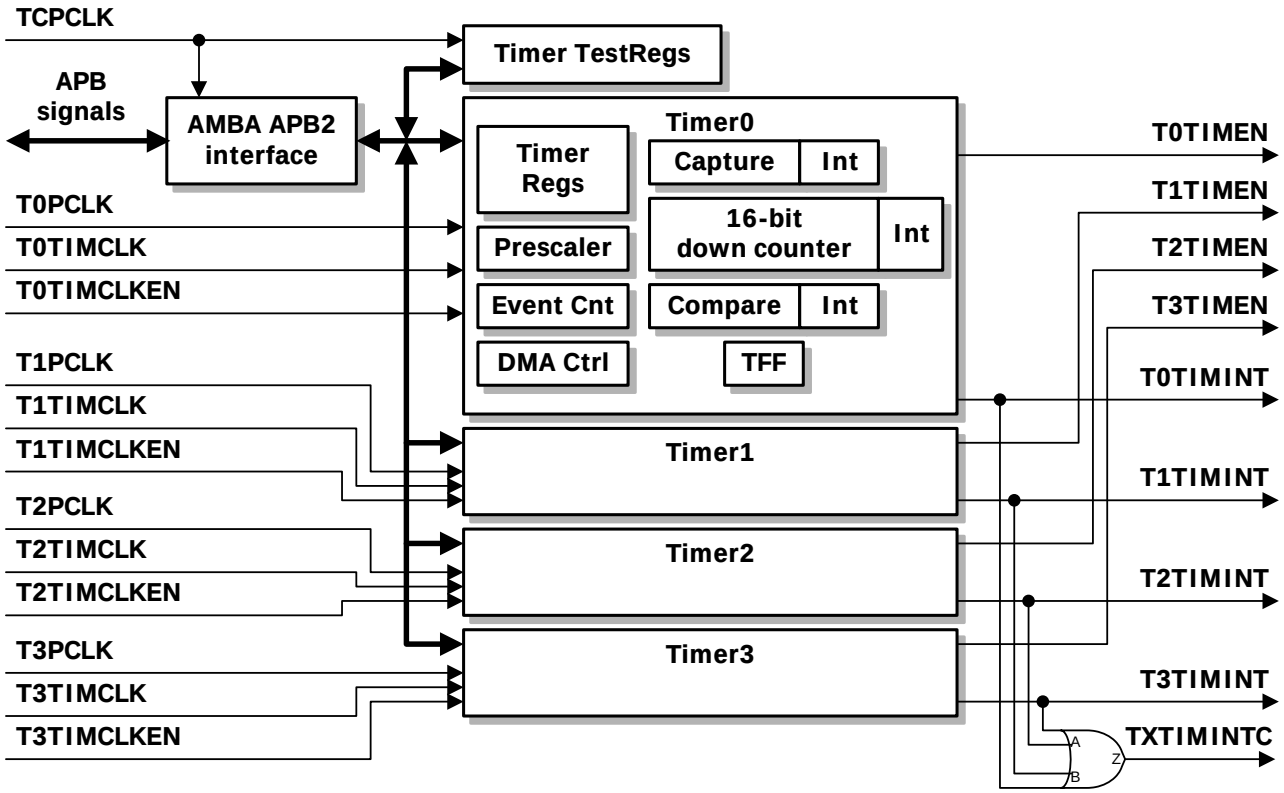

Figure 2.1 ADVTMR internal block diagram

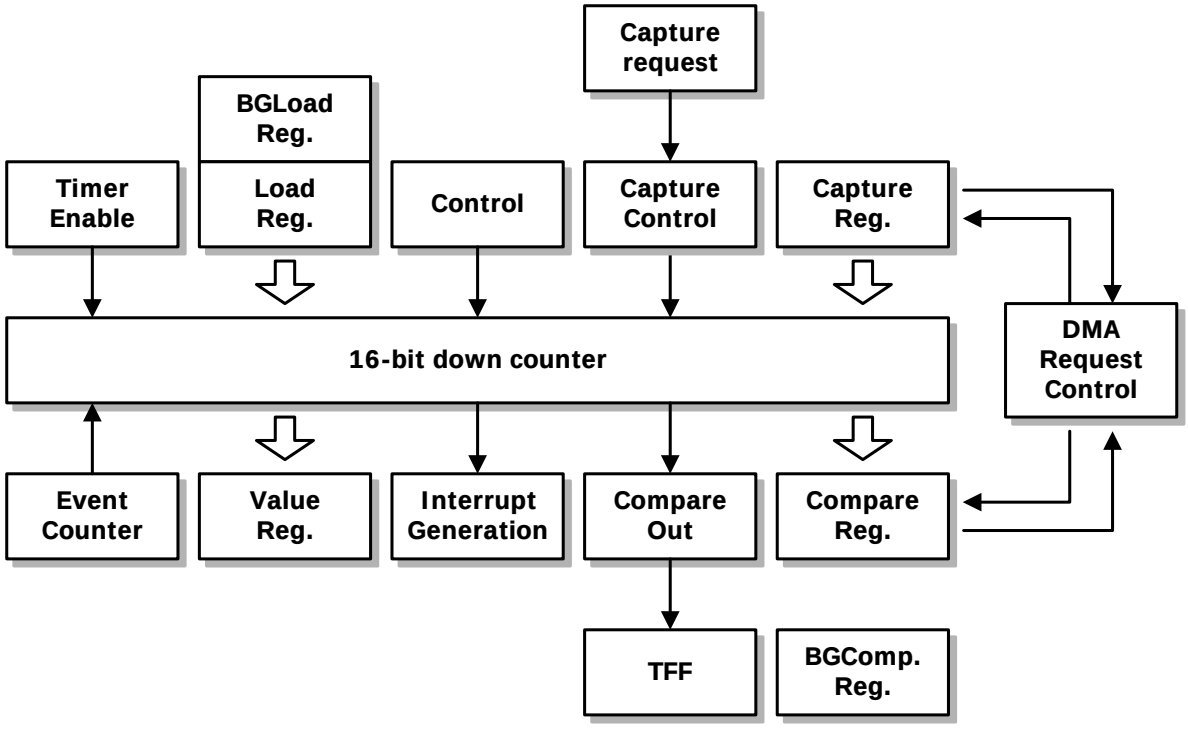

Figure 2.2 1 channel block diagram of ADVTMR

The outlines of the internal blocks of the ADVTMR are as follows.

- **AMBA® APB2 interface**
  - This interface is the APB slave interface accessed by the CPU. It is used to access the registers in 4 KB address space.
- **Test Regs**
  - The registers for the tests of the timer. These registers control the interrupt output, the capture input, the event counter input, the comparison output, and both the input and output of the SDMAC.
- **16-bit down counter**
  - The 16-bit counter which consists of the timer.
- **Timer Regs**
  - The registers for the timer.
- **Prescaler**
  - The prescaler which generates the clock to the 16-bit counter.
- **Event Cnt**
  - Controls the event count.
- **Capture**
  - Controls the input capture.
- **Compare**
  - Control the output comparison.
- **TFF (Toggle Flip Flop)**
  - Controls the output pin. It generates a variety of output.
- **Int**
  - Controls the interrupt signals.
- **DMA request control**
  - Controls the DMA request signals.

3. Input and Output Signals

3.1. Function Signals and ADVTMR signals

The function signals and the ADVTMR signals are shown in the following table. The function signals are described in Section 5.

Table 3.1 Signal comparison (1)

function signal name	ADVTMR signal name	Description
PCLK	TCPCLK	Common bus clock
	T0PCLK	ch0 bus clock
	T1PCLK	ch1 bus clock
	T2PCLK	ch2 bus clock
	T3PCLK	ch3 bus clock
TnTIMCLK	T0TIMCLK	ch0 counter clock
	T1TIMCLK	ch1 counter clock
	T2TIMCLK	ch2 counter clock
	T3TIMCLK	ch3 counter clock
TnTIMCLKEN	T0TIMCLKEN	ch0 clock enable
	T1TIMCLKEN	ch1 clock enable
	T2TIMCLKEN	ch2 clock enable
	T3TIMCLKEN	ch3 clock enable
PRESETn	TCPRESETn	Common bus reset
	T0PRESETn	ch0 bus reset
	T1PRESETn	ch1 bus reset
	T2PRESETn	ch2 bus reset
	T3PRESETn	ch3 bus reset
	T0TIMRESETn	ch0 counter reset
	T1TIMRESETn	ch1 counter reset
	T2TIMRESETn	ch2 counter reset
	T3TIMRESETn	ch3 counter reset
OTSYNC	OTSYNC	clock enable select
TnCAPSEL	T0CAPSEL	T0CAPREQ input select
	T1CAPSEL	T1CAPREQ input select
	T2CAPSEL	T2CAPREQ input select
	T3CAPSEL	T3CAPREQ input select
TnEVSRCSEL	T0EVSRCSEL	T0EVCNTSRC input select
	T1EVSRCSEL	T1EVCNTSRC input select
	T2EVSRCSEL	T2EVCNTSRC input select
	T3EVSRCSEL	T3EVCNTSRC input select
TnEVENSEL	T0EVENSEL	T0EVCNTEN input select
	T1EVENSEL	T1EVCNTEN input select
	T2EVENSEL	T2EVCNTEN input select
	T3EVENSEL	T3EVCNTEN input select

Table 3.2 Signal comparison (2)

function signal name	ADVTMR signal name	Description
PADDR	PADDR	APB signals
PENABLE	PENABLE	
PSEL	PSEL	
PWDATA	PWDATA	
PWRITE	PWRITE	
PRDATA	PRDATA	
TnTIMINT	T0TIMINT	ch0 base counter interrupt
	T1TIMINT	ch1 base counter interrupt
	T2TIMINT	ch2 base counter interrupt
	T3TIMINT	ch3 base counter interrupt
	TXTIMINTC	base counter interrupt (combined)
TnCAPINT	T0CAPINT	ch0 capture interrupt
	T1CAPINT	ch1 capture interrupt
	T2CAPINT	ch2 capture interrupt
	T3CAPINT	ch3 capture interrupt
	TXCAPINTC	capture interrupt (combined)
TnCMPINT	T0CMPINT	ch0 compare interrupt
	T1CMPINT	ch1 compare interrupt
	T2CMPINT	ch2 compare interrupt
	T3CMPINT	ch3 compare interrupt
	TXCMPINTC	compare interrupt (combined)
TnCAPREQ	T0CAPREQ	ch0 capture input
	T1CAPREQ	ch1 capture input
	T2CAPREQ	ch2 capture input
	T3CAPREQ	ch3 capture input
TnEVCNTSRC	T0EVCNTSRC	ch0 event counter source clock input
	T1EVCNTSRC	ch1 event counter source clock input
	T2EVCNTSRC	ch2 event counter source clock input
	T3EVCNTSRC	ch3 event counter source clock input
TnEVCNTEN	T0EVCNTEN	ch0 event counter enable input
	T1EVCNTEN	ch1 event counter enable input
	T2EVCNTEN	ch2 event counter enable input
	T3EVCNTEN	ch3 event counter enable input
TnIOSEL	T0IOSEL	ch0 IO direction select
	T1IOSEL	ch1 IO direction select
	T2IOSEL	ch2 IO direction select
	T3IOSEL	ch3 IO direction select
TnTFFOUT	T0TFFOUT	ch0 compare/PWM output
	T1TFFOUT	ch1 compare/PWM output
	T2TFFOUT	ch2 compare/PWM output
	T3TFFOUT	ch3 compare/PWM output

Table 3.3 Signal comparison (3)

function signal name	ADVTMR signal name	Description
EVM_CAPTURE	evm_advtimer_capture[0]	evm capture signal[0]
	evm_advtimer_capture[1]	evm capture signal[1]
	evm_advtimer_capture[2]	evm capture signal[2]
	evm_advtimer_capture[3]	evm capture signal[3]
TnCAPDMAREQ	T0CAPDMAREQ	ch0 capture DMA request
	T1CAPDMAREQ	ch1 capture DMA request
	T2CAPDMAREQ	ch2 capture DMA request
	T3CAPDMAREQ	ch3 capture DMA request
TnCAPDMACLR	T0CAPDMACLR	ch0 capture DMA clear
	T1CAPDMACLR	ch1 capture DMA clear
	T2CAPDMACLR	ch2 capture DMA clear
	T3CAPDMACLR	ch3 capture DMA clear
TnCAPDMATC	T0CAPDMATC	ch0 capture DMA transfer complete
	T1CAPDMATC	ch1 capture DMA transfer complete
	T2CAPDMATC	ch2 capture DMA transfer complete
	T3CAPDMATC	ch3 capture DMA transfer complete
TnCMPDMAREQ	T0CMPDMAREQ	ch0 compare DMA request
	T1CMPDMAREQ	ch1 compare DMA request
	T2CMPDMAREQ	ch2 compare DMA request
	T3CMPDMAREQ	ch3 compare DMA request
TnCMPDMACLR	T0CMPDMACLR	ch0 compare DMA clear
	T1CMPDMACLR	ch1 compare DMA clear
	T2CMPDMACLR	ch2 compare DMA clear
	T3CMPDMACLR	ch3 compare DMA clear
TnCMPDMATC	T0CMPDMATC	ch0 compare DMA transfer complete
	T1CMPDMATC	ch1 compare DMA transfer complete
	T2CMPDMATC	ch2 compare DMA transfer complete
	T3CMPDMATC	ch3 compare DMA transfer complete

3.2. Input/Output signals and ADVTMR signals

The list of the output pins of the TZ1000 is shown in the following table. The input signals are widely selected. For detail, refer to Section 5.8.

Table 3.4 Input/Output pins and ADVTMR signals

PIN name	Direction	Pin share	ADVTMR signal
MCU_GPIO_8	output	FMOD2	T0TFFOUT
MCU_GPIO_9	output	FMOD2	T1TFFOUT
MCU_GPIO_10	output	FMOD2	T2TFFOUT
MCU_GPIO_11	output	FMOD2	T3TFFOUT
MCU_SPIM0_CS_N	output	FMOD3	T0TFFOUT
MCU_SPIM0_CLK	output	FMOD3	T1TFFOUT
MCU_SPIM0_MOSI	output	FMOD3	T2TFFOUT
MCU_GPIO_27	output	FMOD3	T3TFFOUT
MCU_UA0_RXD	input	FMOD2	(Note)
MCU_UA0_TXD	input	FMOD2	(Note)
MCU_I2C0_DATA	input	FMOD2	(Note)
MCU_I2C0_CLK	input	FMOD2	(Note)
MCU_GPIO_12	input	FMOD3	(Note)
MCU_GPIO_13	input	FMOD3	(Note)

Note: By the connections described in Section 5.8, the input signal is decided.

4. Register map

Table 4.1 Register map

Register Name	Type	Width	Reset Value	Address Offset
ADVTMR_T0LOAD	RW	32	0x0000 0000	0x0000 0000
ADVTMR_T0VALUE	RO	32	0x0000 FFFF	0x0000 0004
ADVTMR_T0CONTROL	RW	32	0x0000 0008	0x0000 0008
ADVTMR_T0INTCLR	RW	32	-	0x0000 000C
ADVTMR_T0RIS	RO	32	0x0000 0000	0x0000 0010
ADVTMR_T0MIS	RO	32	0x0000 0000	0x0000 0014
ADVTMR_T0BGLOAD	RW	32	0x0000 0000	0x0000 0018
ADVTMR_T0INTCNT	RW	32	0x0000 0000	0x0000 001C
ADVTMR_T0CAPTURE	RO	32	0x0000 0000	0x0000 0020
ADVTMR_T0CAPINTCLR	RW	32	-	0x0000 0040
ADVTMR_T0CAPRIS	RO	32	0x0000 0000	0x0000 0060
ADVTMR_T0CAPMIS	RO	32	0x0000 0000	0x0000 0064
ADVTMR_T0CAPINTEN	RW	32	0x0000 0000	0x0000 0068
ADVTMR_T0CAPEN	RW	32	0x0000 0000	0x0000 006C
ADVTMR_T0CAPRELOAD	RW	32	0x0000 0000	0x0000 0074
ADVTMR_T0CAPCTRL	RW	32	0x0000 0000	0x0000 0078
ADVTMR_T0CAPSYNC	RW	32	0x0000 0000	0x0000 007C
ADVTMR_T0BGCOMPARE	RW	32	0x0000 0000	0x0000 0080
ADVTMR_T0COMPARE	RW	32	0x0000 0000	0x0000 00A0
ADVTMR_T0CMPINTCLR	RW	32	-	0x0000 00C0
ADVTMR_T0CMPRIS	RO	32	0x0000 0000	0x0000 00E0
ADVTMR_T0CMPMIS	RO	32	0x0000 0000	0x0000 00E4
ADVTMR_T0CMPINTEN	RW	32	0x0000 0000	0x0000 00E8
ADVTMR_T0CMPEN	RW	32	0x0000 0000	0x0000 00EC
ADVTMR_T1LOAD	RW	32	0x0000 0000	0x0000 0100
ADVTMR_T1VALUE	RO	32	0x0000 FFFF	0x0000 0104
ADVTMR_T1CONTROL	RW	32	0x0000 0008	0x0000 0108
ADVTMR_T1INTCLR	RW	32	-	0x0000 010C
ADVTMR_T1RIS	RO	32	0x0000 0000	0x0000 0110
ADVTMR_T1MIS	RO	32	0x0000 0000	0x0000 0114
ADVTMR_T1BGLOAD	RW	32	0x0000 0000	0x0000 0118
ADVTMR_T1INTCNT	RW	32	0x0000 0000	0x0000 011C
ADVTMR_T1CAPTURE	RO	32	0x0000 0000	0x0000 0120
ADVTMR_T1CAPINTCLR	RW	32	-	0x0000 0140
ADVTMR_T1CAPRIS	RO	32	0x0000 0000	0x0000 0160
ADVTMR_T1CAPMIS	RO	32	0x0000 0000	0x0000 0164
ADVTMR_T1CAPINTEN	RW	32	0x0000 0000	0x0000 0168
ADVTMR_T1CAPEN	RW	32	0x0000 0000	0x0000 016C
ADVTMR_T1CAPRELOAD	RW	32	0x0000 0000	0x0000 0174
ADVTMR_T1CAPCTRL	RW	32	0x0000 0000	0x0000 0178
ADVTMR_T1CAPSYNC	RW	32	0x0000 0000	0x0000 017C
ADVTMR_T1BGCOMPARE	RW	32	0x0000 0000	0x0000 0180
ADVTMR_T1COMPARE	RW	32	0x0000 0000	0x0000 01A0
ADVTMR_T1CMPINTCLR	RW	32	-	0x0000 01C0
ADVTMR_T1CMPRIS	RO	32	0x0000 0000	0x0000 01E0
ADVTMR_T1CMPMIS	RO	32	0x0000 0000	0x0000 01E4
ADVTMR_T1CMPINTEN	RW	32	0x0000 0000	0x0000 01E8
ADVTMR_T1CMPEN	RW	32	0x0000 0000	0x0000 01EC
ADVTMR_T2LOAD	RW	32	0x0000 0000	0x0000 0200
ADVTMR_T2VALUE	RO	32	0x0000 FFFF	0x0000 0204
ADVTMR_T2CONTROL	RW	32	0x0000 0008	0x0000 0208
ADVTMR_T2INTCLR	RW	32	-	0x0000 020C
ADVTMR_T2RIS	RO	32	0x0000 0000	0x0000 0210

Register Name	Type	Width	Reset Value	Address Offset
ADVTMR_T2MIS	RO	32	0x0000 0000	0x0000 0214
ADVTMR_T2BGLOAD	RW	32	0x0000 0000	0x0000 0218
ADVTMR_T2INTCNT	RW	32	0x0000 0000	0x0000 021C
ADVTMR_T2CAPTURE	RO	32	0x0000 0000	0x0000 0220
ADVTMR_T2CAPINTCLR	RW	32	-	0x0000 0240
ADVTMR_T2CAPRIS	RO	32	0x0000 0000	0x0000 0260
ADVTMR_T2CAPMIS	RO	32	0x0000 0000	0x0000 0264
ADVTMR_T2CAPINTEN	RW	32	0x0000 0000	0x0000 0268
ADVTMR_T2CAPEN	RW	32	0x0000 0000	0x0000 026C
ADVTMR_T2CAPRELOAD	RW	32	0x0000 0000	0x0000 0274
ADVTMR_T2CAPCTRL	RW	32	0x0000 0000	0x0000 0278
ADVTMR_T2CAPSYNC	RW	32	0x0000 0000	0x0000 027C
ADVTMR_T2BGCOMPARE	RW	32	0x0000 0000	0x0000 0280
ADVTMR_T2COMPARE	RW	32	0x0000 0000	0x0000 02A0
ADVTMR_T2CMPINTCLR	RW	32	-	0x0000 02C0
ADVTMR_T2CMPRIS	RO	32	0x0000 0000	0x0000 02E0
ADVTMR_T2CMPMIS	RO	32	0x0000 0000	0x0000 02E4
ADVTMR_T2CMPINTEN	RW	32	0x0000 0000	0x0000 02E8
ADVTMR_T2CMPEN	RW	32	0x0000 0000	0x0000 02EC
ADVTMR_T3LOAD	RW	32	0x0000 0000	0x0000 0300
ADVTMR_T3VALUE	RO	32	0x0000 FFFF	0x0000 0304
ADVTMR_T3CONTROL	RW	32	0x0000 0008	0x0000 0308
ADVTMR_T3INTCLR	RW	32	-	0x0000 030C
ADVTMR_T3RIS	RO	32	0x0000 0000	0x0000 0310
ADVTMR_T3MIS	RO	32	0x0000 0000	0x0000 0314
ADVTMR_T3BGLOAD	RW	32	0x0000 0000	0x0000 0318
ADVTMR_T3INTCNT	RW	32	0x0000 0000	0x0000 031C
ADVTMR_T3CAPTURE	RO	32	0x0000 0000	0x0000 0320
ADVTMR_T3CAPINTCLR	RW	32	-	0x0000 0340
ADVTMR_T3CAPRIS	RO	32	0x0000 0000	0x0000 0360
ADVTMR_T3CAPMIS	RO	32	0x0000 0000	0x0000 0364
ADVTMR_T3CAPINTEN	RW	32	0x0000 0000	0x0000 0368
ADVTMR_T3CAPEN	RW	32	0x0000 0000	0x0000 036C
ADVTMR_T3CAPRELOAD	RW	32	0x0000 0000	0x0000 0374
ADVTMR_T3CAPCTRL	RW	32	0x0000 0000	0x0000 0378
ADVTMR_T3CAPSYNC	RW	32	0x0000 0000	0x0000 037C
ADVTMR_T3BGCOMPARE	RW	32	0x0000 0000	0x0000 0380
ADVTMR_T3COMPARE	RW	32	0x0000 0000	0x0000 03A0
ADVTMR_T3CMPINTCLR	RW	32	-	0x0000 03C0
ADVTMR_T3CMPRIS	RO	32	0x0000 0000	0x0000 03E0
ADVTMR_T3CMPMIS	RO	32	0x0000 0000	0x0000 03E4
ADVTMR_T3CMPINTEN	RW	32	0x0000 0000	0x0000 03E8
ADVTMR_T3CMPEN	RW	32	0x0000 0000	0x0000 03EC
ADVTMR_T0TFFEN	RW	32	0x0000 0000	0x0000 0400
ADVTMR_T0TFFSTAT	RO	32	0x0000 0000	0x0000 0404
ADVTMR_T0TFFZERO	RW	32	0x0000 0000	0x0000 0408
ADVTMR_T0TFFINV	RW	32	0x0000 0000	0x0000 040C
ADVTMR_T0TFFCTRL	RW	32	0x0000 0003	0x0000 0410
ADVTMR_T0TFFINIT	RW	32	0x0000 0000	0x0000 0414
ADVTMR_T0EVCONTROL	RW	32	0x0000 0008	0x0000 0420
ADVTMR_T0EVSEL	RW	32	0x0000 0000	0x0000 0430
ADVTMR_T0IOSEL	RW	32	0x0000 0000	0x0000 0434
ADVTMR_T0CAPSEL	RW	32	0x0000 0000	0x0000 0438
ADVTMR_T0CAPDMAEN	RW	32	0x0000 0000	0x0000 0480
ADVTMR_T0CAPDMASTAT	RO	32	0x0000 0000	0x0000 0490
ADVTMR_T0CMPDMASTAT	RW	32	0x0000 0000	0x0000 0498
ADVTMR_T0TCDMASEL	RW	32	0x0000 0000	0x0000 049C
ADVTMR_T0CMPDMAEN	RW	32	0x0000 0000	0x0000 04A0

Register Name	Type	Width	Reset Value	Address Offset
ADVTMR_T0CAPDMASYNC	RW	32	0x0000 0000	0x0000 04B8
ADVTMR_T0CMPDMASYNC	RW	32	0x0000 0000	0x0000 04BC
ADVTMR_T0CAPDMACLR	RW	32	0x0000 0000	0x0000 04F0
ADVTMR_T0CMPDMACLR	RW	32	0x0000 0000	0x0000 04F4
ADVTMR_T1TFFEN	RW	32	0x0000 0000	0x0000 0500
ADVTMR_T1TFFSTAT	RO	32	0x0000 0000	0x0000 0504
ADVTMR_T1TFFZERO	RW	32	0x0000 0000	0x0000 0508
ADVTMR_T1TFFINV	RW	32	0x0000 0000	0x0000 050C
ADVTMR_T1TFFCTRL	RW	32	0x0000 0003	0x0000 0510
ADVTMR_T1TFFINIT	RW	32	0x0000 0000	0x0000 0514
ADVTMR_T1EVCONTROL	RW	32	0x0000 0008	0x0000 0520
ADVTMR_T1EVSEL	RW	32	0x0000 0000	0x0000 0530
ADVTMR_T1IOSEL	RW	32	0x0000 0000	0x0000 0534
ADVTMR_T1CAPSEL	RW	32	0x0000 0000	0x0000 0538
ADVTMR_T1CAPDMAEN	RW	32	0x0000 0000	0x0000 0580
ADVTMR_T1CAPDMASTAT	RO	32	0x0000 0000	0x0000 0590
ADVTMR_T1CMPDMASTAT	RO	32	0x0000 0000	0x0000 0598
ADVTMR_T1TCDMASEL	RW	32	0x0000 0000	0x0000 059C
ADVTMR_T1CMPDMAEN	RW	32	0x0000 0000	0x0000 05A0
ADVTMR_T1CAPDMASYNC	RW	32	0x0000 0000	0x0000 05B8
ADVTMR_T1CMPDMASYNC	RW	32	0x0000 0000	0x0000 05BC
ADVTMR_T1CAPDMACLR	RW	32	0x0000 0000	0x0000 05F0
ADVTMR_T1CMPDMACLR	RW	32	0x0000 0000	0x0000 05F4
ADVTMR_T2TFFEN	RW	32	0x0000 0000	0x0000 0600
ADVTMR_T2TFFSTAT	RO	32	0x0000 0000	0x0000 0604
ADVTMR_T2TFFZERO	RW	32	0x0000 0000	0x0000 0608
ADVTMR_T2TFFINV	RW	32	0x0000 0000	0x0000 060C
ADVTMR_T2TFFCTRL	RW	32	0x0000 0003	0x0000 0610
ADVTMR_T2TFFINIT	RW	32	0x0000 0000	0x0000 0614
ADVTMR_T2EVCONTROL	RW	32	0x0000 0008	0x0000 0620
ADVTMR_T2EVSEL	RW	32	0x0000 0000	0x0000 0630
ADVTMR_T2IOSEL	RW	32	0x0000 0000	0x0000 0634
ADVTMR_T2CAPSEL	RW	32	0x0000 0000	0x0000 0638
ADVTMR_T2CAPDMAEN	RW	32	0x0000 0000	0x0000 0680
ADVTMR_T2CAPDMASTAT	RO	32	0x0000 0000	0x0000 0690
ADVTMR_T2CMPDMASTAT	RO	32	0x0000 0000	0x0000 0698
ADVTMR_T2TCDMASEL	RW	32	0x0000 0000	0x0000 069C
ADVTMR_T2CMPDMAEN	RW	32	0x0000 0000	0x0000 06A0
ADVTMR_T2CAPDMASYNC	RW	32	0x0000 0000	0x0000 06B8
ADVTMR_T2CMPDMASYNC	RW	32	0x0000 0000	0x0000 06BC
ADVTMR_T2CAPDMACLR	RW	32	0x0000 0000	0x0000 06F0
ADVTMR_T2CMPDMACLR	RW	32	0x0000 0000	0x0000 06F4
ADVTMR_T3TFFEN	RW	32	0x0000 0000	0x0000 0700
ADVTMR_T3TFFSTAT	RO	32	0x0000 0000	0x0000 0704
ADVTMR_T3TFFZERO	RW	32	0x0000 0000	0x0000 0708
ADVTMR_T3TFFINV	RW	32	0x0000 0000	0x0000 070C
ADVTMR_T3TFFCTRL	RW	32	0x0000 0003	0x0000 0710
ADVTMR_T3TFFINIT	RW	32	0x0000 0000	0x0000 0714
ADVTMR_T3EVCONTROL	RW	32	0x0000 0008	0x0000 0720
ADVTMR_T3EVSEL	RW	32	0x0000 0000	0x0000 0730
ADVTMR_T3IOSEL	RW	32	0x0000 0000	0x0000 0734
ADVTMR_T3CAPSEL	RW	32	0x0000 0000	0x0000 0738
ADVTMR_T3CAPDMAEN	RW	32	0x0000 0000	0x0000 0780
ADVTMR_T3CAPDMASTAT	RO	32	0x0000 0000	0x0000 0790
ADVTMR_T3CMPDMASTAT	RO	32	0x0000 0000	0x0000 0798
ADVTMR_T3TCDMASEL	RW	32	0x0000 0000	0x0000 079C
ADVTMR_T3CMPDMAEN	RW	32	0x0000 0000	0x0000 07A0
ADVTMR_T3CAPDMASYNC	RW	32	0x0000 0000	0x0000 07B8

Register Name	Type	Width	Reset Value	Address Offset
ADVTMR_T3CMPDMASYNC	RW	32	0x0000 0000	0x0000 07BC
ADVTMR_T3CAPDMACLR	RW	32	0x0000 0000	0x0000 07F0
ADVTMR_T3CMPDMACLR	RW	32	0x0000 0000	0x0000 07F4
ADVTMR_TITCR	RW	32	0x0000 0000	0x0000 0F00
ADVTMR_TITOP	RW	32	0x0000 0000	0x0000 0F04
ADVTMR_TOTSYNC	RW	32	0x0000 00FF	0x0000 0F10
ADVTMR_T0ITCMPCAPINT	RW	32	0x0000 0000	0x0000 0F20
ADVTMR_T1ITCMPCAPINT	RW	32	0x0000 0000	0x0000 0F24
ADVTMR_T2ITCMPCAPINT	RW	32	0x0000 0000	0x0000 0F28
ADVTMR_T3ITCMPCAPINT	RW	32	0x0000 0000	0x0000 0F2C
ADVTMR_T0ITEVCNT	RO	32	0x0000 0000	0x0000 0F40
ADVTMR_T1ITEVCNT	RO	32	0x0000 0000	0x0000 0F44
ADVTMR_T2ITEVCNT	RO	32	0x0000 0000	0x0000 0F48
ADVTMR_T3ITEVCNT	RO	32	0x0000 0000	0x0000 0F4C
ADVTMR_T0ITCAPDRQCAPRQ	RW	32	0x0000 0000	0x0000 0F60
ADVTMR_T0ITCAPDTCDCLR	RO	32	0x0000 0000	0x0000 0F64
ADVTMR_T1ITCAPDRQCAPRQ	RW	32	0x0000 0000	0x0000 0F68
ADVTMR_T1ITCAPDTCDCLR	RO	32	0x0000 0000	0x0000 0F6C
ADVTMR_T2ITCAPDRQCAPRQ	RW	32	0x0000 0000	0x0000 0F70
ADVTMR_T2ITCAPDTCDCLR	RO	32	0x0000 0000	0x0000 0F74
ADVTMR_T3ITCAPDRQCAPRQ	RW	32	0x0000 0000	0x0000 0F78
ADVTMR_T3ITCAPDTCDCLR	RO	32	0x0000 0000	0x0000 0F7C
ADVTMR_T0ITCMPDRQTFF	RW	32	0x0000 0000	0x0000 0FA0
ADVTMR_T0ITCMPDTCDCLR	RO	32	0x0000 0000	0x0000 0FA4
ADVTMR_T1ITCMPDRQTFF	RW	32	0x0000 0000	0x0000 0FA8
ADVTMR_T1ITCMPDTCDCLR	RO	32	0x0000 0000	0x0000 0FAC
ADVTMR_T2ITCMPDRQTFF	RW	32	0x0000 0000	0x0000 0FB0
ADVTMR_T2ITCMPDTCDCLR	RO	32	0x0000 0000	0x0000 0FB4
ADVTMR_T3ITCMPDRQTFF	RW	32	0x0000 0000	0x0000 0FB8
ADVTMR_T3ITCMPDTCDCLR	RO	32	0x0000 0000	0x0000 0FBC
ADVTMR_TPERIPHID0	RO	32	0x0000 0004	0x0000 0FE0
ADVTMR_TPERIPHID1	RO	32	0x0000 0048	0x0000 0FE4
ADVTMR_TPERIPHID2	RO	32	0x0000 0025	0x0000 0FE8
ADVTMR_TPERIPHID3	RO	32	0x0000 0216	0x0000 0FEC
ADVTMR_TPCELLID0	RO	32	0x0000 000D	0x0000 0FF0
ADVTMR_TPCELLID1	RO	32	0x0000 00F0	0x0000 0FF4
ADVTMR_TPCELLID2	RO	32	0x0000 0005	0x0000 0FF8
ADVTMR_TPCELLID3	RO	32	0x0000 00B1	0x0000 0FFC

5. Functional Description

The function signal names are used in this chapter. For the function signal names, refer to Table 3.1 and Table 3.2.

5.1. Clock Operation

5.1.1. Clock and Clock Enable Operation

The relation among the PCLK, the TIMCLK, and the TIMCLKEN is shown in the following figure (Each channel has its own clock names, but the following uses the function names to represent the channel signal names.) The count shows the count number of the base counter.

The TIMCLK and the TIMCLKEN are synchronized with the PCLK. The corresponding clocks of each channel are also synchronized as the same manner.

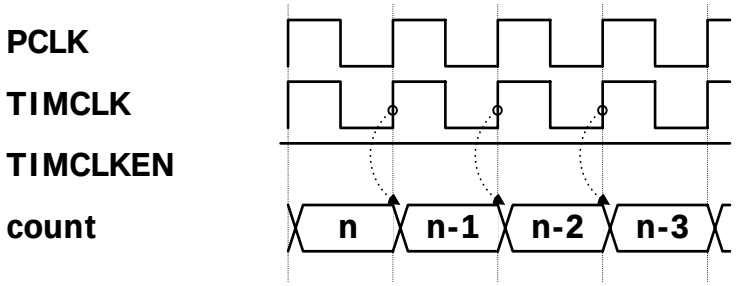

Figure 5.1 Case that PCLK and TIMCLK have the same frequency (TIMCLKEN = 1)

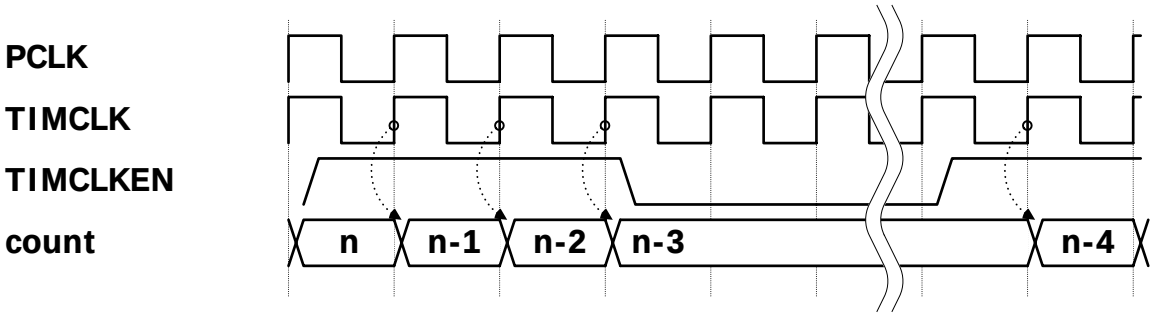

Figure 5.2 Case that PCLK and TIMCLK have the same frequency (TIMCLKEN is changing)

5.1.2. Prescaler Operation

The block diagram of the Prescaler in the ADVTMR is shown in the following figure. The prescaler enable output is used as the clock enable to the counter.

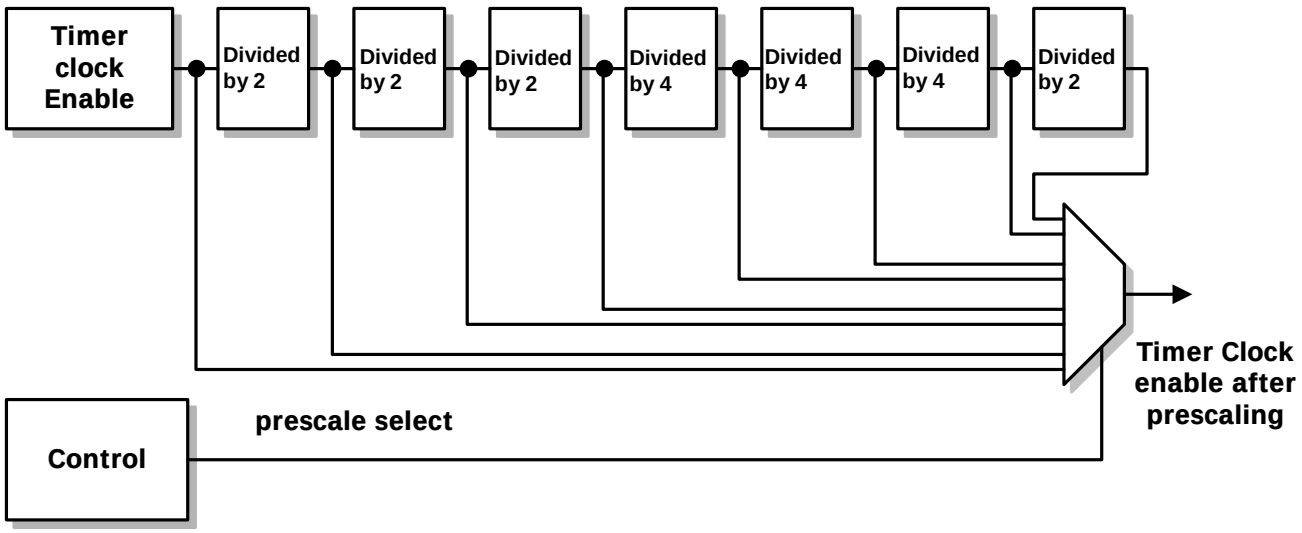

Figure 5.3 Block diagram of Prescaler

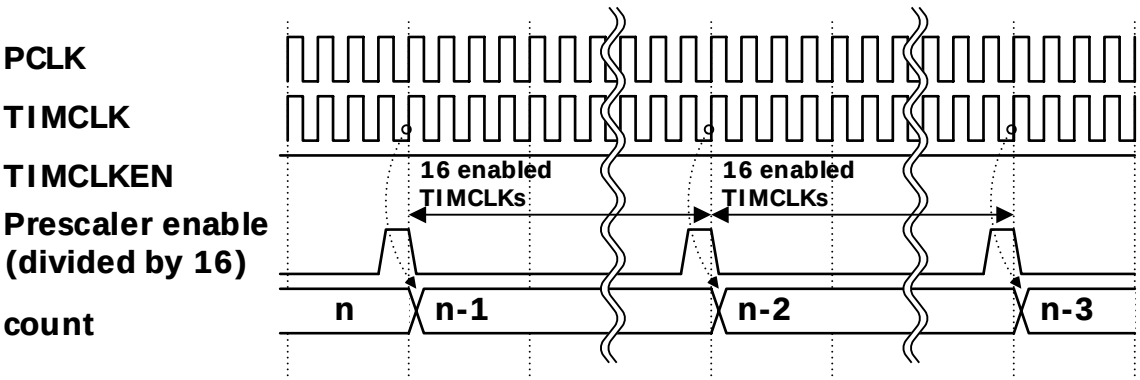

Figure 5.4 Example of Base counter operation with dividing frequency by Prescaler

The interval time of the interrupt generation is calculated using the following formula.

Interrupt generation interval = (**TnLOAD** +1) × (**TIMCLK** period: during **TIMCLKEN** = 1)
× (Prescaler setting value)
(**n** is a channel number: 0, 1, 2, or 3)

Table 5.1 Interrupt generation interval (TIMCLK = 1 MHz, Prescaler: ×1, ×128, and ×1024)

Interrupt interval	TnLOAD register (Prescaler ×1)		TnLOAD register (Prescaler ×128)		TnLOAD register (Prescaler ×1024)	
	Hex	Decimal	Hex	Decimal	Hex	Decimal
100 µs	0x0063	99	—	—	—	—
500 µs	0x01F3	499	0x0003	3	—	—
1 ms	0x03E7	999	0x0007	7	—	—
5 ms	0x1387	4999	0x0027	39	0x0004	4
10 ms	0x270F	9999	0x004D	77	0x0009	9
50 ms	0xC34F	49999	0x0185	389	0x0031	49
100 ms	—	—	0x030B	779	0x0063	99
500 ms	—	—	0x0F3B	3899	0x01F3	499
1 s	—	—	0x1E77	7799	0x03E7	999
60 s	—	—	—	—	0xEA5F	59999

Note: "—" shows that the setting is not available.

The following is the maximum value of the interrupt generation interval for each setting.

Prescaler ×1: 65.536 ms
Prescaler ×128: 8.3886 s
Prescaler ×1024: 67.1089 s

Table 5.2 Interrupt generation interval (TIMCLK = 12 MHz, Prescaler: ×1, ×128, and ×1024)

Interrupt interval	TxLOAD register (Prescaler ×1)		TxLOAD register (Prescaler ×128)		TxLOAD register (Prescaler ×1024)	
	Hex	Decimal	Hex	Decimal	Hex	Decimal
50 μs	0x0257	599	—	—	—	—
100 μs	0x04AF	1199	0x0009	9	—	—
500 μs	0x176F	5999	0x002E	46	0x0005	5
1 ms	0x2EDF	11999	0x005D	93	0x000B	11
5 ms	0xEA5F	59999	0x01D3	467	0x0031	49
10 ms	—	—	0x03A8	936	0x0075	117
50 ms	—	—	0x124E	4686	0x0257	585
100 ms	—	—	0x249E	9374	0x0493	1171
500 ms	—	—	0xB71A	46874	0x16E3	5859
1 s	—	—	—	—	0x2DC5	11717

Note: "—" shows that the setting is not available.

The following is the maximum value of the interrupt generation interval for each setting.

Prescaler ×1: 5.4613 ms
Prescaler ×128: 699.05 ms
Prescaler ×1024: 5.5924 s

5.2. Base Counter Operation

5.2.1. One-shot Mode

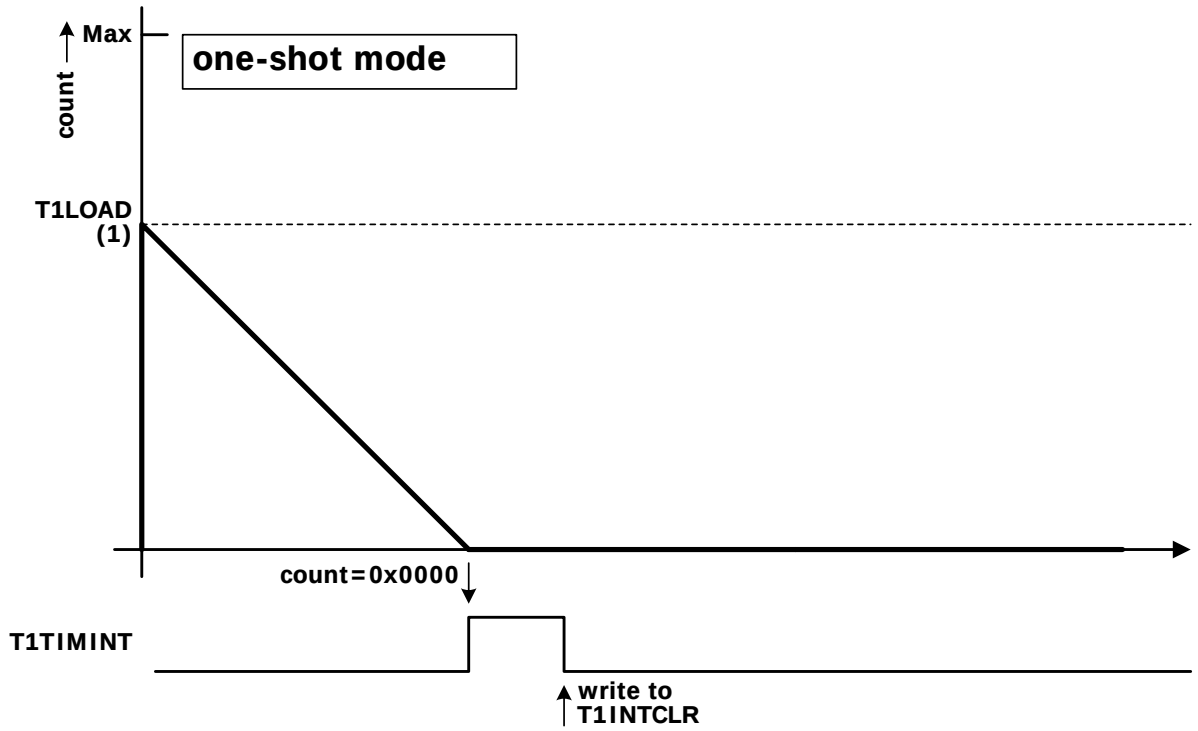

Figure 5.5 One-shot mode operation

In the one-shot mode, after the register is set and the timer enable is asserted, the counter starts to operate. The counter decrements from the value which is set to the load register *[ADVTMR_T1LOAD].* When the count value in the counter becomes 0000 (the terminal count), the counter stops and the timer interrupt request is generated. After the interrupt process finishes in the CPU, the interrupt request is cleared by writing to the interrupt clear register *[ADVTMR_T1INTCLR].*

In the following example, the register setting and the operation represent the channel 1 in the ADVTMR. (The other examples later are also the same.)

Example

Register	Event	Reg. Value	Comments
T1CONTROL	—	**0x0038**	16-bit width, Normal, Timer disable, Interrupt disable, Periodic, One-shot, x1
T1LOAD	—	**0xAAAA**	Set value: T1LOAD(1)
T1CONTROL	—	**0x0F8**	Timer enable, Interrupt enable
—	**count = 0x0000**	—	terminal count occurs
—	**T1TIMINT = 0b1**	—	Timer interrupt (terminal count) occurs
T1INTCLR	**—**	**any value**	Clear Timer Interrupt
—	**T1TIMINT = 0b0**	—	—

Note: When the one-shot operation finishes, the counter stops. The clock is, however, still supplied. Even though the dynamic clock gating is set (refer to Section 5.12), the clock does not stop. It is necessary to stop the clock that the timer should be disabled or the PMU register should be set to the clock stop.

5.2.2. Constant Period Timer Wrapping Mode

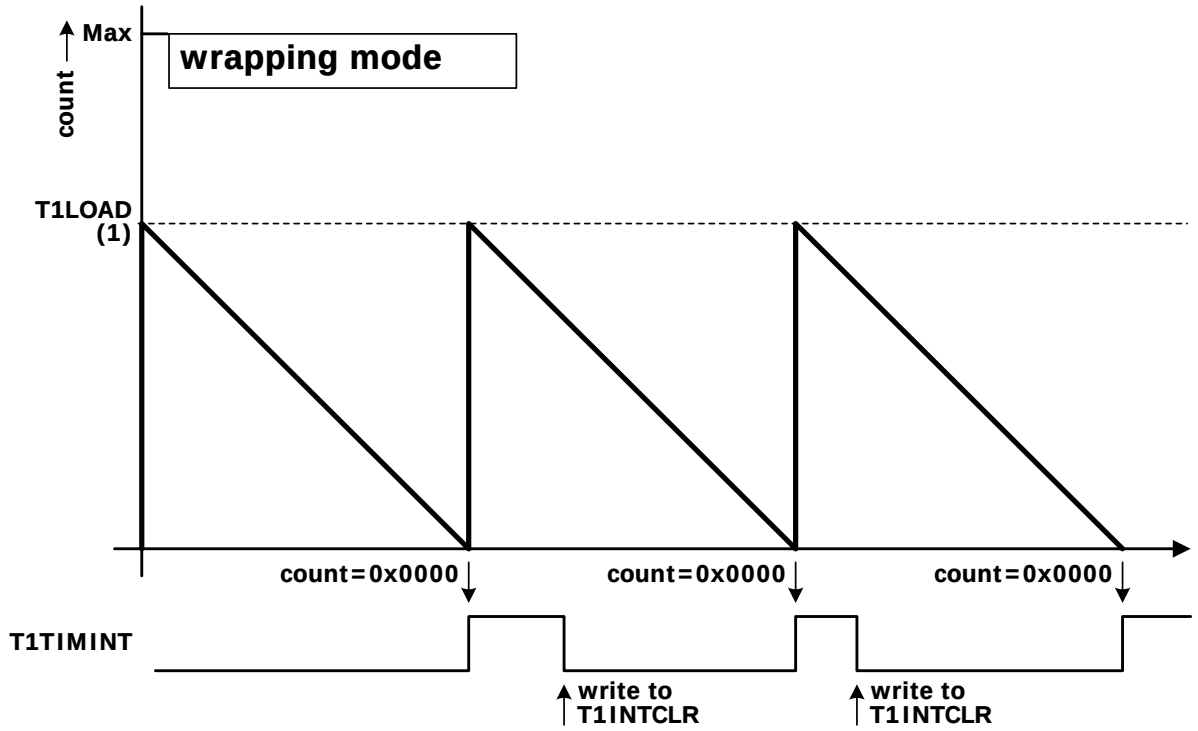

Figure 5.6 Constant period wrapping mode

In the constant period timer wrapping mode, after the register is set and the timer enable is asserted, the counter starts frequent counts. The counter decrements from the value which is set to the load register *[ADVTMR_T1LOAD].* When the count value in the counter becomes 0000 (the terminal count), the counter stops and the timer interrupt request is generated. After the interrupt process finishes in the CPU, the interrupt request is cleared by writing to the interrupt clear register *[ADVTMR_T1INTCLR].*

The counter is set again to the value in the load register *[ADVTMR_T1LOAD]* and repeats the operation until the timer disable is asserted.

Example

Register	Event	Reg. Value	Comments
T1CONTROL	—	**0x0028**	16-bit width, Normal, Timer disable, Interrupt disable, Periodic, Wrapping, x1
T1LOAD	—	**0xAAAA**	Set value: T1LOAD(1)
T1CONTROL	—	**0x0E8**	Timer enable, Interrupt enable
—	**count = 0x0000**	—	terminal count occurs
—	**T1TIMINT = 0b1**	—	Timer interrupt (terminal count) occurs
T1INTCLR	—	**any value**	Clear Timer Interrupt
—	**T1TIMINT = 0b0**	—	—
:	:	—	—
—	**count = 0x0000**	—	terminal count occurs
—	**T1TIMINT = 0b1**	—	Timer interrupt occurs
T1INTCLR	—	**any value**	Clear Timer Interrupt
—	**T1TIMINT = 0b0**	—	—
:	:	—	—
—	**count = 0x0000**	—	terminal count occurs
—	**T1TIMINT = 0b1**	—	Timer interrupt occurs

5.2.3. Free-run Timer Wrapping Mode

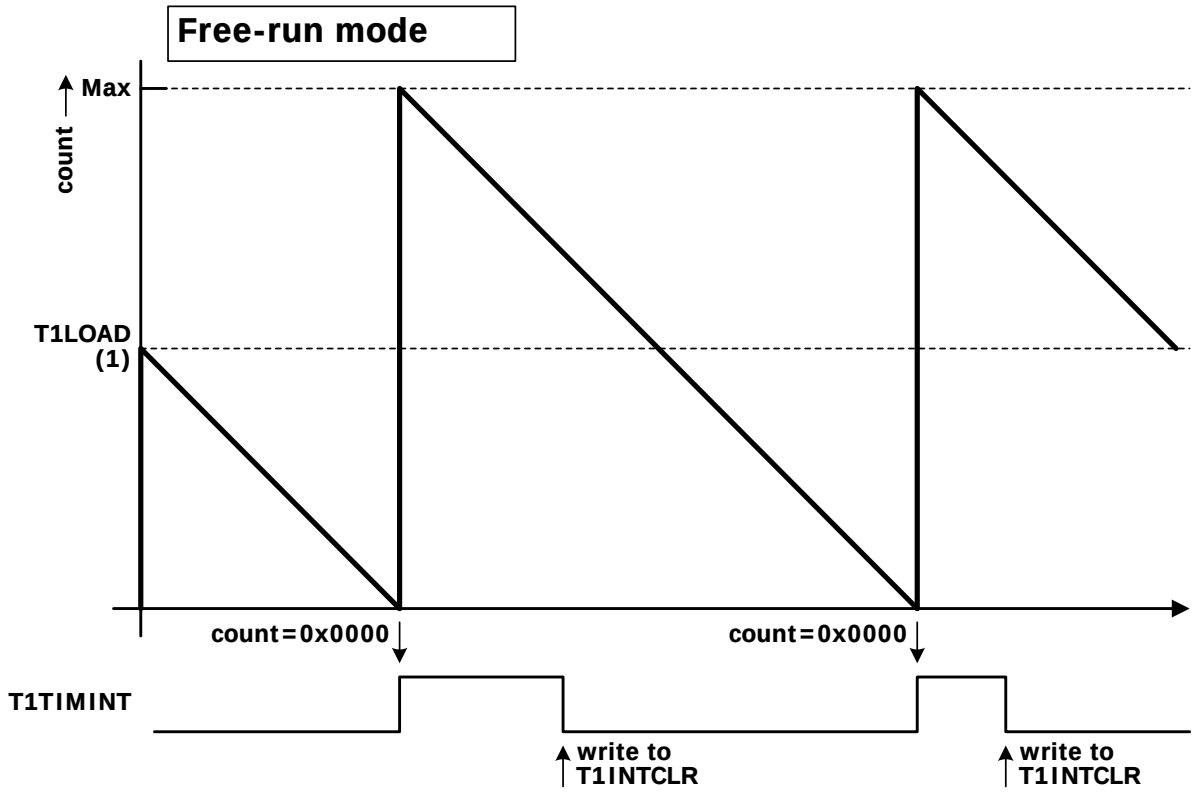

Figure 5.7 Free-run timer wrapping mode

In the free-run timer wrapping mode, after the register is set and the timer enable is asserted, the counter starts frequent counts. The counter decrements from the value which is set to the load register *[ADVTMR_T1LOAD]*. When the count value in the counter becomes 0000 (the terminal count), the counter stops and the timer interrupt request is generated. After the interrupt process finishes in the CPU, the interrupt request is cleared by writing to the interrupt clear register *[ADVTMR_T1INTCLR]*.

The counter is set to the maximum count value regardless of the value in the load register *[ADVTMR_T1LOAD]* and repeats the operation until the timer disable is asserted.

Example

Register	Event	Reg. Value	Comments
T1CONTROL	—	**0x0008**	16-bit width, Normal, Timer disable, Interrupt disable, Free-run, Wrapping, x1
T1LOAD	—	**0xAAAA**	Set value: T1LOAD(1)
T1CONTROL	—	**0x0C8**	Timer enable, Interrupt enable
—	**count = 0x0000**	—	terminal count occurs
—	**T1TIMINT = 0b1**	—	Timer interrupt (terminal count) occurs
T1INTCLR	—	**any value**	Clear Timer Interrupt
—	**T1TIMINT = 0b0**	—	—
:	**:**	—	—
—	**count = 0x0000**	—	terminal count occurs
—	**T1TIMINT = 0b1**	—	Timer interrupt (terminal count) occurs
T1INTCLR	—	**any value**	Clear Timer Interrupt
—	**T1TIMINT = 0b0**	—	—

5.2.4. Load Register Change Operation

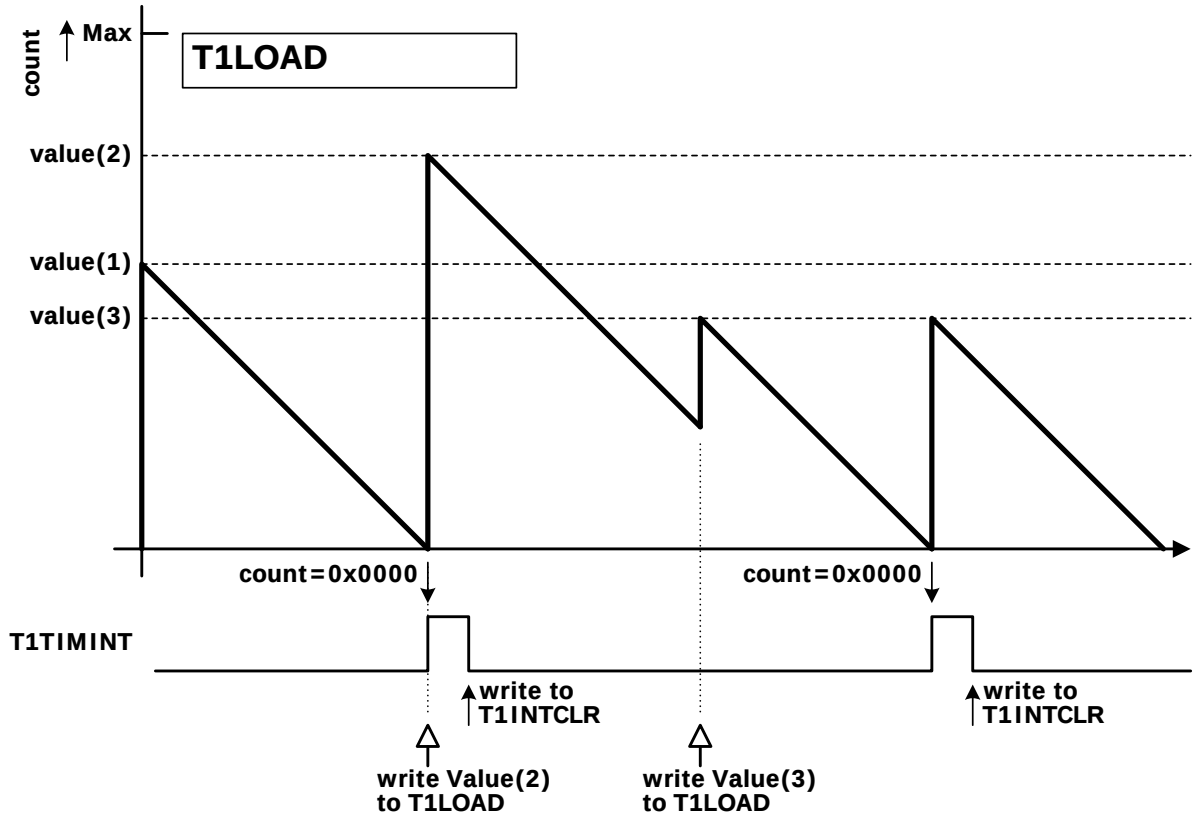

Figure 5.8 Load Register Change Operation

In the constant period timer wrapping mode, when the counter is operating and the load register *[ADVTMR_T1LOAD]* is changed, the count value in the counter is set to the value immediately. This means that the counter value changes before the terminal count. To prevent this discontinuity, the setting of the load register *[ADVTMR_T1LOAD]* should be done in the following state.

- When the counter stops. Or,
- When the count value is 0000 (the terminal count).

Example

Register	Event	Reg. Value	Comments
T1CONTROL	—	**0x0028**	16-bit width, Normal, Timer disable, Interrupt disable, Periodic, Wrapping, x1
T1LOAD	—	**0xAAAA**	Set value: T1LOAD(1)
T1CONTROL	—	**0x00E8**	Timer enable, Interrupt enable
—	**count = 0x0000**	—	terminal count occurs
—	**T1TIMINT = 0b1**	—	Timer interrupt (terminal count) occurs
T1LOAD	—	**0xDDDD**	Set value: T1LOAD(2)
T1INTCLR	—	**any value**	Clear Timer Interrupt
—	**T1TIMINT = 0b0**	—	—
T1LOAD	—	**0x9999**	**Set value: T1LOAD(3)**
—	**count = 0x0000**	—	terminal count occurs
—	**T1TIMINT = 0b1**	—	Timer interrupt (terminal count) occurs
T1INTCLR	—	**any value**	Clear Timer Interrupt
—	**T1TIMINT = 0b0**	—	—

5.2.5. Background Load Register Change Operation

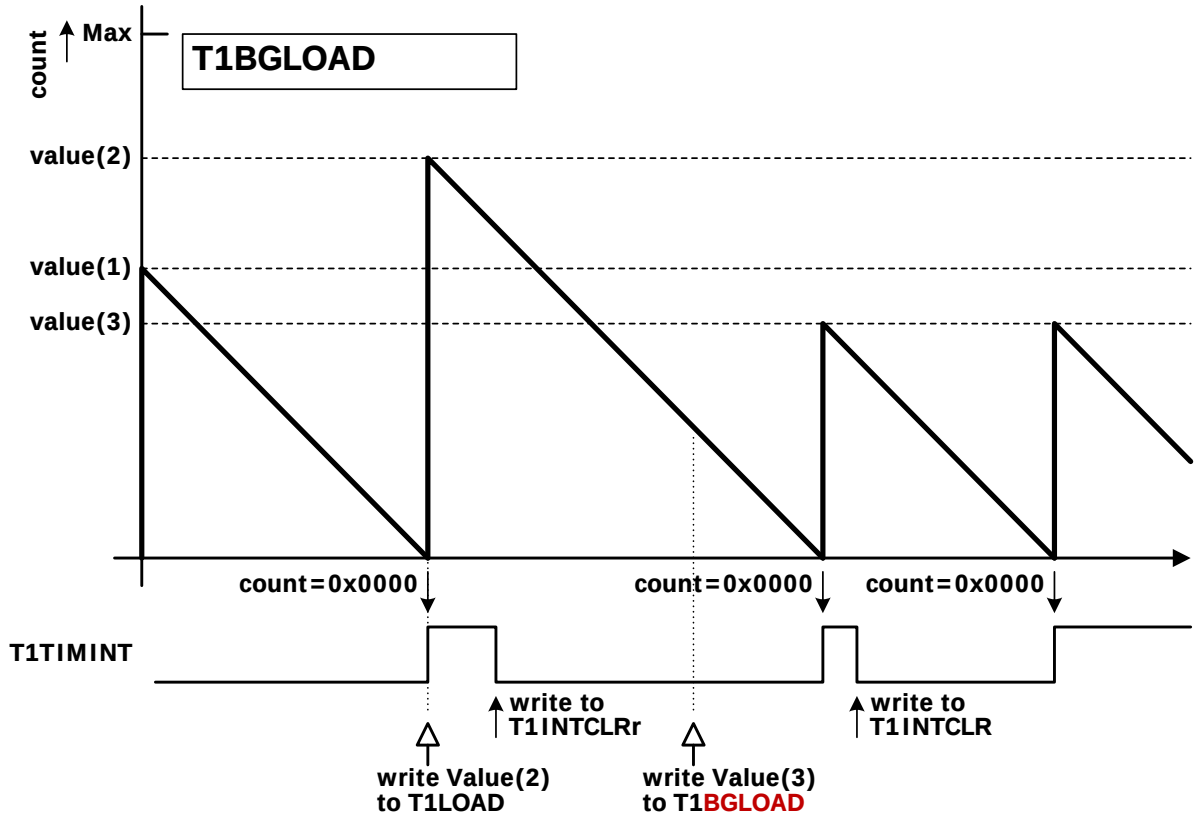

Figure 5.9 Background load register change operation

When the background load register *[ADVTMR_T1BGLOAD]* is used and the value is changed during the counter operation, the count value in the counter does not changed immediately. The *[ADVTMR_T1BGLOAD]* value is set to the counter when the count becomes 0000 (the terminal count). So the discontinuity in the count does not occur.

Example

Register	Event	Reg. Value	Comments
T1CONTROL	—	**0x0028**	16-bit width, Normal, Timer disable, Interrupt disable, Periodic, Wrapping, x1
T1LOAD	—	**0xAAAA**	Set value: T1LOAD(1)
T1CONTROL	—	**0x00E8**	Timer enable, Interrupt enable
—	**count = 0x0000**	—	terminal count occurs
—	**T1TIMINT = 0b1**	—	Timer interrupt (terminal count) occurs
T1LOAD	—	**0xDDDD**	Set value: T1LOAD(2)
T1INTCLR	—	**any value**	Clear Timer Interrupt
—	**T1TIMINT = 0b0**	—	—
T1BGLOAD	—	**0x9999**	**Set value: T1BGLOAD(3)**
—	**count = 0x0000**	—	terminal count occurs
—	**T1TIMINT = 0b1**	—	Timer interrupt (terminal count) occurs
T1INTCLR	—	**any value**	Clear Timer Interrupt
—	**T1TIMINT = 0b0**	—	—
:	:	—	—
—	**count = 0x0000**	—	terminal count occurs
—	**T1TIMINT = 0b1**	—	Timer interrupt (terminal count) occurs

5.3. Capture Operation

5.3.1. Input Capture Operation (One channel)

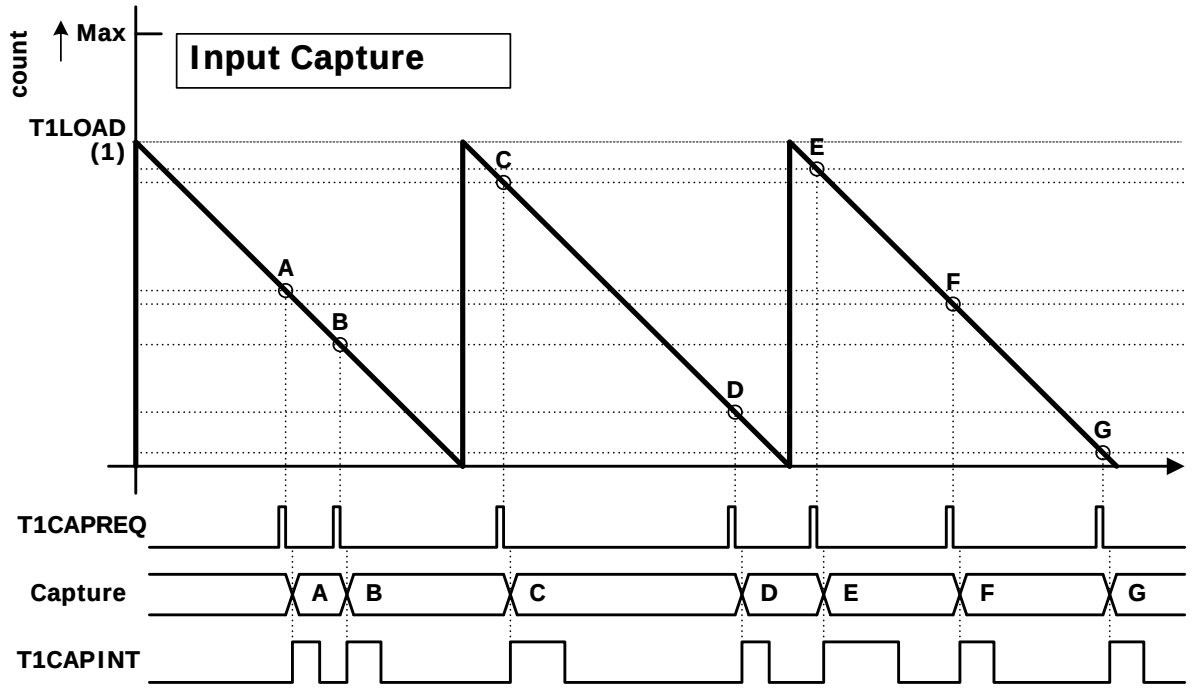

Figure 5.10 Input capture operation (One channel)

The count value is captured by the Capture register ***[ADVTMR_T1CAPTURE]*** when the **T1CAPREQ** is asserted. And the capture interrupt is generated. This interrupt can be cleared by writing the capture interrupt clear register ***[ADVTMR_T1CAPINTCLR]***. The data in the Capture register should be read by the CPU in the interrupt process. When the new capture occurs before the read of the previous capture data, the captured data is stored to a capture buffer. If the next capture occurs, the latest data is discarded. The ADVTMR error is not generated. So the interval time between the captures should be long enough.

Example

Register	Event	Reg. Value	Comments
T1CONTROL	—	**0x0028**	16-bit width, Normal, Timer disable, Interrupt disable, Periodic, Wrapping, x1
T1LOAD	—	**0xAAAA**	Set value: T1LOAD(1)
T1CAPSYNC	—	**0x0001**	Select sync. Capture
T1CAPCTRL	—	**0x0000**	Select Capture: pulse
T1CAPINTEN	—	**0x0001**	Capture interrupt enable
T1CAPEN	—	**0x0001**	Capture enable
T1CONTROL	—	**0x000A8**	Timer enable, Interrupt disable
—	**T1CAPREQ**	—	Input Capture (pulse signal)
—	**count = A**	—	—
—	**Capture = A**	—	Count value into Capture register
—	**T1CAPINT = 0b1**	—	Capture interrupt occurs
T1CAPTURE		**A**	Read Capture register
T1CAPINTCLR		**any value**	Clear Capture Interrupt
—	**T1CAPINT = 0b0**	—	—

Register	Event	Reg. Value	Comments
:	:	—	—
—	**T1CAPREQ**	—	Input Capture (pulse signal)
—	**count = B**	—	—
—	**Capture = B**	—	Count value into Capture register
—	**T1CAPINT = 0b1**	—	Capture interrupt occurs
T1CAPTURE	—	**B**	Read Capture register
T1CAPINTCLR	—	**any value**	Clear Capture Interrupt
—	**T1CAPINT = 0b0**	—	—
:	:		—
—	**T1CAPREQ**	—	Input Capture (pulse signal)
—	**count = C**	—	—
—	**Capture = C**	—	Count value into Capture register
—	**T1CAPINT = 0b1**	—	Capture interrupt occurs
T1CAPTURE	—	**C**	Read Capture register
T1CAPINTCLR	—	**any value**	Clear Capture Interrupt
—	**T1CAPINT = 0b0**	—	—
:	:		—
—	**T1CAPREQ**	—	Input Capture (pulse signal)
—	**count = D**	—	—
—	**Capture = D**	—	Count value into Capture register
—	**T1CAPINT = 0b1**	—	Capture interrupt occurs
T1CAPTURE	—	**D**	Read Capture register
T1CAPINTCLR	—	**any value**	Clear Capture Interrupt
—	**T1CAPINT = 0b0**	—	—

5.3.2. Input Capture Edge Control

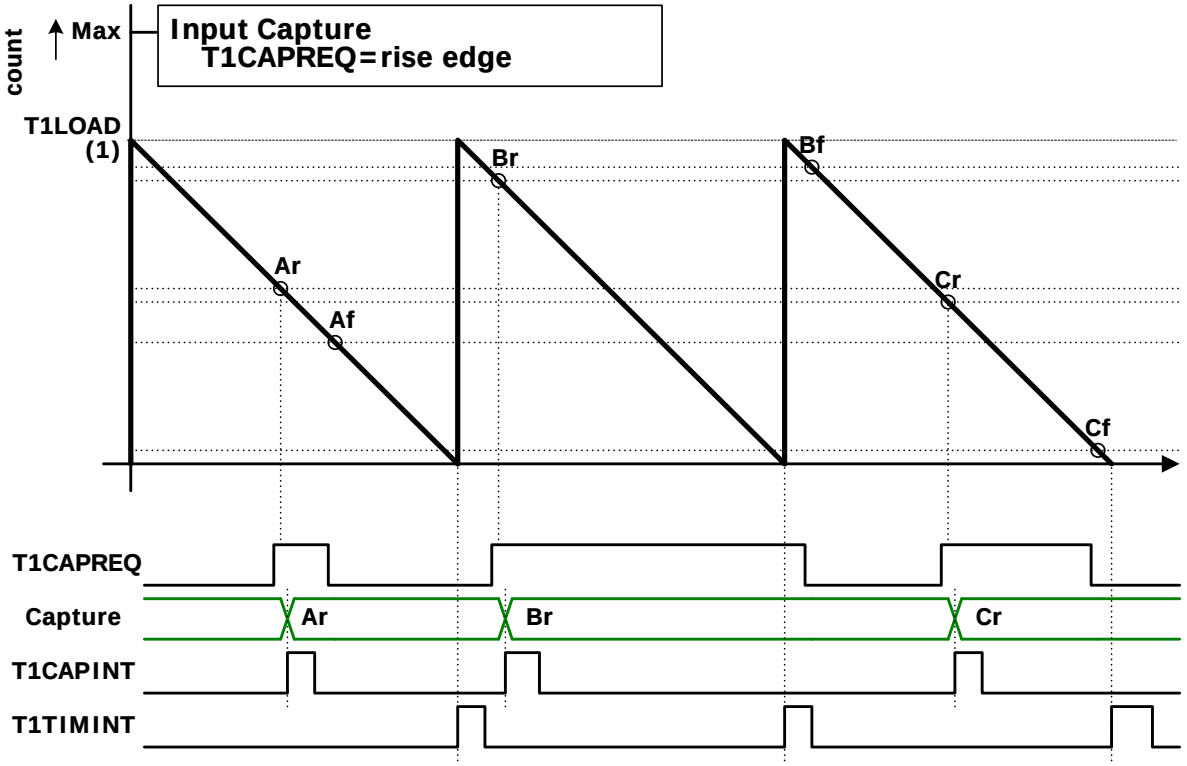

Figure 5.11 Input capture edge control

The timing of the capture is selected among the rising edge, the falling edge, and both edges of the **TICAPREQ** signal. This selection is set by the capture control register *[ADVTMR_T1CAPCTRL]*.

Figure 5.11 shows an example of the rising edge.

5.3.3. Input Capture PWM Operation (One channel)

PWM: Pulse Width Measurement

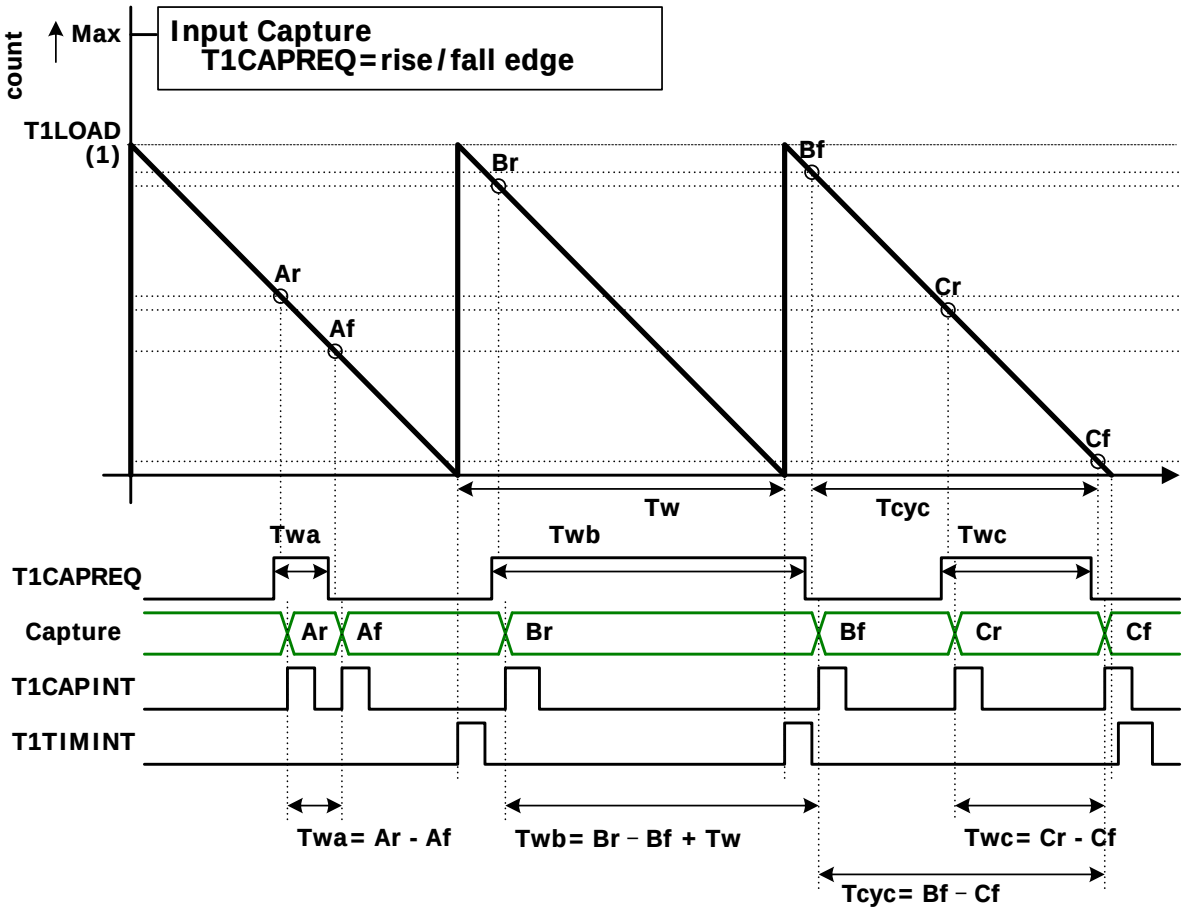

Figure 5.12 Input capture PWM operation (One channel)

The high level width of the **T1CAPREQ** can be measured by the capture operation. The capture at both edges of the **T1CAPREQ** is selected by the capture control register *[ADVTMR_T1CAPCTRL]*.

The data Ar is captured in *[ADVTMR_T1CAPTURE]* at the rising edge, and the data Af is captured in the same register *[ADVTMR_T1CAPTURE]*, and those data are read and the subtraction, Ar – AF, is done by the CPU to calculate the width. If the width is longer than the period of the counter, the counter period should be added to the calculation result (Twb in Figure 5.12).

To measure the period of a signal, the rising edge or the falling edge is used to capture the counter (Tcyc in Figure 5.12).

Example

Register	Event	Reg. Value	Comments
T1CONTROL	—	**0x0028**	16-bit width, Normal, Timer disable, Interrupt disable, Periodic, Wrapping, x1
T1LOAD	—	**0xAAAA**	Set value: T1LOAD(1)
T1CAPSYNC	—	**0x0001**	Select sync. Capture
T1CAPCTRL	—	**0x0003**	Select Capture: rise or fall edge
T1CAPINTEN	—	**0x0001**	Capture interrupt enable
T1CAPEN	—	**0x0001**	Capture enable
T1CONTROL	—	**0x00E8**	Timer enable, Interrupt enable

Register	Event	Reg. Value	Comments
:	:	—	—
—	**T1CAPREQ**	—	Input Capture (rise edge signal)
—	**count = Ar**	—	—
—	**Capture = Ar**	—	Count value into Capture register
—	**T1CAPINT = 0b1**	—	Capture interrupt occurs
T1CAPTURE	—	**Ar**	Read Capture register
T1CAPINTCLR	—	**any value**	Clear Capture Interrupt
—	**T1CAPINT = 0b0**	—	—
:	:	—	—
—	**T1CAPREQ**	—	Input Capture (fall edge signal)
—	**count = Af**	—	—
—	**Capture = Af**	—	Count value into Capture register
—	**T1CAPINT = 0b1**	—	Capture interrupt occurs
T1CAPTURE	—	**Af**	Read Capture register
T1CAPINTCLR	—	**any value**	Clear Capture Interrupt
—	**T1CAPINT = 0b0**	—	—
:	:	—	Twa = Ar - Af
—	**T1TIMINT = 0b1**	—	Timer interrupt (terminal count) occurs
:	:	—	—
—	**T1CAPREQ**	—	Input Capture (rise edge signal)
—	**count = Br**	—	—
—	**Capture = Br**	—	Count value into Capture register
—	**T1CAPINT = 0b1**	—	Capture interrupt occurs
T1CAPTURE	—	**Br**	Read Capture register
T1CAPINTCLR	—	**any value**	Clear Capture Interrupt
—	**T1CAPINT = 0b0**	—	—
:	:		—
—	**T1TIMINT = 0b1**	—	Timer interrupt (terminal count) occurs
:	:	—	—
—	**T1CAPREQ**	—	Input Capture (fall edge signal)
—	**count = Bf**	—	—
—	**Capture = Bf**	—	Count value into Capture register
—	**T1CAPINT = 0b1**	—	Capture interrupt occurs
T1CAPTURE	—	**Bf**	Read Capture register
T1CAPINTCLR	—	**any value**	Clear Capture Interrupt
—	**T1CAPINT = 0b0**	—	—

5.3.4. Input Capture Operation (Reload)

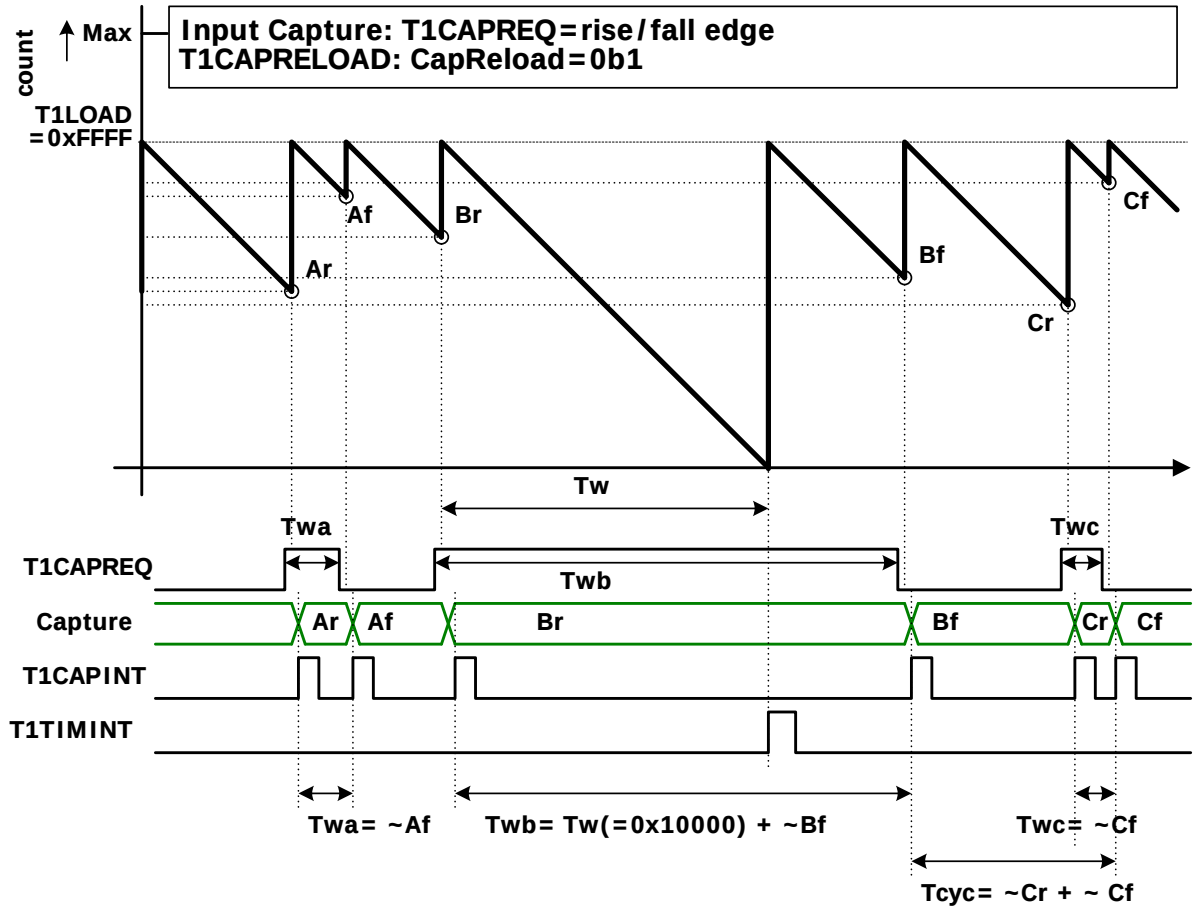

Figure 5.13 Input capture PWM operation (Reload)

When a capture occurs, the counter can re-load a count if *[ADVTMR_T1CAPRELOAD]*.CapReload is set to 1. This re-load does not generate the interrupt (TITIMIN) which is done by the terminal count. This function simplifies the calculation of the pulse measurement. If the load register *[ADVTMR_T1LOAD]* is set to 0xFFFF, each data is 1's complement of the captured value.

This function cannot be used the other functions like the comparison because the count value in the counter is forced to the value at the capture.

Example

Register	Event	Reg. Value	Comments
T1CONTROL	—	**0x0028**	16-bit width, Normal, Timer disable, Interrupt disable, Periodic, Wrapping, x1
T1LOAD	—	**0xFFFF**	Set value: T1LOAD(1)
T1CAPRELOAD	—	**0x0001**	Select Capture Reload
T1CAPSYNC	—	**0x0001**	Select sync. Capture
T1CAPCTRL	—	**0x0003**	Select Capture: rise or fall edge
T1CAPINTEN	—	**0x0001**	Capture interrupt enable
T1CAPEN	—	**0x0001**	Capture enable
T1CONTROL	—	**0x00E8**	Timer enable, Interrupt enable
—	**T1CAPREQ**	—	Input Capture (rise edge signal)
—	**count = Ar**	—	—
—	**Capture = Ar**	—	Count value into Capture register
—	**T1CAPINT = 0b1**	—	Capture interrupt occurs

Register	Event	Reg. Value	Comments
T1CAPTURE	—	**Ar**	Read Capture register
T1CAPINTCLR	—	**any value**	Clear Capture Interrupt
—	**T1CAPINT = 0b0**	—	—
:	**:**	—	—
—	**T1CAPREQ**	—	Input Capture (fall edge signal)
—	**count = Af**	—	—
—	**Capture = Af**	—	Count value into Capture register
—	**T1CAPINT = 0b1**	—	Capture interrupt occurs
T1CAPTURE	—	**Af**	Read Capture register
T1CAPINTCLR	—	**any value**	Clear Capture Interrupt
—	**T1CAPINT = 0b0**	—	—

5.4. Comparison Operation

5.4.1. Output Comparison Operation (One channel)

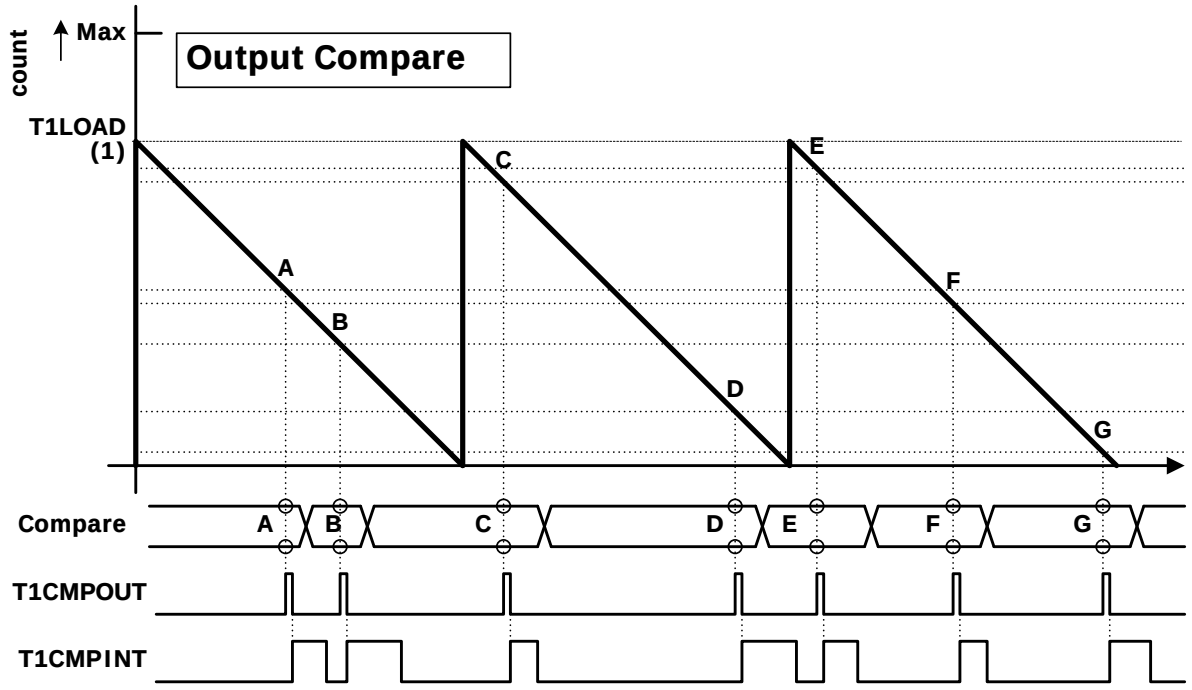

Figure 5.14 Output comparison operation (One channel)

A count data is set to the comparison register *[ADVTMR_T1COMPARE]*. When the counter operates and the count becomes the comparison value, the comparison interrupt is generated. The interrupt is cleared by writing to the comparison interrupt clear register *[ADVTMR_T1CMPINTCLR]*. Usually, the next comparison is set in the previous interrupt process.

Example

Register	Event	Reg. Value	Comments
T1CONTROL	—	**0x0028**	16-bit width, Normal, Timer disable, Interrupt disable, Periodic, Wrapping, x1
T1LOAD	—	**0xAAAA**	Set value: T1LOAD(1)
T1COMPARE	—	**A**	Set value: T1COMPARE(A)
T1CMPINTEN	—	**0x0001**	Compare interrupt enable
T1CMPEN	—	**0x0001**	Compare enable
T1CONTROL	—	**0x00A8**	Timer enable, Interrupt disable
—	**count = A**	—	—
—	**T1CMPOUT = 0b1/0**	—	Compare occurs
—	**T1CMPINT = 0b1**	—	Compare interrupt occurs
T1COMPARE	—	**B**	Set value: T1COMPARE(B)
T1CMPINTCLR	—	**any value**	Clear Compare Interrupt
—	**T1CMPINT = 0b0**	—	—
:	:	—	—
—	**count = B**	—	—
—	**T1CMPOUT = 0b1/0**	—	Compare occurs
—	**T1CMPINT = 0b1**	—	Compare interrupt occurs
T1COMPARE	—	**C**	Set value: T1COMPARE(C)
T1CMPINTCLR	—	**any value**	Clear Compare Interrupt
—	**T1CMPINT = 0b0**	—	—

Register	Event	Reg. Value	Comments
:	:	—	—
—	count = 0x0000	—	terminal count occurs
—	count = C	—	—
—	T1CMPOUT = 0b1/0	—	Compare occurs
—	T1CMPINT = 0b1	—	Compare interrupt occurs
T1COMPARE	—	D	Set value: T1COMPARE(D)
T1CMPINTCLR	—	any value	Clear Compare Interrupt
—	T1CMPINT = 0b0	—	—
:	:	—	—
—	count = D	—	—
—	T1CMPOUT = 0b1/0	—	Compare occurs
—	T1CMPINT = 0b1	—	Compare interrupt occurs
T1COMPARE	—	E	Set value: T1COMPARE(E)
T1CMPINTCLR	—	any value	Clear Compare Interrupt
—	T1CMPINT = 0b0	—	—
:	:	—	—
—	count = 0x0000	—	terminal count occurs

5.4.2. Output Comparison TFF Control (One channel)

TFF: Toggle Flip-Flop

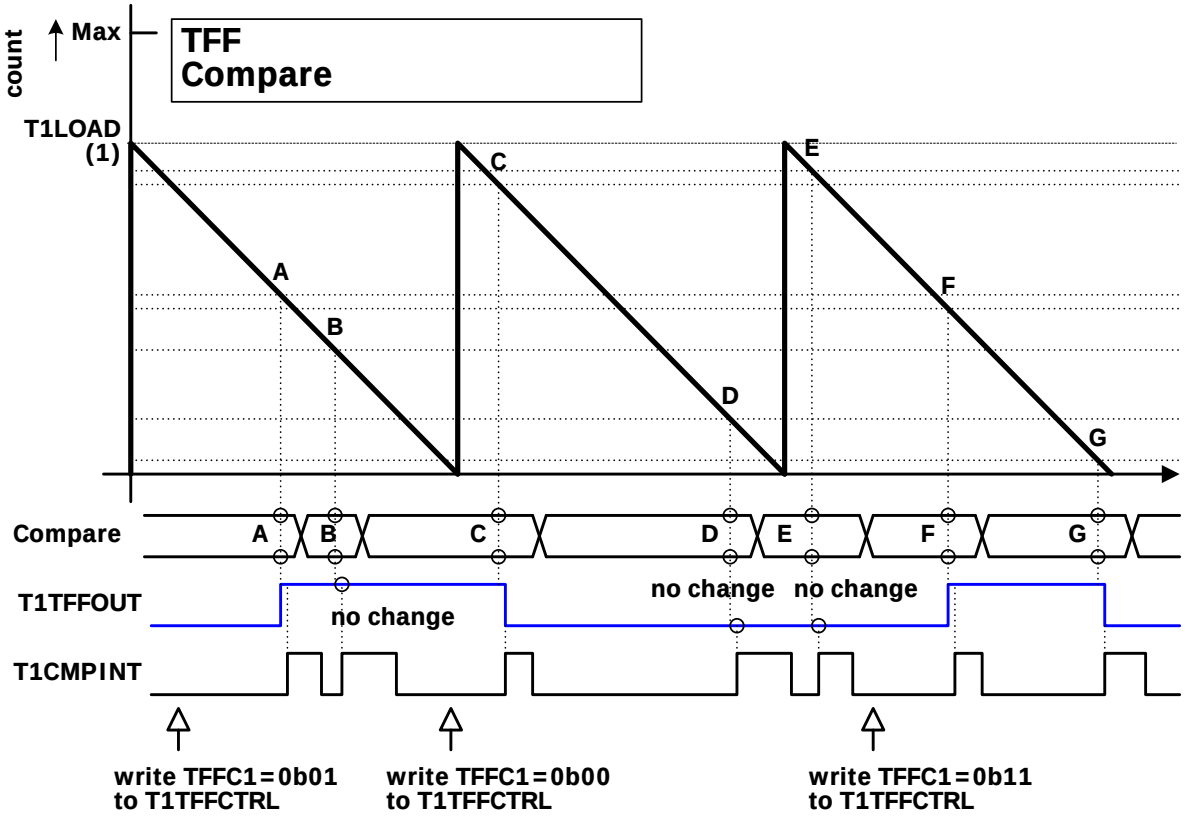

Figure 5.15 Output comparison TFF control (One channel)

The external output signals generated by the comparison operations are selected as follows. These are controlled by the TFF control register *[ADVTMR_T1TFFCTRL]*.

- Change to 0 with the pulse
- Change to 1 with the pulse
- Reverse the output value with the pulse

Example

Register	Event	Reg. Value	Comments
T1CONTROL	—	**0x0028**	16-bit width, Normal, Timer disable, Interrupt disable, Periodic, Wrapping, x1
T1LOAD	—	**0xAAAA**	Set value: T1LOAD(1)
T1COMPARE	—	**A**	Set value: T1COMPARE(A)
T1TFFCTRL	—	**0x0001**	Select TFF0: "High level"
T1TFFEN	—	**0x0001**	TFF0 enable
T1IOSEL	—	**0x0001**	TFF0 I/O enable
T1CMPINTEN	—	**0x0001**	Compare interrupt enable
T1CMPEN	—	**0x0001**	Compare enable
T1CONTROL	—	**0x00A8**	Timer enable, Interrupt disable
—	**count = A**	—	—
—	**T1TFFOUT = 0b1**	—	T1TFFOUT go to "High"
—	**T1CMPINT = 0b1**	—	Compare interrupt occurs
T1COMPARE		**B**	Set value: T1COMPARE(B)
T1CMPINTCLR		**any value**	Clear Compare Interrupt
—	**T1CMPINT = 0b0**	—	—
:	:	—	—
—	**count = B**	—	—
—	**T1TFFOUT = 0b1**	—	T1TFFOUT hold "High"
—	**T1CMPINT = 0b1**	—	Compare interrupt occurs
T1COMPARE	—	**C**	Set value: T1COMPARE(C)
T1CMPINTCLR	—	**any value**	Clear Compare Interrupt
—	**T1CMPINT = 0b0**	—	—
T1TFFCTRL		**0x0000**	Select TFF0: "Low level"
—	**count = 0x0000**	—	terminal count occurs
:	:	—	—
—	**count = C**	—	—
—	**T1TFFOUT = 0b1**	—	T1TFFOUT go to "Low"
—	**T1CMPINT = 0b1**	—	Compare interrupt occurs
T1COMPARE	—	**D**	Set value: T1COMPARE(D)
T1CMPINTCLR	—	**any value**	Clear Compare Interrupt
—	**T1CMPINT = 0b0**	—	—
T1CMPINTCLR	—	**any value**	Clear Compare Interrupt
—	**T1CMPINT = 0b0**	—	—
—	**count = D**	—	—
—	**T1TFFOUT = 0b1**	—	T1TFFOUT hold "Low"
—	**T1CMPINT = 0b1**	—	Compare interrupt occurs
T1COMPARE	—	**E**	Set value: T1COMPARE(E)
T1CMPINTCLR	—	**any value**	Clear Compare Interrupt
—	**T1CMPINT = 0b0**	—	—
:	:	—	—
—	**count = 0x0000**	—	—
—	**count = E**	—	—
—	**T1TFFOUT = 0b1**	—	T1TFFOUT hold "Low"
—	**T1CMPINT = 0b1**	—	Compare interrupt occurs
T1COMPARE	—	**F**	Set value: T1COMPARE(F)
T1CMPINTCLR	—	**any value**	Clear Compare Interrupt
—	**T1CMPINT = 0b0**	—	—

Register	Event	Reg. Value	Comments
:	:	—	—
T1TFFCTRL	—	0x0002	Select TFF0: "Toggle"
—	count = F	—	—
—	T1TFFOUT = 0b1	—	T1TFFOUT go to "High"
—	T1CMPINT = 0b1	—	Compare interrupt occurs
T1COMPARE	—	G	Set value: T1COMPARE(G)
T1CMPINTCLR	—	any value	Clear Compare Interrupt
—	T1CMPINT = 0b0	—	—
:	:	—	—
—	count = G	—	—
—	T1TFFOUT = 0b1	—	T1TFFOUT go to "Low"
—	T1CMPINT = 0b1	—	Compare interrupt occurs
T1COMPARE	—	—	Set value: T1COMPARE(-)
T1CMPINTCLR	—	any value	Clear Compare Interrupt
—	T1CMPINT = 0b0	—	—

5.4.3. Output Comparison PWM Operation (1)

PWM: Pulse Width Modulation

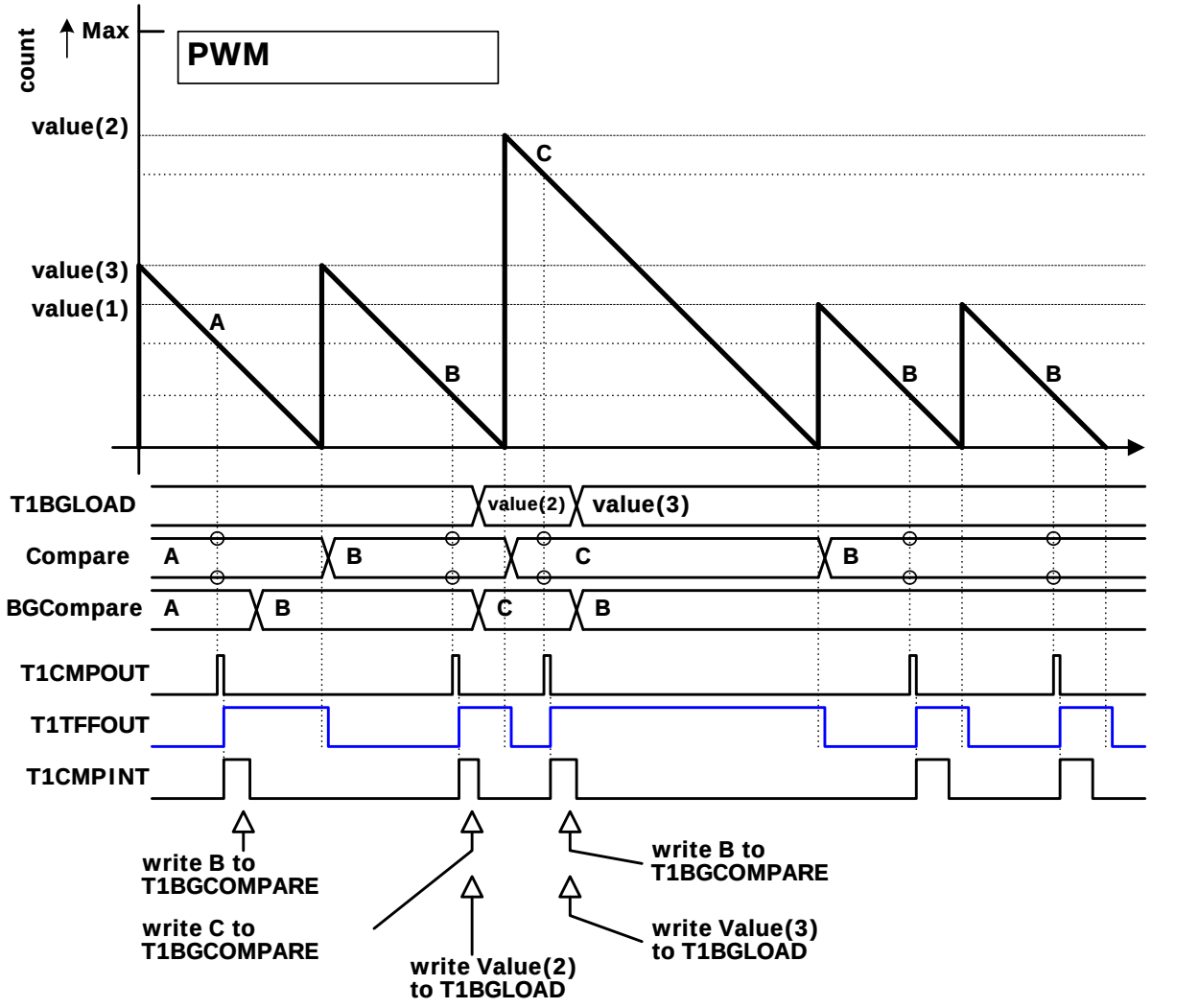

Figure 5.16 Output comparison PWM operation (1)

A PWM wave is generated using the comparison function and the base counter. The period of the PWM wave is set to the base counter setting register (the *[ADVTMR_T1LOAD]* register or the *[ADVTMR_T1BGLOAD]* register). The width of the PWM wave is set to the output comparison setting register (the *[ADVTMR_T1COMPARE]* register or the *[ADVTMR_T1BGCOMPARE]* register).

If the comparison register *[ADVTMR_T1COMPARE]* is used during the operation of the base counter, an unexpected wave may be generated. So the background comparison register *[ADVTMR_T1COMPARE]* is usually used. The set value in this register is transferred to the comparison register *[ADVTMR_T1COMPARE]* when the count value becomes 0000, which is a safer setting.

Example

Register	Event	Reg. Value	Comments
T1CONTROL	—	**0x0028**	16-bit width, Normal, Timer disable, Interrupt disable, Periodic, Wrapping, x1
T1LOAD	—	**0x5555**	Set value: T1LOAD(3)
T1COMPARE	—	**A**	Set value: T1COMPARE(A)
T1BGCOMPARE	—	**A**	Set value: T1BGCOMPARE(A)
T1TFFZERO	—	**0x0001**	TFF0: toggle (Compare or Timer1 terminal count)
T1TFFINV	—	**0x0000**	TFF0: not invert
T1TFFEN	—	**0x0001**	TFF0 enable
T1IOSEL	—	**0x0001**	TFF0 I/O enable
T1CMPINTEN	—	**0x0001**	Compare interrupt enable
T1CMPEN	—	**0x0001**	Compare enable
T1CONTROL	—	**0x00E8**	Timer enable, Interrupt enable
:	:	—	—
—	**count = A**	—	—
—	**T1TFFOUT = 0b1**	—	T1TFFOUT go to "High"
—	**T1CMPINT = 0b1**	—	Compare interrupt occurs
T1BGCOMPARE	—	**B**	Set value: T1BGCOMPARE(B)
T1CMPINTCLR	—	**any value**	Clear Compare Interrupt
—	**T1CMPINT = 0b0**	—	—
:	:	—	—
—	**count = 0x0000**	—	terminal count occurs
—	**T1TFFOUT = 0b0**	—	T1TFFOUT go to "Low"
:	:	—	—
—	**count = B**	—	—
—	**T1TFFOUT = 0b1**	—	T1TFFOUT hold "High"
—	**T1CMPINT = 0b1**	—	Compare interrupt occurs
T1BGCOMPARE	—	**C**	Set value: T1BGCOMPARE(C)
T1BGLOAD	—	**0xAAAA**	Set value: T1BGLOAD(2)
T1CMPINTCLR	—	**any value**	Clear Compare Interrupt
—	**T1CMPINT = 0b0**	—	—
:	:	—	—
—	**count = 0x0000**	—	terminal count occurs
—	**T1TFFOUT = 0b0**	—	T1TFFOUT go to "Low"
:	:	—	—
—	**count = C**	—	—
—	**T1TFFOUT = 0b1**	—	T1TFFOUT hold "High"
—	**T1CMPINT = 0b1**	—	Compare interrupt occurs

Register	Event	Reg. Value	Comments
T1BGCOMPARE	—	**B**	Set value: T1BGCOMPARE(B)
T1BGLOAD	—	**0x4444**	Set value: T1BGLOAD(3)
T1CMPINTCLR	—	**any value**	Clear Compare Interrupt
—	**T1CMPINT = 0b0**	—	—
:	:	—	—
—	**count = 0x0000**	—	terminal count occurs
—	**T1TFFOUT = 0b0**	—	T1TFFOUT go to "Low"
:	:		—
—	**count = B**	—	—
—	**T1TFFOUT = 0b1**	—	T1TFFOUT hold "High"
—	**T1CMPINT = 0b1**	—	Compare interrupt occurs
T1CMPINTCLR	—	**any value**	Clear Compare Interrupt
—	**T1CMPINT = 0b0**	—	—
:	:	—	—
—	**count = 0x0000**	—	terminal count occurs
—	**T1TFFOUT = 0b0**	—	T1TFFOUT go to "Low"
:	:	—	—
—	**count = B**	—	—
—	**T1TFFOUT = 0b1**	—	T1TFFOUT hold "High"
—	**T1CMPINT = 0b1**	—	Compare interrupt occurs
T1CMPINTCLR		**any value**	Clear Compare Interrupt
—	**T1CMPINT = 0b0**	—	—
:	:	—	—
—	**count = 0x0000**	—	terminal count occurs
—	**T1TFFOUT = 0b0**	—	T1TFFOUT go to "Low"

5.4.4. Output Comparison PWM Operation (2)

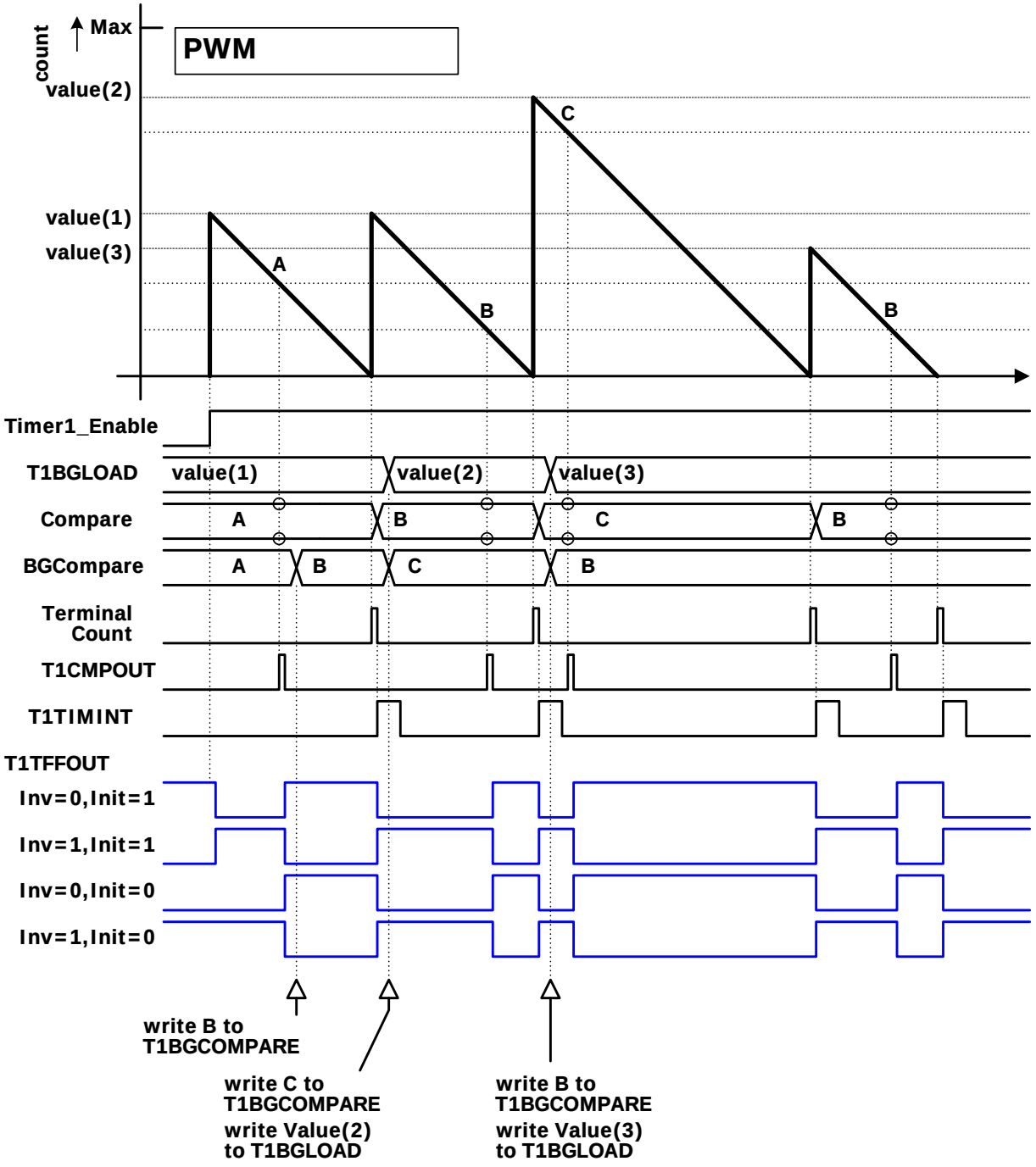

Figure 5.17 Output comparison PWM Operation (2)

In the PWM operation, the *[ADVTMR_T1TFFINIT]* register can initialize the **T1TFFOUT** and the *[ADVTMR_T1TFFINV]* register can reverse the TFF output. When the control register *[ADVTMR_T1CONTROL]* Timer Enable is set to 1, the base counter starts to operate and the output of the PWM is usually 0. When, however, the PWM output should start at 1 or the transition point should be changed from a normal one, the previous scheme is implemented to satisfy such request. Owing to it , the output of the **T1TFFOUT** can be changed as requested.

5.5. Event Counter

5.5.1. Event Counter Operation (EventEn Bit Control)

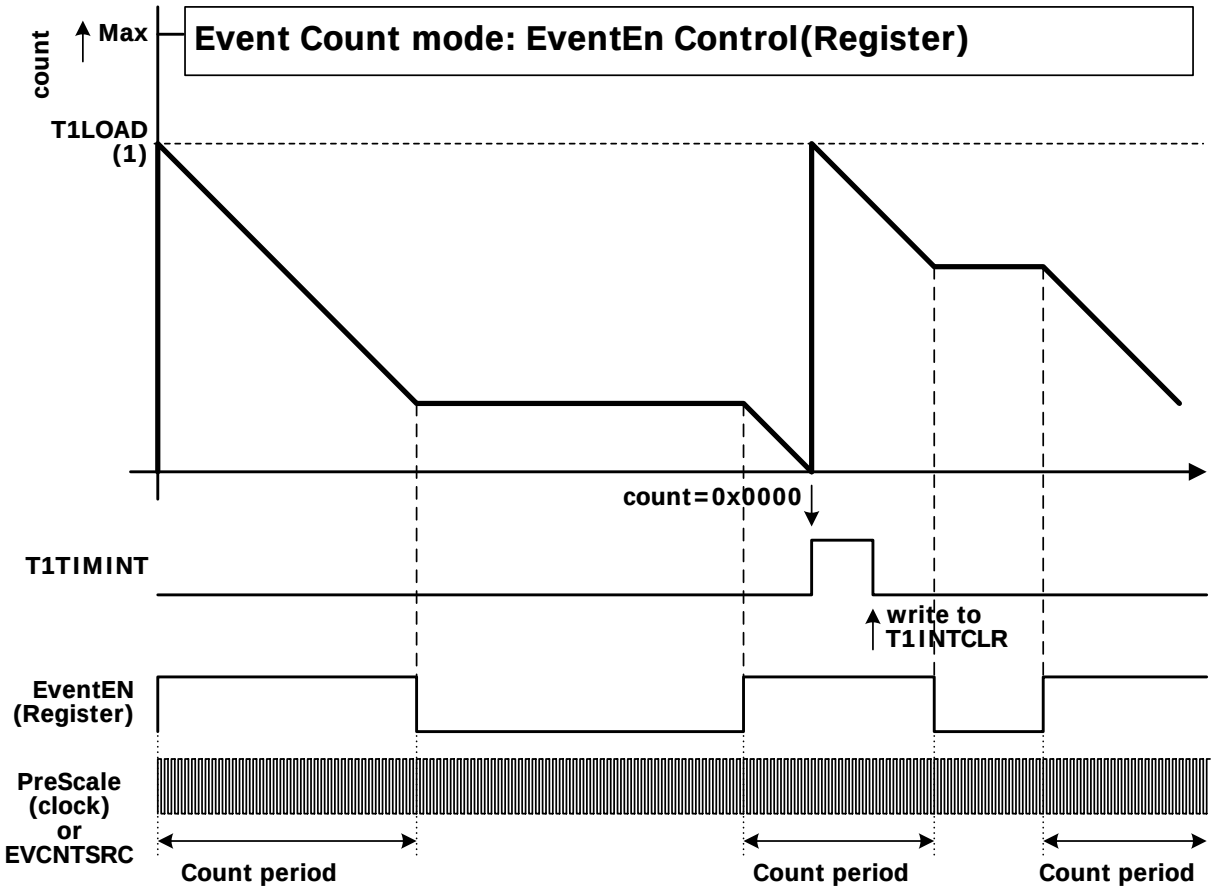

Figure 5.18 Event counter operation (EventEn bit control)

This event counter mode is to start or to stop the counter by a register setting.

The EventSelect bit in the event control register *[ADVTMR_T1EVCONTROL]* is set to the state, "controlled by the EventEn bit only."

When the EventEn bit is set to 1, the event counter starts to count the clock, and when the bit is set to 0, the counter stops.

The clock of the event counter can be selected between the prescaler output and an external input on the **ENCNTSRC** pin. This selection is set by the EventMode bit in the control register *[ADVTMR_T1CONTROL]*.

Example

Register	Event	Reg. Value	Comments
T1CONTROL	—	**0x0228**	16-bit width, Event timer, Timer disable, Interrupt disable, Periodic, Wrapping, x1
T1LOAD	—	**0xAAAA**	Set value: T1LOAD(1)
T1EVCONTROL	—	**0x0001**	**Select: EventEn, NoSync, NoDelay, EventEn = 1**
T1CONTROL	—	**0x02E8**	Timer enable, Interrupt enable
:	**:**	—	count start
T1EVCONTROL	—	**0x0000**	**EventEn = 0:** count stop
:	**:**	—	—
T1EVCONTROL	—	**0x0001**	**EventEn = 1:** count start
:	**:**	—	—
—	**count = 0x0000**	—	terminal count occurs
—	**T1TIMINT = 0b1**	—	Timer interrupt (terminal count) occurs
T1INTCLR	—	**any value**	Clear Timer Interrupt
—	**T1TIMINT = 0b0**	—	—
T1EVCONTROL	—	**0x0000**	**EventEn = 0:** count stop
:	**:**	—	—

5.5.2. Event Counter Operation (EVCNTEN Pin Control: Level)

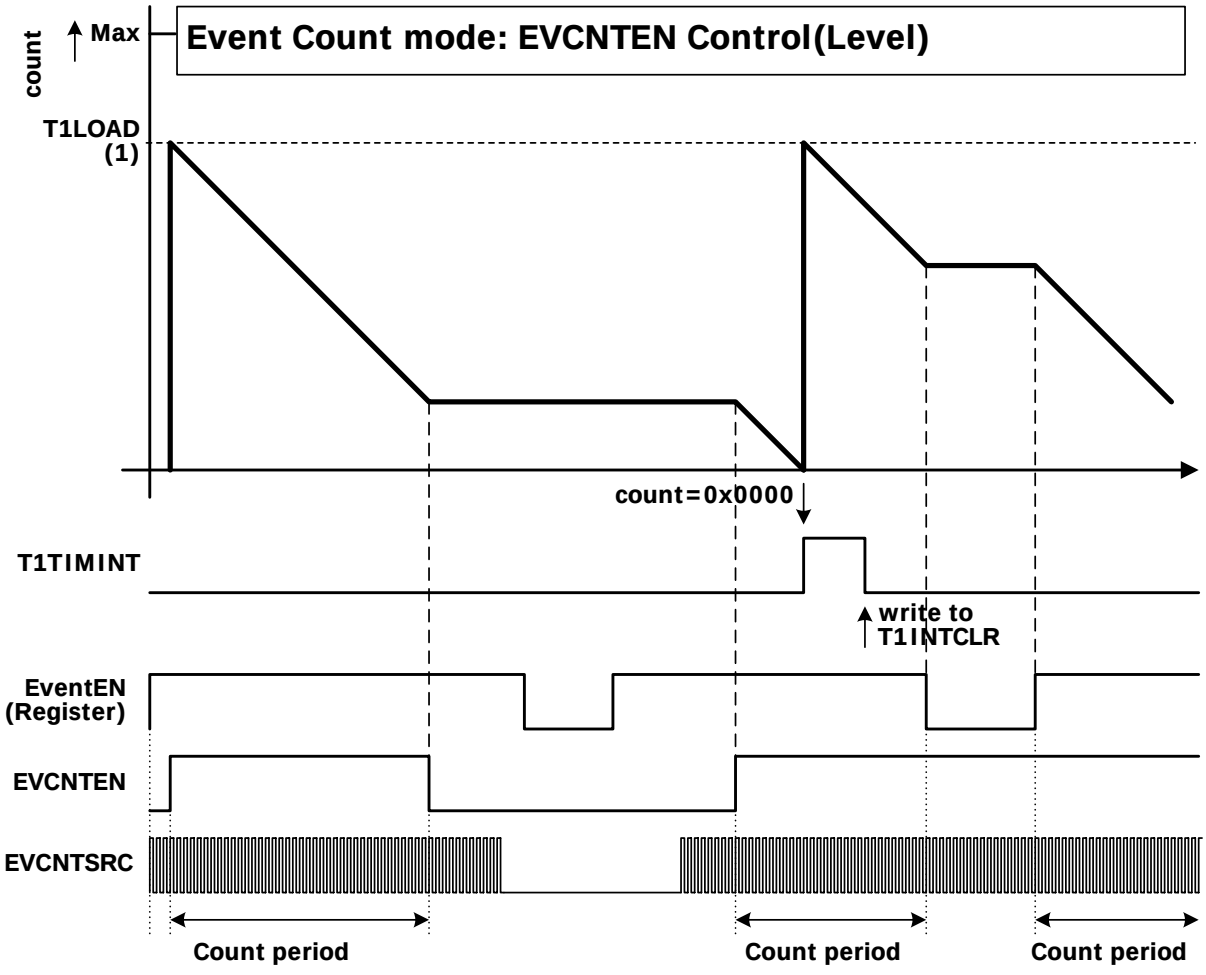

Figure 5.19 Event counter operation (EVCNTEN pin control: Level)

This event counter mode is to start or to stop the counter by a register setting and the **EVCNTEN** level.

The EventSelect bit in the event control register *[ADVTMR_T1EVCONTROL]* is set to the state, "controlled by the EventEn bit and an external input (level)."

When the EventEn bit is set to 1 and the external pin, **EVCNTEN**, is in the High level, the event counter starts to count the clock, and when the bit is set to 0 or the pin is Low, the counter stops.

The clock of the event counter can be selected between the prescaler output and an external input on the **ENCNTSRC** pin. This selection is set by the EventMode bit in the control register *[ADVTMR_T1CONTROL]*.

Example

Register	Event	Reg. Value	Comments
T1CONTROL	—	**0x0328**	16-bit width, Event timer, Timer disable, Interrupt disable, Periodic, Wrapping, x1
T1LOAD	—	**0xAAAA**	Set value**:** T1LOAD(1)
T1EVCONTROL	—	**0x0029**	**Select: EventEn, External input (level), Sync, NoDelay, EventEn = 1**
T1CONTROL	—	**0x03E8**	Timer enable, Interrupt enable
:	**:**	—	count stop
—	**EVCNTEN = 0b1**	—	count start
:	**:**	—	—
—	**EVCNTEN = 0b0**	—	count stop
:	**:**	—	—
T1EVCONTROL	—	**0x0028**	**EventEn = 0 count stop**
:	**:**	—	—
T1EVCONTROL	—	**0x0029**	**EventEn = 1 count start**
:	**:**	—	—
—	**EVCNTEN = 0b1**	—	count start
:	**:**	—	—
—	**count = 0x0000**	—	terminal count occurs
—	**T1TIMINT = 0b1**	—	Timer interrupt (terminal count) occurs
T1INTCLR	—	**any value**	Clear Timer Interrupt
—	**T1TIMINT = 0b0**	—	—
:	**:**	—	—
T1EVCONTROL	—	**0x0028**	**EventEn = 0 count stop**
:	**:**	—	—
T1EVCONTROL	—	**0x0029**	**EventEn = 1 count start**
:	**:**	—	—

5.5.3. Event Counter Operation (EVCNTEN Pin Control: Edge)

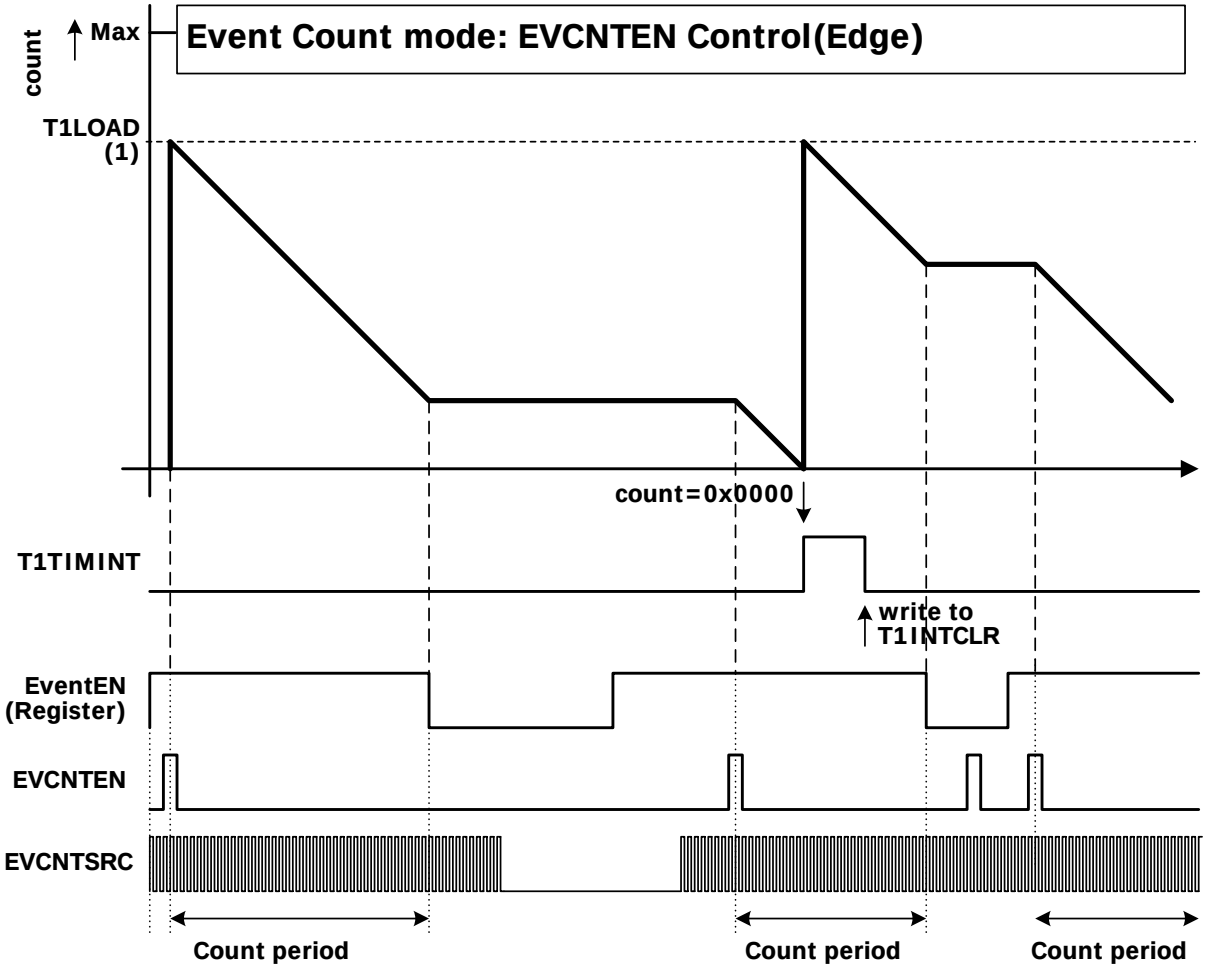

Figure 5.20 Event counter operation (EVCNTEN pin control: edge)

This event counter mode is to start or to stop the counter by a register setting and the **EVCNTEN** edge.

The EventSelect bit in the event control register *[ADVTMR_T1EVCONTROL]* is set to the state, "controlled by the EventEn bit and an external input (edge)."

When the EventEn bit is set to 1 and the rising edge is detected on the external pin, **EVCNTEN**, the event counter starts to count the clock, and when the bit is set to 0, the counter stops.

The clock of the event counter can be selected between the prescaler output and an external input on the **ENCNTSRC** pin. This selection is set by the EventMode bit in the control register *[ADVTMR_T1CONTROL]*.

Example

Register	Event	Reg. Value	Comments
T1CONTROL	—	**0x0328**	16-bit width, Event timer, Timer disable, Interrupt disable, Periodic, Wrapping, x1
T1LOAD	—	**0xAAAA**	Set value**:** T1LOAD(1)
T1EVCONTROL	—	**0x0039**	**Select: EventEn, External input (level), Sync, NoDelay, EventEn = 1**
T1CONTROL	—	**0x03E8**	Timer enable, Interrupt enable
:	**:**	—	count stop
—	**EVCNTEN = 0b1**	—	count start
:	**:**	—	—
T1EVCONTROL	—	**0x0038**	**EventEn = 0 count stop**
:	**:**	—	—
T1EVCONTROL	—	**0x0039**	**EventEn = 1 count start**
:	**:**	—	—
—	**EVCNTEN = 0b1**	—	count start
:	**:**	—	—
—	**count = 0x0000**	—	terminal count occurs
—	**T1TIMINT = 0b1**	—	Timer interrupt (terminal count) occurs
T1INTCLR	—	**any value**	Clear Timer Interrupt
—	**T1TIMINT = 0b0**	—	—
:	**:**	—	—
T1EVCONTROL	—	**0x0038**	**EventEn = 0 count stop**
:	**:**	—	—
T1EVCONTROL	—	**0x0039**	**EventEn = 1 count start**
:	**:**	—	—
—	**T1TIMINT = 0b1**	—	count start
:	**:**	—	—

5.5.4. Event Counter Operation (EvDelay Bit Control)

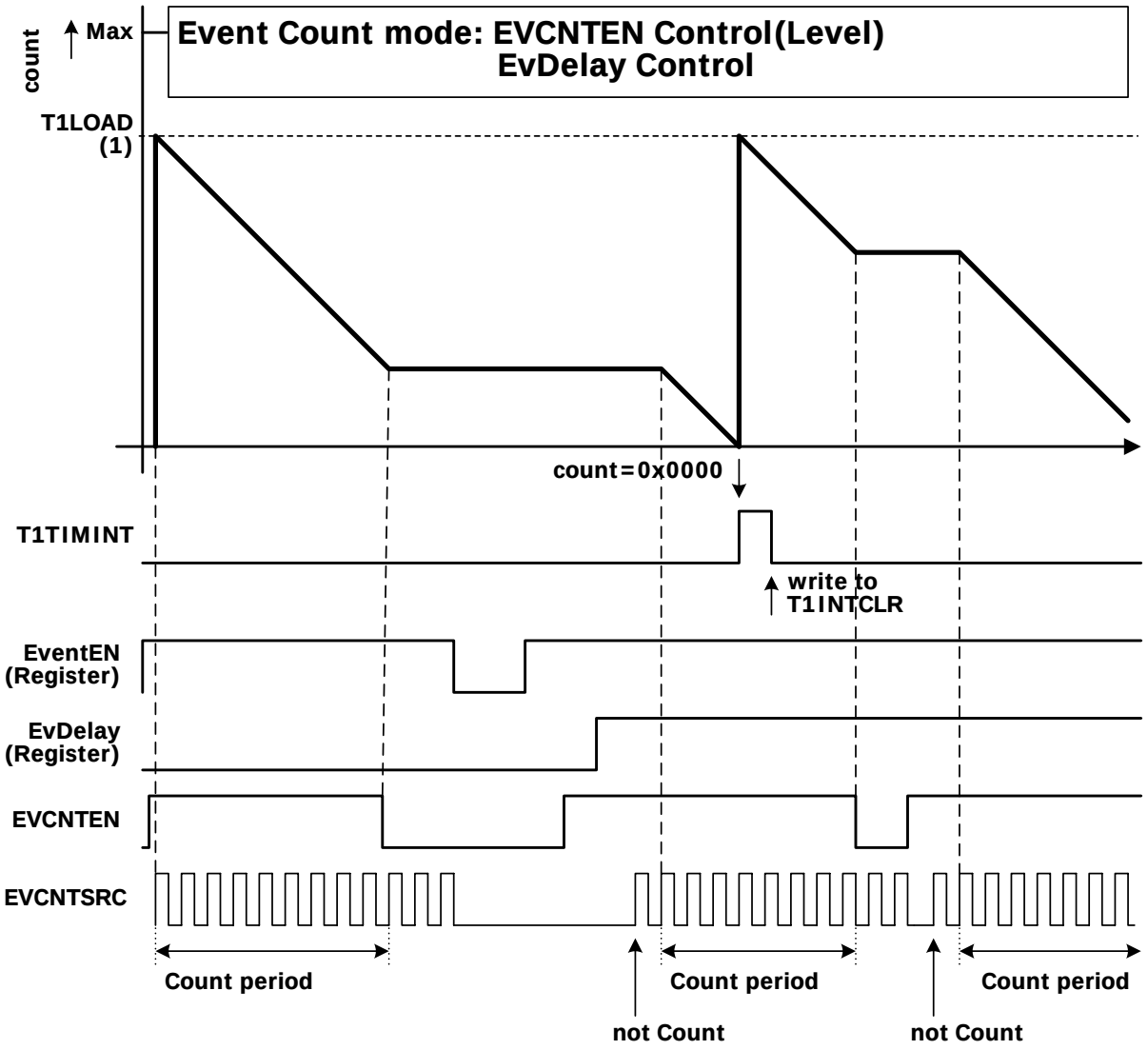

Figure 5.21 Event counter operation (EvDelay bit control)

The EvDelay bit in the event counter control register *[ADVTMR_T1EVCONTROL]* selects whether to count the first event count clock, or not.

When the EvDelay bit is set to 1, the first event count clock is not counted by the event counter. On the other hand, when the EvDelay bit is set to 0, all event count clocks are counted.

Example

Register	Event	Reg. Value	Comments
T1CONTROL	—	**0x0328**	16-bit width, Event timer, Timer disable, Interrupt disable, Periodic, Wrapping, x1
T1LOAD	—	**0xAAAA**	Set value**:** T1LOAD(1)
T1EVCONTROL	—	**0x0029**	**Select: EventEn, External input (level), Sync, NoDelay, EventEn = 1**
T1CONTROL	—	**0x03E8**	Timer enable, Interrupt enable
:	**:**	—	count stop
—	**EVCNTEN = 0b1**	—	count start
:	**:**	—	—
—	**EVCNTEN = 0b0**	—	count stop
:	**:**	—	—
T1EVCONTROL	—	**0x0028**	**EventEn = 0**
:	**:**	—	—
T1EVCONTROL	—	**0x0029**	**EventEn = 1**
:	**:**	—	—
—	**EVCNTEN = 0b1**	—	—
T1EVCONTROL	—	**0x002B**	**Input (level), Sync, Delay, EventEn = 1**
:	**:**	—	—
—	**EVCNTSRC = 1 pulse**	—	not count
—	**EVCNTSRC = 1 pulse**	—	count start
:	**:**	—	—
—	**EVCNTEN = 0b0**	—	—
:	**:**	—	count stop
—	**EVCNTEN = 0b1**	—	—
:	**:**	—	—
—	**EVCNTSRC = 1 pulse**	—	not count
—	**EVCNTSRC = 1 pulse**	—	count start
:	**:**	—	—

5.6. Count Synchronization

5.6.1. Count Synchronization Operation

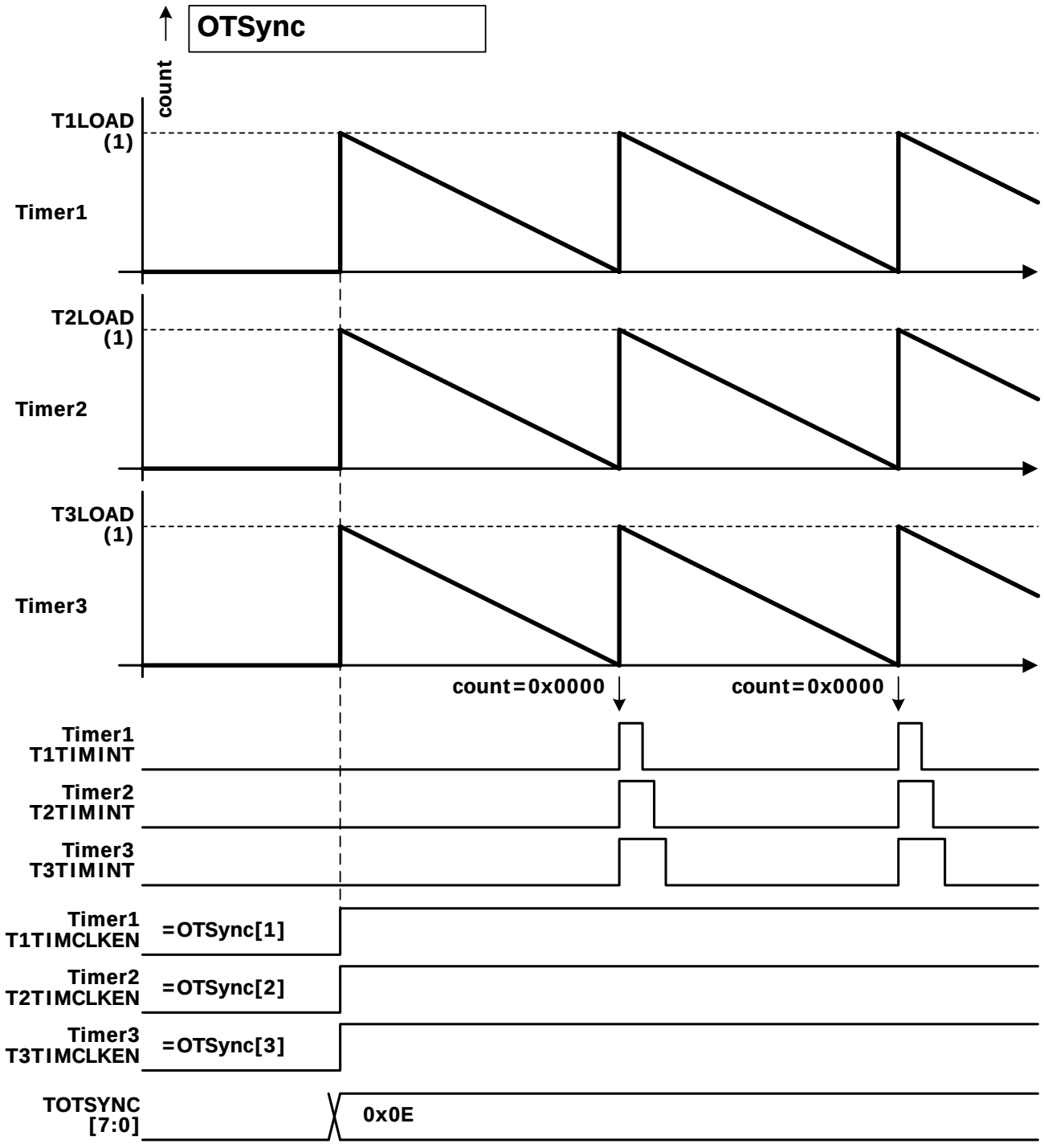

Figure 5.22 Count synchronization operation

One OTSync register *[ADVTMR_OTSYNC]* can control the **TIMCLKEN** signal of each timer. Because the OTSync[3:0] are connected to **TnTIMCLKEN** (**n** is a channel number: one of 0, 1, 2, and 3) of each timer, respectively, the timers which are set to the same value can start to count simultaneously. Setting 1 means the start and 0, the stop.

Example

Register	Event	Reg. Value	Comments
Timer1: T1CONTROL		**0x0028**	16-bit width, Normal, Timer disable, Interrupt disable, Periodic, Wrapping, x1
Timer2: T2CONTROL		**0x0028**	16-bit width, Normal, Timer disable, Interrupt disable, Periodic, Wrapping, x1
Timer3: T3CONTROL		**0x0028**	16-bit width, Normal, Timer disable, Interrupt disable, Periodic, Wrapping, x1
Timer1: T1LOAD		**0xAAAA**	Set value**:** T1LOAD(1)
Timer2: T2LOAD		**0xAAAA**	Set value**:** T2LOAD(1)
Timer3: T3LOAD		**0xAAAA**	Set value**:** T3LOAD(1)
TOTSYNC		**0x0000**	count stop (TIMCLKEN = 0)
:	**:**	—	—
Timer1: T1CONTROL		**0x00E8**	Timer enable, Interrupt enable
Timer2: T2CONTROL		**0x00E8**	Timer enable, Interrupt enable
Timer3: T3CONTROL		**0x00E8**	Timer enable, Interrupt enable
:	**:**	—	count stop
TOTSYNC		**0x000E**	**count start (TIMCLKEN = 1)**
:	**:**	—	count start
—	**count = 0x0000**	—	terminal count occurs
—	**Timer1: T1TIMINT = 0b1**	—	Timer1 interrupt (terminal count) occurs
—	**Timer2: T2TIMINT = 0b1**	—	Timer2 interrupt (terminal count) occurs
—	**Timer3: T3TIMINT = 0b1**	—	Timer3 interrupt (terminal count) occurs
Timer1: T1INTCLR		**any value**	Clear Timer1 interrupt
—	**Timer1: T1TIMINT = 0b0**	—	—
Timer2: T2INTCLR		**any value**	Clear Timer2 interrupt
—	**Timer2: T2TIMINT = 0b0**	—	—
Timer3: T3INTCLR		**any value**	Clear Timer3 interrupt
—	**Timer3: T3TIMINT = 0b0**	—	—
:	**:**	—	—

5.7. DMA Operation

5.7.1. DMA (Input Capture (IC)) Operation

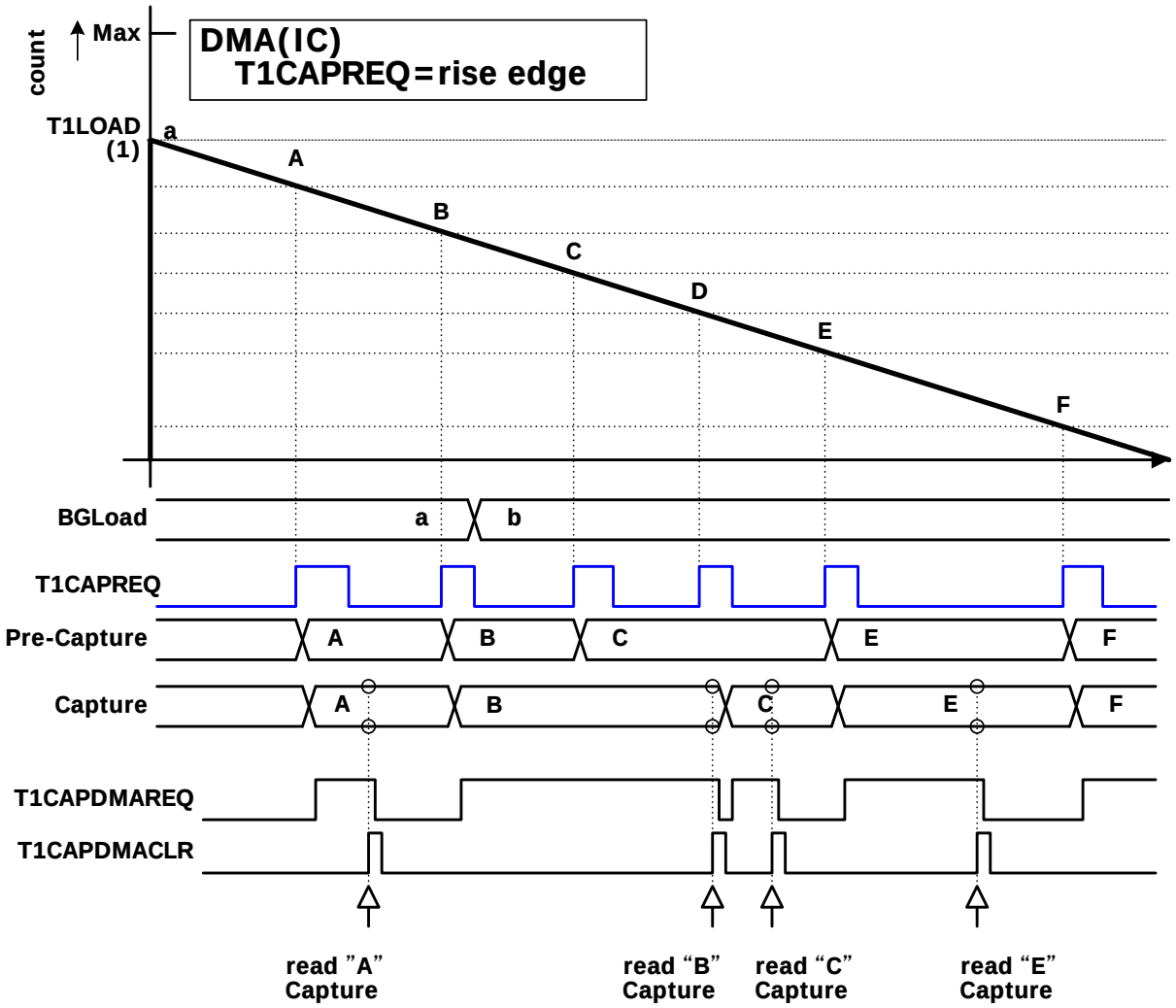

Figure 5.23 DMA (input capture) operation

This DMA mode is to generate the DMA request and its clear by using the capture operation. In this example, when a capture occurs, the DMA request is generated. Though the DMA request (**T1CAPDMAREQ**) is cleared by the DMA clear signal (**T1CAPDMACLR**), the internal DMA request condition is not cleared. The condition is cleared by reading the capture register *[ADVTMR_T1CAPTURE]*. Otherwise, it is not cleared.

One capture buffer (Pre-buffer) is implemented to store two capture data. If the next capture occurs, the latest data is discarded.

(In Figure 5.23 "D" input capture is discarded.)

Example

Register	Event	Reg. Value	Comments
T1CONTROL	—	**0x0028**	16-bit width, Normal, Timer disable, Interrupt disable, Periodic, Wrapping, x1
T1LOAD	—	**0xAAAA**	Set value**:** T1LOAD(1)
T1CAPINTEN	—	**0x0000**	Capture interrupt disable
T1CAPCTRL	—	**0x0001**	Select Capture**:** rise edge
T1CAPDMAEN	—	**0x0001**	Capture DMA enable
T1CAPTURE	—	—	Clear the capture buffer by dummy read of the capture register twice because there is a possibility that previous captured data is stored.
T1CAPTURE	—	—	Same as above
T1CAPEN	—	**0x0001**	Capture enable
T1CONTROL	—	**0x00A8**	Timer enable, Interrupt disable
:	**:**	—	—
—	**T1CAPREQ**	—	Input Capture (rise edge signal)
—	**count = A**	—	—
—	**Pre-Capture = A**	—	Count value into Pre-Capture register
—	**Capture = A**	—	Count value into Capture register
—	**T1CAPDMAREQ = 0b1**	—	Capture DMA request occurs
T1CAPTURE	—	**A**	Read Capture register (DMA transfer)
—	**T1CAPDMACLR = 0b1**	—	Assert CAPDMACLR
—	**T1CAPDMAREQ = 0b0**	—	Clear Capture DMA request
—	**T1CAPDMACLR = 0b0**	—	De-assert CAPDMACLR
:	**:**	—	—
—	**T1CAPREQ**	—	Input Capture (rise edge signal)
—	**count = B**	—	—
—	**Pre-Capture = B**	—	Count value into Pre-Capture register
—	**Capture = B**	—	Count value into Capture register
—	**T1CAPDMAREQ = 0b1**	—	Capture DMA request occurs
:	**:**	—	—
—	**T1CAPREQ**	—	Input Capture (rise edge signal)
—	**count = C**	—	—
—	**Pre-Capture = C**	—	Count value into Pre-Capture register
:	**:**	—	—
—	**T1CAPREQ**	—	Input Capture (rise edge signal)
—	**count = D**	—	—
—	**Pre-Capture**	—	Ignore Input Capture
:	**:**	—	—
T1CAPTURE	—	**B**	Read Capture register (DMA transfer)
—	**T1CAPDMACLR = 0b1**	—	Assert CAPDMACLR
—	**T1CAPDMAREQ = 0b0**	—	Clear Capture DMA request
—	**T1CAPDMACLR = 0b0**	—	De-assert CAPDMACLR
—	**Capture = C**	—	Count value into Capture register
—	**T1CAPDMAREQ = 0b1**	—	Capture DMA request occurs
:	**:**	—	—
T1CAPTURE	—	**C**	Read Capture register (DMA transfer)
—	**T1CAPDMACLR = 0b1**	—	Assert CAPDMACLR
—	**T1CAPDMAREQ = 0b0**	—	Clear Capture DMA request
—	**T1CAPDMACLR = 0b0**	—	De-assert CAPDMACLR
:	**:**	—	—

5.7.2. DMA (Output Comparison (OC)) Operation

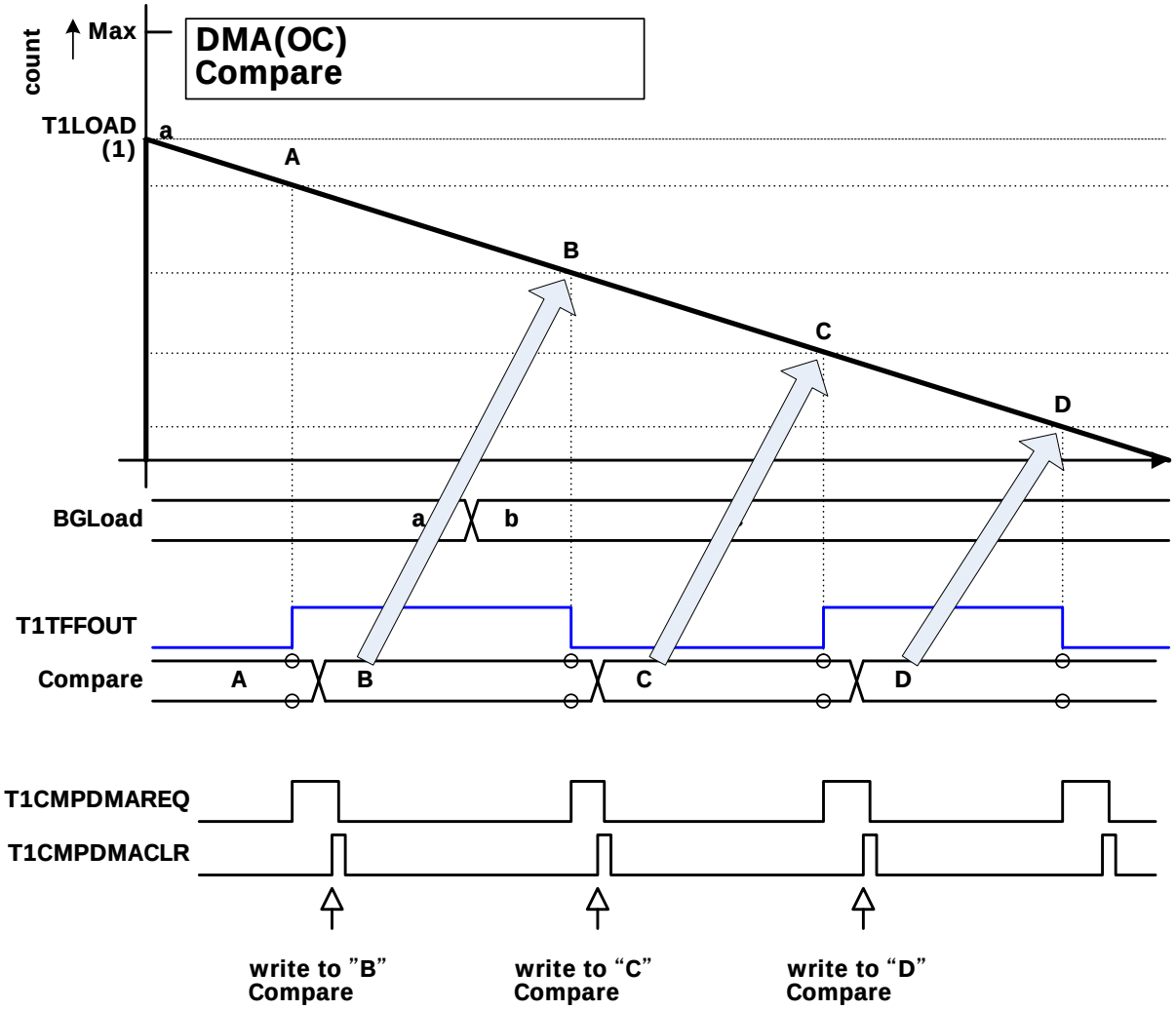

Figure 5.24 DMA (output compare) operation

This DMA mode is to generate the DMA request and its clear by using the comparison operation. In this example, when a comparison occurs, the DMA request is generated. Though the DMA request (**T1CAPDMAREQ**) is cleared by the DMA clear signal (**T1CAPDMACLR**), the internal DMA request condition is not cleared. The condition is cleared by writing to the capture register *[ADVTMR_T1COMPARE]*.

Example

Register	Event	Reg. Value	Comments
T1CONTROL	—	**0x0028**	16-bit width, Normal, Timer disable, Interrupt disable, Periodic, Wrapping, x1
T1LOAD	—	**0x5555**	Set value**:** T1LOAD(1)
T1COMPARE	—	**A**	Set value**:** T1COMPARE(A)
T1TFFCTRL	—	**0x0002**	Select TFF0**:** "Toggle"
T1CMPINTEN	—	**0x0000**	Compare interrupt disable
T1CDMASEL	—	**0x0000**	**DMA request: Compare**
T1CMPDMAEN	—	**0x0001**	Compare DMA enable
T1TFFEN	—	**0x0001**	TFF0 enable
T1CMPEN	—	**0x0001**	Compare enable
T1CONTROL	—	**0x00A8**	Timer enable, Interrupt disable
:	**:**	—	—
—	**count = A**	—	—
—	**T1TFFOUT = 0b1**	—	T1TFFOUT go to "High"
—	**T1CMPDMAREQ = 0b1**	—	Compare DMA request occurs
T1COMPARE		**B**	Set value**:** T1COMPARE(B) (**DMA transfer**)
—	**T1CMPDMACLR = 0b1**	—	Assert CMPDMACLR
—	**T1CMPDMAREQ = 0b0**	—	Clear Compare DMA request
—	**T1CMPDMACLR = 0b0**	—	De-assert CMPDMACLR
:	**:**	—	—
—	**count = B**	—	—
—	**T1TFFOUT = 0b0**	—	T1TFFOUT go to "Low"
—	**T1CMPDMAREQ = 0b1**	—	Compare DMA request occurs
T1COMPARE		**C**	Set value**:** T1COMPARE(C) (**DMA transfer**)
—	**T1CMPDMACLR = 0b1**	—	Assert CMPDMACLR
—	**T1CMPDMAREQ = 0b0**	—	Clear Compare DMA request
—	**T1CMPDMACLR = 0b0**	—	De-assert CAPDMACLR
:	**:**	—	—

5.7.3. DMA (Output Comparison and Base Counter) Operation

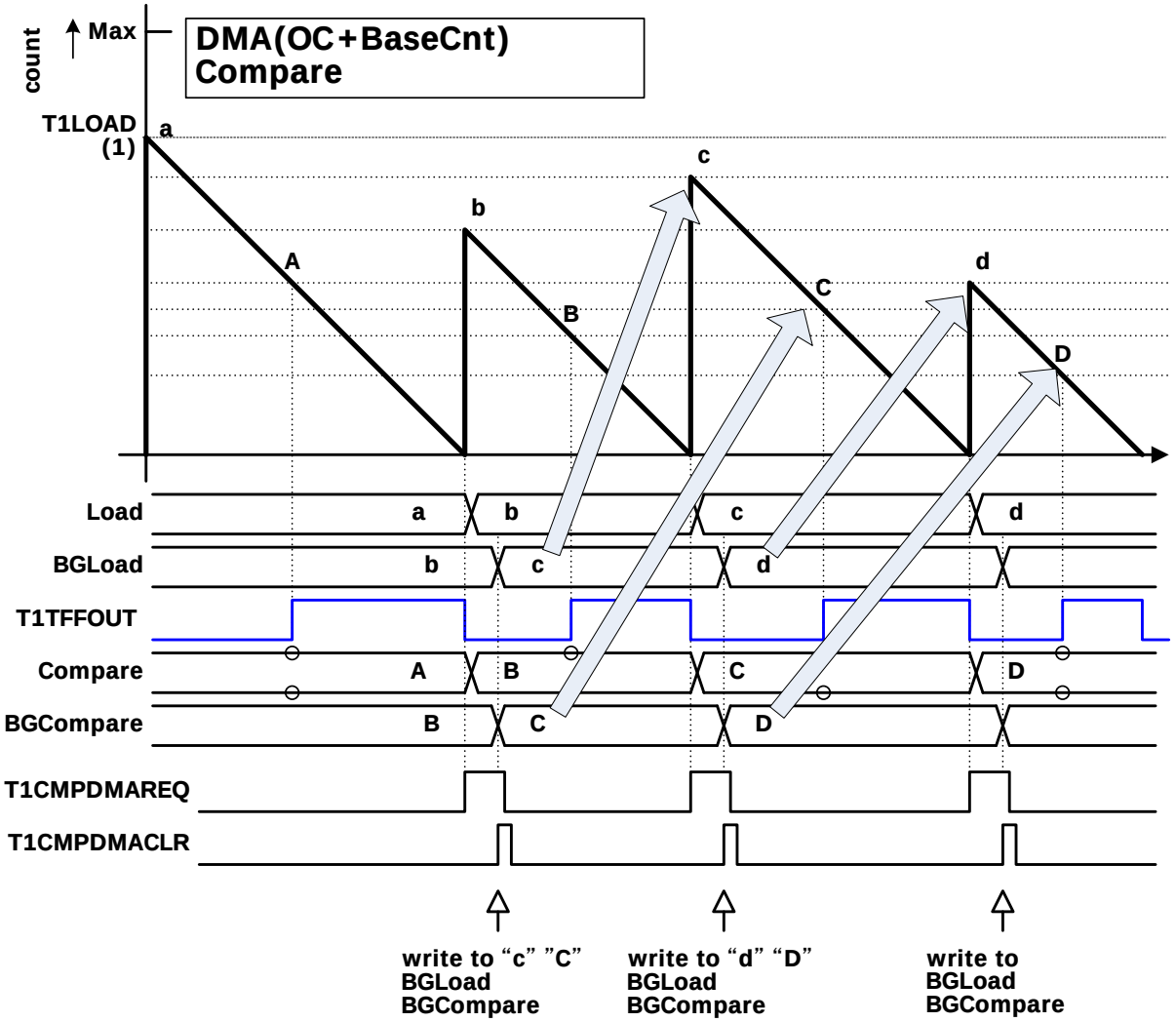

Figure 5.25 DMA (output comparison and base counter) operation

This DMA mode is to generate the DMA request and its clear by using the comparison operation. In this example, when the base counter becomes 0000, the DMA request is generated. This example is usually used for the PWM operation.

When the base counter is 0000, the load and comparison values are set. The setting for the next cycle is not suitable for generating a continuous waveform because the setting takes some time. (The setting for the next cycle should be done by the CPU in the comparison interrupt process.)

Though the DMA request (**T1CAPDMAREQ**) is cleared by the DMA clear signal (**T1CAPDMACLR**), the internal DMA request condition is not cleared. The condition is cleared by writing to the background comparison register *[ADVTMR_T1BGCOMPARE]*.

The background comparison register *[ADVTMR_T1BGCOMPARE]* can be accessed in 32-bit unit by setting 1 to *[ADVTMR_T1CDMASEL]* (the upper 16-bit *[ADVTMR_T1BGLOAD]* and the lower 16-bit *[ADVTMR_BGCOMPARE]*). One 32-bit data transfer can set both registers.

Example

Register	Event	Reg. Value	Comments
T1CONTROL	—	**0x0028**	16-bit width, Normal, Timer disable, Interrupt disable, Periodic, Wrapping, x1
T1LOAD	—	**a**	Set value**:** T1LOAD(a)
T1BGLOAD	—	**b**	Set value**:** T1BGLOAD(b)
T1COMPARE	—	**A**	Set value**:** T1COMPARE(A)
T1BGCOMPARE	—	**B**	Set value**:** T1BGCOMPARE(B)
T1TFFCTRL	—	**0x0002**	Select TFF0**:** "Toggle"
T1CMPINTEN	—	**0x0000**	Compare interrupt disable
T1CDMASEL	—	**0x0001**	**DMA request: terminal count**
T1CMPDMAEN	—	**0x0001**	Compare DMA enable
T1TFFEN	—	**0x0001**	TFF0 enable
T1CMPEN	—	**0x0001**	Compare enable
T1CONTROL	—	**0x00A8**	Timer enable, Interrupt disable
:	**:**	—	—
—	**count = A**	—	—
—	**T1TFFOUT = 0b1**	—	T1TFFOUT go to "High"
:	**:**	—	—
—	**count = 0x0000**	—	terminal count occurs
—	**T1CMPDMAREQ = 0b1**	—	Compare DMA request occurs
T1BGLOAD	—	**c**	Set value**:** T1BGLOAD(c) (**DMA transfer**)
T1BGCOMPARE	—	**C**	Set value**:** T1BGCOMPARE(C) (**DMA transfer**)
—	**T1CMPDMACLR = 0b1**	—	Assert CMPDMACLR
—	**T1CMPDMAREQ = 0b0**	—	Clear Compare DMA request
—	**T1CMPDMACLR = 0b0**	—	De-assert CMPDMACLR
:	**:**	—	—
—	**count = B**	—	—
—	**T1TFFOUT = 0b1**	—	T1TFFOUT go to "High"
:	**:**	—	—
—	**count = 0x0000**	—	terminal count occurs
—	**T1CMPDMAREQ = 0b1**	—	Compare DMA request occurs
T1BGLOAD	—	**d**	Set value**:** T1BGLOAD(d) (**DMA transfer**)
T1COMPARE	—	**D**	Set value**:** T1BGCOMPARE(D) (**DMA transfer**)
—	**T1CMPDMACLR = 0b1**	—	Assert CMPDMACLR
—	**T1CMPDMAREQ = 0b0**	—	Clear Compare DMA request
—	**T1CMPDMACLR = 0b0**	—	De-assert CMPDMACLR
:	**:**	—	—

5.8. Top Connection of ADVTMR

Multiplexers are implemented on the boundary of the ADVTMR block to select input signals. The selection is done by registers in the ADVTMR.

(*[ADVTMR_TnEVSEL],[ADVTMR_TnCAPSEL]* register) (**n** is a channel number: 0, 1, 2, and 3.)

- **TnEVSEL[6:4]** (EVCNTSRC_Sel field) selects the input signal to **EVCNTSRC.**
- **TnEVSEL[2:0]** (EVCNTEN_Sel field) selects the input signal to **EVCNTEN.**
- **TnCAPSEL[2:0]** (CapSel field) selects the input signal to **CAPREQ.**

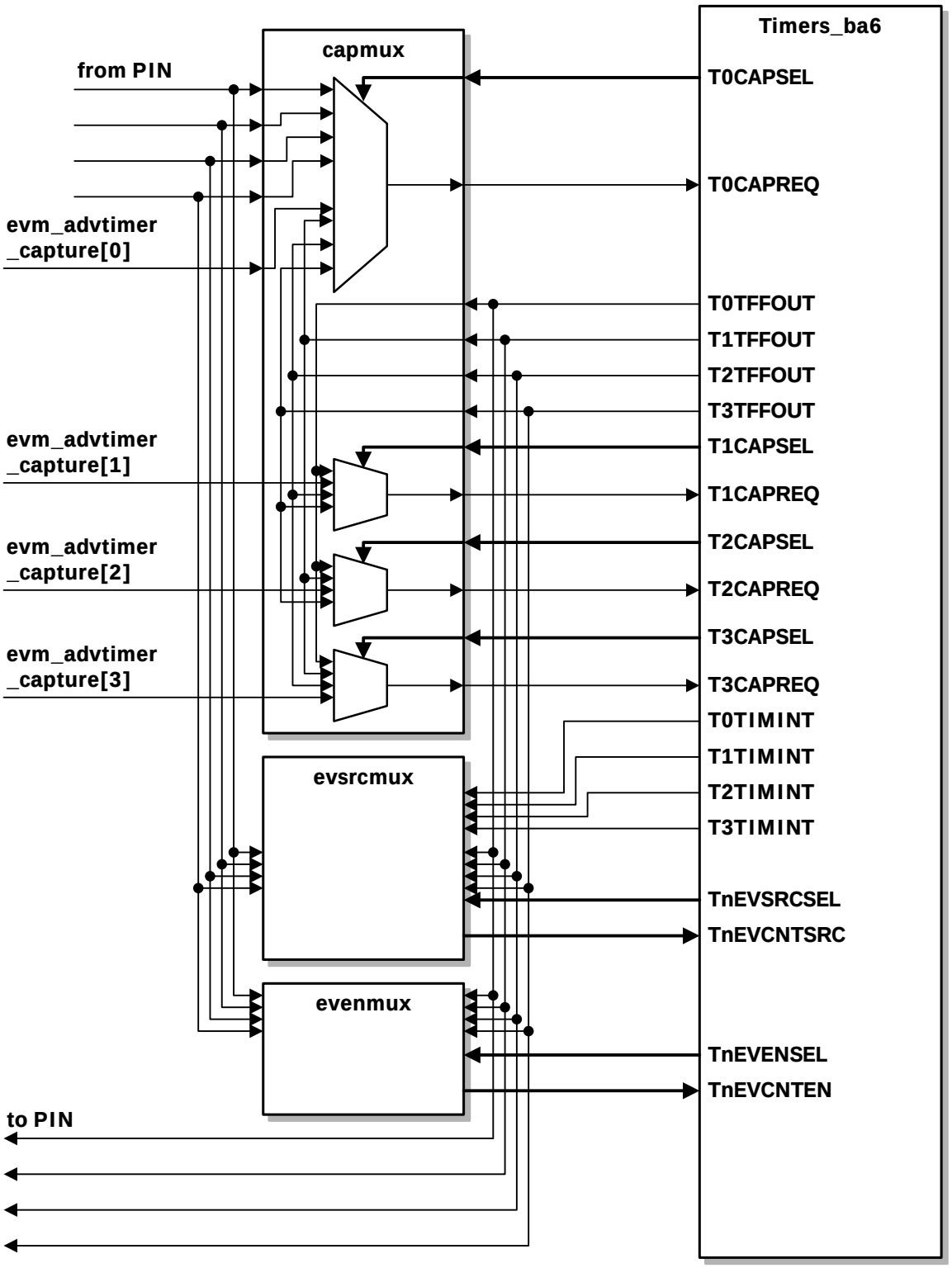

Figure 5.26 Top connection of ADVTMR

Table 5.3 TnEVSEL register setting (1)

ch	TnEVSEL [6:4]	Connect Block	Connect signal	Pin share	Description
ch0	000	PIN	MCU_UA0_RXD	FMODE2	from PIN signal
		PIN	MCU_GPIO_12	FMODE3	from PIN signal
	001	PIN	MCU_UA0_TXD	FMODE2	from PIN signal
		PIN	MCU_GPIO_13	FMODE3	from PIN signal
	010	PIN	MCU_I2C0_DATA	FMODE2	from PIN signal
	011	PIN	MCU_I2C0_CLK	FMODE2	from PIN signal
	100	ADVTMR	T3TIMINT	—	ch3->ch0 cascade connect
	101	ADVTMR	T1TFFOUT	—	from ch1 output signal
	110	ADVTMR	T2TFFOUT	—	from ch2 output signal
	111	ADVTMR	T3TFFOUT	—	from ch3 output signal
ch1	000	PIN	MCU_UA0_RXD	FMODE2	from PIN signal
		PIN	MCU_GPIO_12	FMODE3	from PIN signal
	001	PIN	MCU_UA0_TXD	FMODE2	from PIN signal
		PIN	MCU_GPIO_13	FMODE3	from PIN signal
	010	PIN	MCU_I2C0_DATA	FMODE2	from PIN signal
	011	PIN	MCU_I2C0_CLK	FMODE2	from PIN signal
	100	ADVTMR	T0TFFOUT	—	from ch0 output signal
	101	ADVTMR	T0TIMINT	—	ch0->ch1 cascade connect
	110	ADVTMR	T2TFFOUT	—	from ch2 output signal
	111	ADVTMR	T3TFFOUT	—	from ch3 output signal
ch2	000	PIN	MCU_UA0_RXD	FMODE2	from PIN signal
		PIN	MCU_GPIO_12	FMODE3	from PIN signal
	001	PIN	MCU_UA0_TXD	FMODE2	from PIN signal
		PIN	MCU_GPIO_13	FMODE3	from PIN signal
	010	PIN	MCU_I2C0_DATA	FMODE2	from PIN signal
	011	PIN	MCU_I2C0_CLK	FMODE2	from PIN signal
	100	ADVTMR	T0TFFOUT	—	from ch0 output signal
	101	ADVTMR	T1TFFOUT	—	from ch1 output signal
	110	ADVTMR	T1TIMINT	—	ch1->ch2 cascade connect
	111	ADVTMR	T3TFFOUT	—	from ch3 output signal
ch3	000	PIN	MCU_UA0_RXD	FMODE2	from PIN signal
		PIN	MCU_GPIO_12	FMODE3	from PIN signal
	001	PIN	MCU_UA0_TXD	FMODE2	from PIN signal
		PIN	MCU_GPIO_13	FMODE3	from PIN signal
	010	PIN	MCU_I2C0_DATA	FMODE2	from PIN signal
	011	PIN	MCU_I2C0_CLK	FMODE2	from PIN signal
	100	ADVTMR	T0TFFOUT	—	from ch0 output signal
	101	ADVTMR	T1TFFOUT	—	from ch1 output signal
	110	ADVTMR	T2TFFOUT	—	from ch2 output signal
	111	ADVTMR	T2TIMINT	—	ch2->ch3 cascade connect

Table 5.4 TnEVSEL register setting (2)

ch	TnEVSEL [2:0]	Connect Block	Connect signal	Pin share	Description
ch0	000	PIN	MCU_UA0_RXD	FMODE2	from PIN signal
		PIN	MCU_GPIO_12	FMODE3	from PIN signal
	001	PIN	MCU_UA0_TXD	FMODE2	from PIN signal
		PIN	MCU_GPIO_13	FMODE3	from PIN signal
	010	PIN	MCU_I2C0_DATA	FMODE2	from PIN signal
	011	PIN	MCU_I2C0_CLK	FMODE2	from PIN signal
	100	ADVTMR	T0TFFOUT	—	from ch0 output signal
	101	ADVTMR	T1TFFOUT	—	from ch1 output signal
	110	ADVTMR	T2TFFOUT	—	from ch2 output signal
	111	ADVTMR	T3TFFOUT	—	from ch3 output signal
ch1	000	PIN	MCU_UA0_RXD	FMODE2	from PIN signal
		PIN	MCU_GPIO_12	FMODE3	from PIN signal
	001	PIN	MCU_UA0_TXD	FMODE2	from PIN signal
		PIN	MCU_GPIO_13	FMODE3	from PIN signal
	010	PIN	MCU_I2C0_DATA	FMODE2	from PIN signal
	011	PIN	MCU_I2C0_CLK	FMODE2	from PIN signal
	100	ADVTMR	T0TFFOUT	—	from ch0 output signal
	101	ADVTMR	T1TFFOUT	—	from ch1 output signal
	110	ADVTMR	T2TFFOUT	—	from ch2 output signal
	111	ADVTMR	T3TFFOUT	—	from ch3 output signal
ch2	000	PIN	MCU_UA0_RXD	FMODE2	from PIN signal
		PIN	MCU_GPIO_12	FMODE3	from PIN signal
	001	PIN	MCU_UA0_TXD	FMODE2	from PIN signal
		PIN	MCU_GPIO_13	FMODE3	from PIN signal
	010	PIN	MCU_I2C0_DATA	FMODE2	from PIN signal
	011	PIN	MCU_I2C0_CLK	FMODE2	from PIN signal
	100	ADVTMR	T0TFFOUT	—	from ch0 output signal
	101	ADVTMR	T1TFFOUT	—	from ch1 output signal
	110	ADVTMR	T2TFFOUT	—	from ch2 output signal
	111	ADVTMR	T3TFFOUT	—	from ch3 output signal
ch3	000	PIN	MCU_UA0_RXD	FMODE2	from PIN signal
		PIN	MCU_GPIO_12	FMODE3	from PIN signal
	001	PIN	MCU_UA0_TXD	FMODE2	from PIN signal
		PIN	MCU_GPIO_13	FMODE3	from PIN signal
	010	PIN	MCU_I2C0_DATA	FMODE2	from PIN signal
	011	PIN	MCU_I2C0_CLK	FMODE2	from PIN signal
	100	ADVTMR	T0TFFOUT	—	from ch0 output signal
	101	ADVTMR	T1TFFOUT	—	from ch1 output signal
	110	ADVTMR	T2TFFOUT	—	from ch2 output signal
	111	ADVTMR	T3TFFOUT	—	from ch3 output signal

Table 5.5 TnCAPSEL register setting

ch	TnCAPSEL [2:0]	Connect Block	Connect signal	Pin share	Description
ch0	000	PIN	MCU_UA0_RXD	FMODE2	from PIN signal
		PIN	MCU_GPIO_12	FMODE3	from PIN signal
	001	PIN	MCU_UA0_TXD	FMODE2	from PIN signal
		PIN	MCU_GPIO_13	FMODE3	from PIN signal
	010	PIN	MCU_I2C0_DATA	FMODE2	from PIN signal
	011	PIN	MCU_I2C0_CLK	FMODE2	from PIN signal
	100	EVM	evm_advtimer_capture[0]	—	from evm output signal
	101	ADVTMR	T1TFFOUT	—	from ch1 output signal
	110	ADVTMR	T2TFFOUT	—	from ch2 output signal
	111	ADVTMR	T3TFFOUT	—	from ch3 output signal
ch1	000	PIN	MCU_UA0_RXD	FMODE2	from PIN signal
		PIN	MCU_GPIO_12	FMODE3	from PIN signal
	001	PIN	MCU_UA0_TXD	FMODE2	from PIN signal
		PIN	MCU_GPIO_13	FMODE3	from PIN signal
	010	PIN	MCU_I2C0_DATA	FMODE2	from PIN signal
	011	PIN	MCU_I2C0_CLK	FMODE2	from PIN signal
	100	ADVTMR	T0TFFOUT	—	from ch0 output signal
	101	EVM	evm_advtimer_capture[1]	—	from evm output signal
	110	ADVTMR	T2TFFOUT	—	from ch2 output signal
	111	ADVTMR	T3TFFOUT	—	from ch3 output signal
ch2	000	PIN	MCU_UA0_RXD	FMODE2	from PIN signal
		PIN	MCU_GPIO_12	FMODE3	from PIN signal
	001	PIN	MCU_UA0_TXD	FMODE2	from PIN signal
		PIN	MCU_GPIO_13	FMODE3	from PIN signal
	010	PIN	MCU_I2C0_DATA	FMODE2	from PIN signal
	011	PIN	MCU_I2C0_CLK	FMODE2	from PIN signal
	100	ADVTMR	T0TFFOUT	—	from ch0 output signal
	101	ADVTMR	T1TFFOUT	—	from ch1 output signal
	110	EVM	evm_advtimer_capture[2]	—	from evm output signal
	111	ADVTMR	T3TFFOUT	—	from ch3 output signal
ch3	000	PIN	MCU_UA0_RXD	FMODE2	from PIN signal
		PIN	MCU_GPIO_12	FMODE3	from PIN signal
	001	PIN	MCU_UA0_TXD	FMODE2	from PIN signal
		PIN	MCU_GPIO_13	FMODE3	from PIN signal
	010	PIN	MCU_I2C0_DATA	FMODE2	from PIN signal
	011	PIN	MCU_I2C0_CLK	FMODE2	from PIN signal
	100	ADVTMR	T0TFFOUT	—	from ch0 output signal
	101	ADVTMR	T1TFFOUT	—	from ch1 output signal
	110	ADVTMR	T2TFFOUT	—	from ch2 output signal
	111	EVM	evm_advtimer_capture[3]	—	from evm output signal

5.9. Interrupt Generation

Three interrupts are supported; Base counter interrupt, Capture interrupt, and Comparison interrupt.

The base counter interrupt is generated when the down counter becomes 0000 with Interrupt_Enable = 1 in the control register ***[ADVTMR_TnCONTROL]*** (**n** is a channel number: 0, 1, 2, or 3, hereafter the same). The timing of the interrupt generation and its clear is shown in Figure 5.27. The interrupt **TIMINT** is asserted at the rising edge of **TIMCLK** when **TIMCLKEN**=1 .

The **TIMINT** is deasserted at the PCLK timing when the interrupt clear register ***[ADVTMR_TnINTCLR]*** is written. The internal interrupt cause is cleared at the rising edge of the following **TIMCLK** when **TIMCLKEN**=1.

The capture interrupt is generated when a count is captured and stored in the capture buffer. The timing is the same as that of the base counter interrupt.

The outline diagram of the base counter interrupt generator is shown in Figure 5.28. The interrupt is requested through a normal path and a test register path. The test register path is controlled by the Test_Mode_Enable bit in the test register ***[ADVTMR_TITCR]***. Usually Test_Mode_Enable = 0.

The outline diagram of the capture interrupt generator is shown in Figure 5.29. The circuit configuration is the same as that of the base counter interrupt generator.

The outline diagram of the comparison interrupt generator is shown in Figure 5.30.The circuit configuration is the same as that of the base counter interrupt generator.

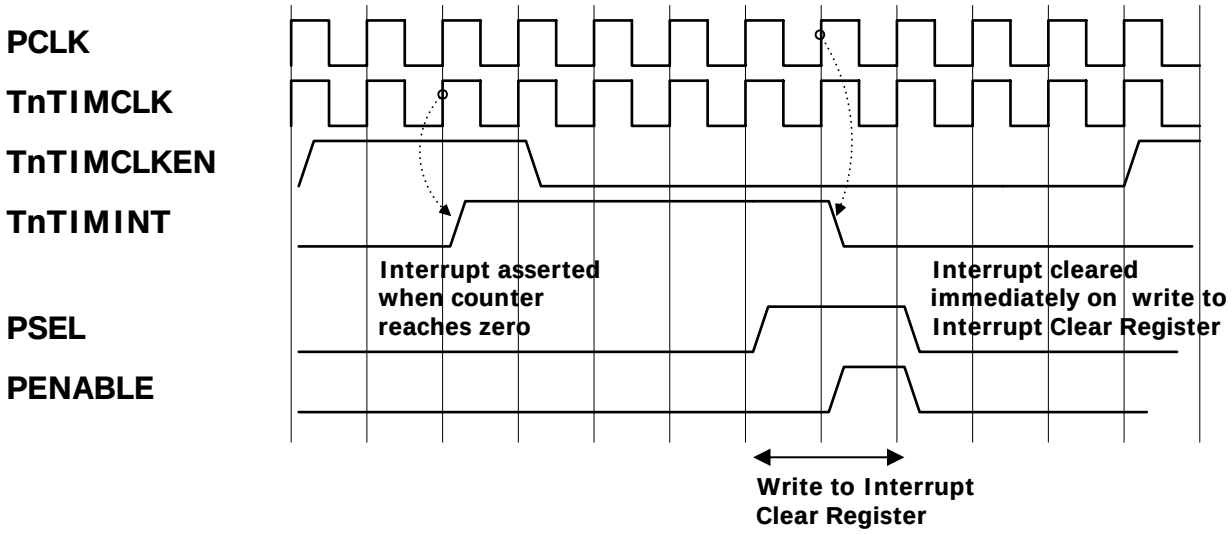

Figure 5.27 Example of interrupt generation

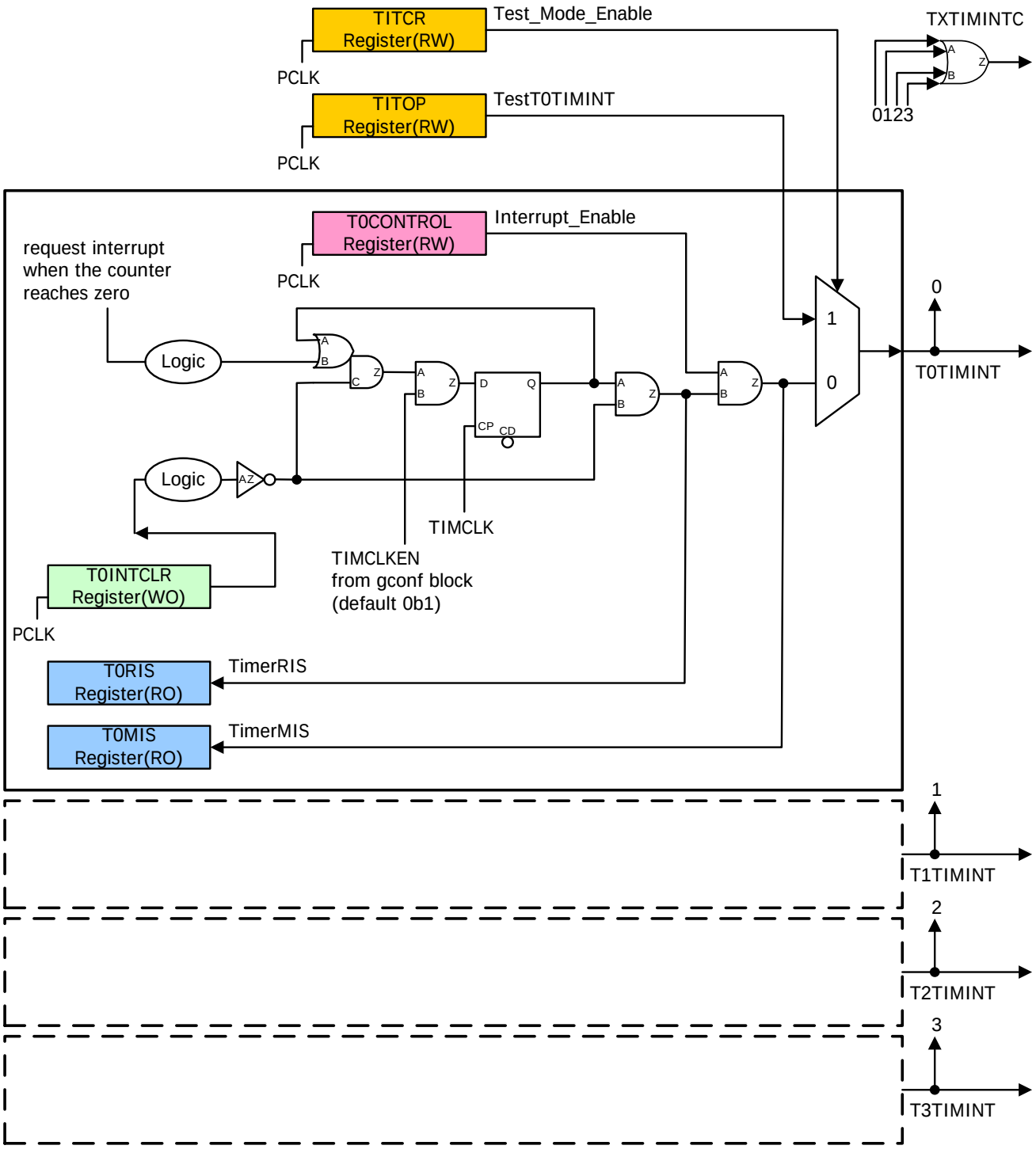

Figure 5.28 Outline diagram of interrupt generator

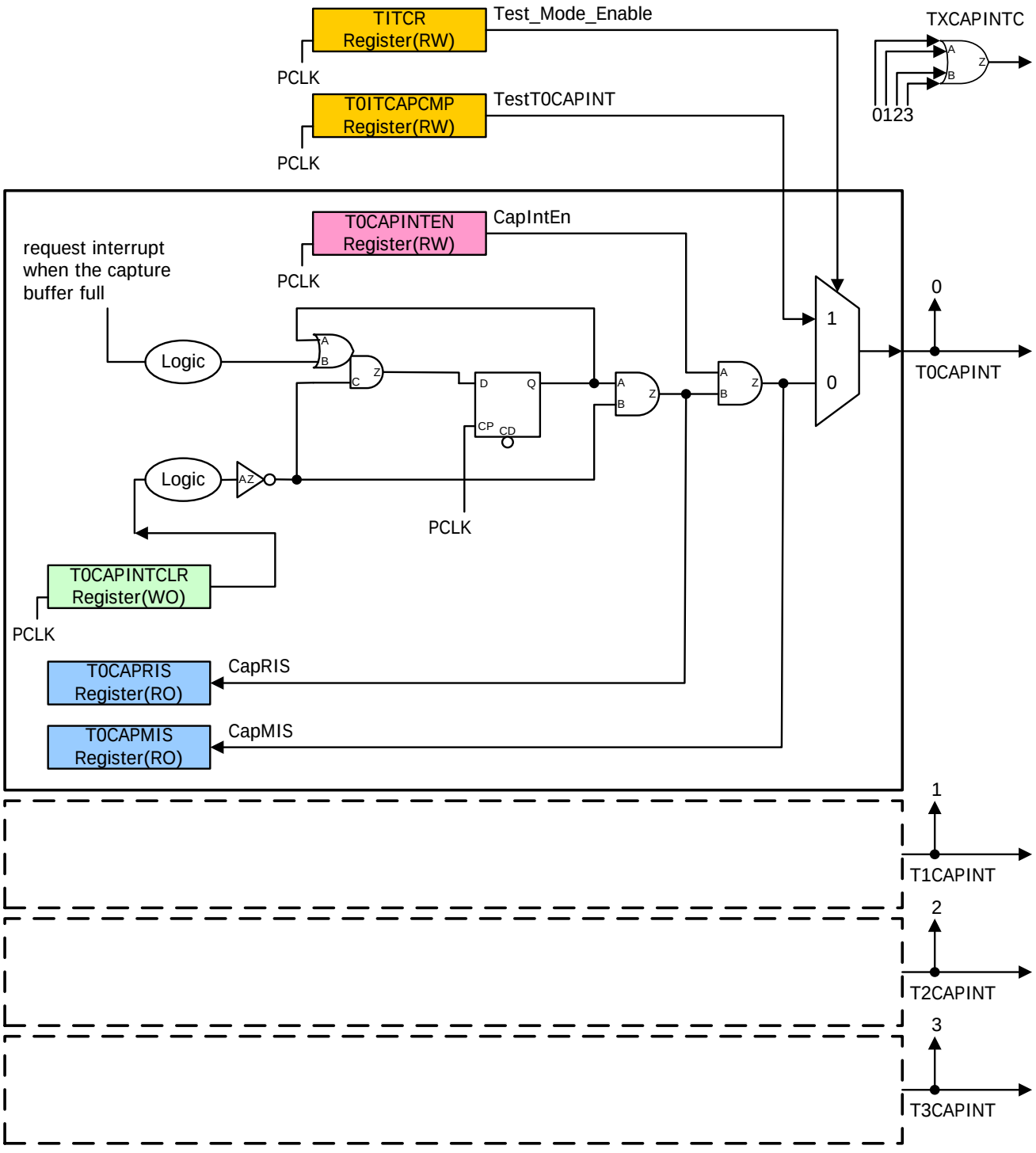

Figure 5.29 Outline diagram of capture interrupt generator

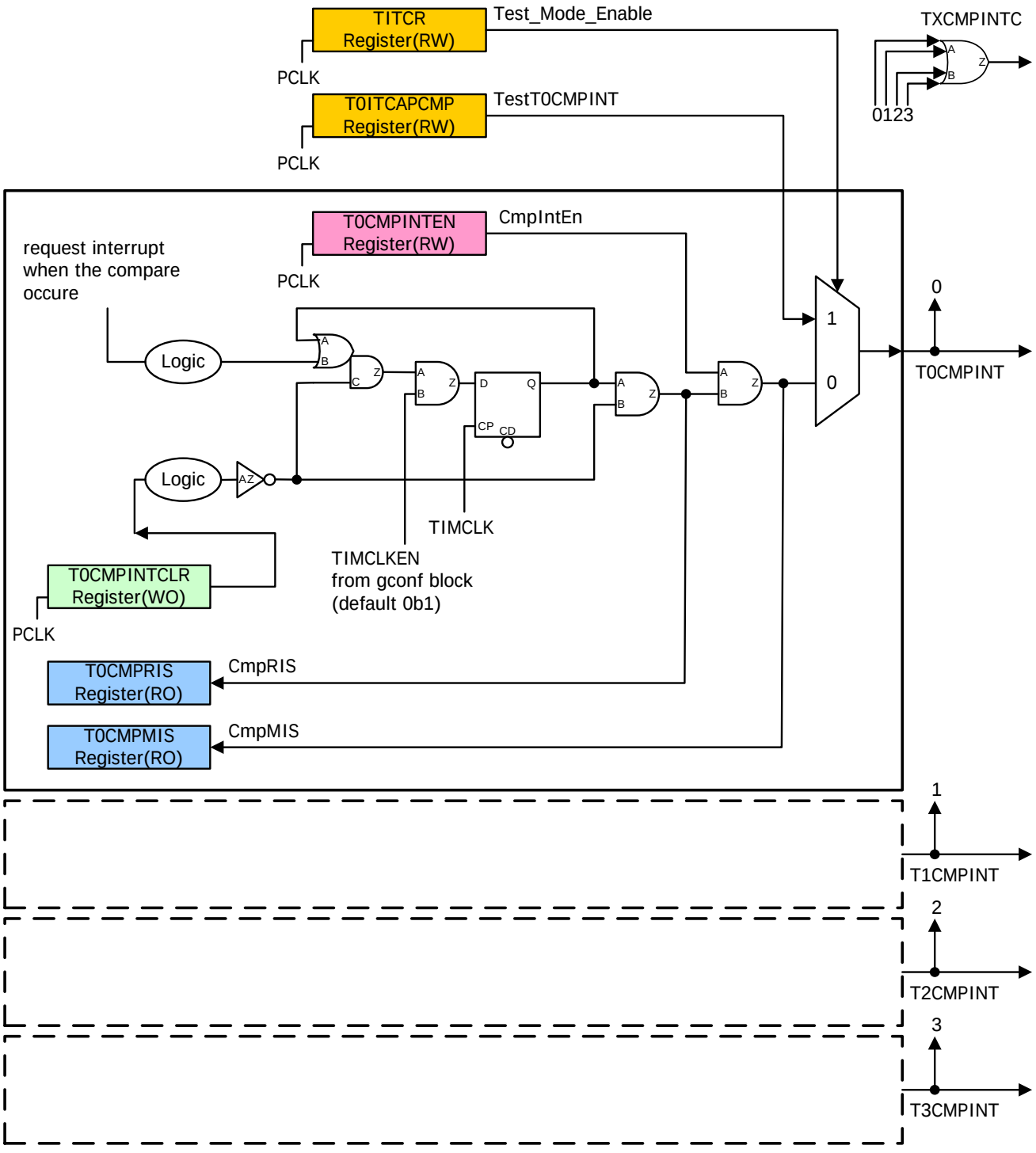

Figure 5.30 Outline diagram of comparison interrupt generator

5.10. Power management

The power modes of the TZ1000 are shown in the following table.

Table 5.6 Power mode and operation

Power mode	State of ADVTMR
ACTIVE	Run (Note)
SLEEP0	Run (Note)
SLEEP1	Run (Note)
SLEEP2	Clock gating
WAIT	Clock gating
RETENTION	Retention
RTC	Power Down
STOP	Power Down

Note: The clock can be started or stopped by software.

- ACTIVE/SLEEP0/SLEEP1:
  Normal operation.
  When the clock stop is set by software, the counter stops and every signal holds its own data. So, if an interrupt, a DMA request, the PWM output, and so on are asserted, they cannot be deasserted because of no clock operation. To prevent that, the clock should be stopped after the interrupt disable, the DMA disable, the PWM output disable, and so on are set. When the clock start is set, the count re-starts with the same state where the clock stopped.
- SLEEP2/WAIT/ RETENTION:
  Both **PCLK** and **TnTIMCLK** (**n** is a channel number: 0, 1, 2, and 3) stop, so the counter also stops and every signal holds its own data. If the interrupt and others are asserted, they will not be able to be deasserted. It is necessary to set the disable to them before the clock stop.
  When returning from this mode, every signal is restored to the data in the previous mode.
- RTC/STOP:
  Before the transition to this mode, it should be checked that each corresponding function is disabled.
  When returning from this mode, the registers are initialized. So, the operation should re-start after the configuration of the registers completes.

5.11. Start-up and Stop Procedure

5.11.1. Start-up Procedure

The start-up procedure after power-on is as follows.

For detail of the PMU (Power Management Unit) registers, refer to the PMU section.

The following setting is supposed that the main bus (the bus connected to the CPU) and the gconf are supplied with clocks.

Each channel of the timer will be supplied with a clock by this setting.

(ch0: channel 0, ch1: channel 1, ch2: channel 2, and ch3: channel 3)

("*" shows the signal which also controls another function. The setting should be done together with another setting.)

The order of the setting procedure is a frequency setting at first, then clock supply, and reset deassertion at last.

- ADVTMR clock frequency setting

PMU register	Bit name	Description
CSM_MAIN	CSMSEL_MAIN	0000000u u: 0: SiOSC4M, 1: OSC12M, 2: PLL, 3: ADPLL, 4: OSC32K/SIOSC32K 5 to 7: reserved
PRESCAL_MAIN	PSSEL_CD_PPIER0	****u*** u: 0: not generate clock 1: divided by 1, 2: divided by 2, 3: divided by 3, 4: divided by 4, 5: divided by 5, 6: divided by 6, 7: divided by 7, 8: divided by 8, 9: divided by 9, A: divided by 10, B: divided by 12, C: divided by 18, D: divided by 24, E: divided by 36, F: divided by 48

Note: CSM_MAIN sets the source of the clock. The PLL is set by another register and the frequency is changed by the setting. (For detail, refer to the PMU section.)

Note: PRESCAL_MAIN has a setting to another power domain.

Note: PSSEL_CD_PPIER0 setting specifies all circuits in the PPIER0 power domain.

Note: The clock frequency setting can be changed even if the counter is operating. In this case, note that the period count is also changed.

The start-up sequence of the ADVTMR is as follows.

Setting of the external shared pins at first, then release of the standby for the external pins, Clock supply, and de-assertion of the reset at last.

- Setting of the external shared pins of the ADVTMR
  It is necessary that the GCONF should configure the shared pins to input or output data. (For detail, refer to the GCONF section.)

- Standby mode release of the external pins in the ADVTMR
  When the external pins are used, it is necessary to release the standby mode of the pins. (For detail, refer to the PMU section.)

- ADVTMR bus clock supply

PMU register	Bit name	value
CG_OFF_POWERDOMAIN	CG_PM	0x00000001
CG_OFF_PM_1	CG_ppier0clk_advtmr_pclk	0x00000083
	CG_mpierclk_h2hp0_hclk	
	CG_ppier0clk_h2pp0_hclk	

Note: Bit 7 in the CG_OFF_PM_1 register corresponds to the ADVTMR bus clock.

The following shows the case that each channel is supplied with a clock separately. If all channels are supplied with a clock, the following values are written serially to the CG_OFF_PM_1 register or the ORed value of all values is written to the CG_OFF_PM_1 register.

- Clock supply to the ADVTMR ch0 counter

PMU register	Bit name	value
CG_OFF_PM_1	CG_ppier0clk_advtmr_ch0_timclk	0x00000200

Note: Bit 9 in CG_OFF_PM_1 register corresponds to the ADVTMR ch0.

- Clock supply to the ADVTMR ch1 counter

PMU register	Bit name	value
CG_OFF_PM_1	CG_ppier0clk_advtmr_ch1_timclk	0x00000800

Note: Bit 11 in CG_OFF_PM_1 register corresponds to the ADVTMR ch1.

- Clock supply to the ADVTMR ch2 counter

PMU register	Bit name	value
CG_OFF_PM_1	CG_ppier0clk_advtmr_ch2_timclk	0x00002000

Note: Bit 13 in CG_OFF_PM_1 register corresponds to the ADVTMR ch2.

- Clock supply to the ADVTMR ch3 counter

PMU register	Bit name	value
CG_OFF_PM_1	CG_ppier0clk_advtmr_ch3_timclk	0x00008000

Note: Bit 15 in CG_OFF_PM_1 register corresponds to the ADVTMR ch3.

- Reset deassertion to the ADVTMR

PMU register	Bit name	value
SRST_OFF_POWERDOMAIN	SRST_PM	0x00000001
SRST_OFF_PM_1	SRST_asyncrst_advtmr_prstn	0x00000083
	SRST_asyncrst_h2pp0_hrstn	
	SRST_asyncrst_h2hp0_hrstn	

Note: Bit 7 in SRST_OFF_PM_1 register corresponds to the ADVTMR.

- Setting of the ADVTMR and operation start
  - When the reset is deasserted, the ADVTMR is in the disable state.
    It starts to operate by writing to the following registers.
  - The period count is set to the load register *[ADVTMR_TnLOAD]*.
  - The operation mode of the ADVTMR (One-shot, Constant period and so on) is set to the control register *[ADVTMR_TnCONTROL]*.
  - Set Enable=1 in the control register *[ADVTMR_TnCONTROL]*.
    (**n** is a channel number: 0, 1, 2, or 3.)

5.11.2. Stop procedure

- In the case of that the ADVTMR counter is stopped;
  The following two ways are used.
  - The ADVTMR is disabled.
    - Set Enable=0 in the control register *[ADVTMR_TnCONTROL]*.
      The counter stops.
  - The period count is set to 0.
    - Set 0000 to the load register *[ADVTMR_TnLOAD]*.
      The prescaler stops, which eventually stops the counter.
- In the case that the controller is not used (the whole block stops);
  The following two ways are used.
  - No reset assertion
    - Only the clock supply is stopped by the following PMU register setting.
  - Reset assertion
    - The reset assertion and the clock stop are set by the following PMU register.

- ADVTMR reset

PMU register	Bit name	value
SRST_ON_PM_1	SRST_asyncrst_advtmr_prstn	0x000000080

Note: The reset is asserted to all channels in the ADVTMR.
It is not possible to assert the reset to the channel separately.

The following shows the case that a clock of each channel is stopped separately. If all channel clocks are stopped, the following values are written serially to the CG_OFF_PM_1 register or the ORed value of all values is written to the CG_OFF_PM_1 register.

- Clock stop for the ADVTMR ch0 counter

PMU register	Bit name	value
CG_ON_PM_1	CG_ppier0clk_advtmr_ch0_timclk	0x00000200

Note: Bit 9 in CG_OFF_PM_1 register corresponds to the ADVTMR ch0.

- Clock stop for the ADVTMR ch1 counter

PMU register	Bit name	value
CG_ON_PM_1	CG_ppier0clk_advtmr_ch1_timclk	0x00000800

Note: Bit 11 in CG_OFF_PM_1 register corresponds to the ADVTMR ch1.

- Clock stop for the ADVTMR ch2 counter

PMU register	Bit name	value
CG_ON_PM_1	CG_ppier0clk_advtmr_ch2_timclk	0x00002000

Note: Bit 13 in CG_OFF_PM_1 register corresponds to the ADVTMR ch2.

- Clock stop for the ADVTMR ch3 counter

PMU register	Bit name	value
CG_ON_PM_1	CG_ppier0clk_advtmr_ch3_timclk	0x00008000

Note: Bit 15 in CG_OFF_PM_1 register corresponds to the ADVTMR ch3.

- Clock stop for the bus of the ADVTMR

PMU register	Bit name	value
CG_ON_PM_1	CG_ppier0clk_advtmr_pclk	0x00000080

Note: Bit 7 in the CG_ON_PM_1 register corresponds to the ADVTMR bus clock.

5.12. Dynamic Clock Gating Setting Procedure

The TZ1000 series can be set to stop the clock supply unless the clock is necessary. When it is set, the following operation reduces the power dissipation.

("*" shows the signal which also controls another function. The setting should be done together with another setting.)

- Clock supply only when the bus access to the ADVTMR.
- Clock supply stop for the counter when the ADVTMR is disabled (Enable=0 in the control register *[ADVTMR_TnCONTROL]*).

- ADVTMR dynamic clock gating setting

PMU register	Bit name	value
DCG_POWERDOMAIN	DCG_PM	0x*******1
DCG_PM_0	DCG_mpierclk_mpier_hclk	0x*******1
DCG_PM_1	DCG_ppier0clk_tmr_ch3_timclk	0x****AA83
	DCG_ppier0clk_tmr_ch2_timclk	
	DCG_ppier0clk_tmr_ch1_timclk	
	DCG_ppier0clk_tmr_ch0_timclk	
	DCG_ppier0clk_tmr_pclk	
	DCG_ppier0clk_h2pp0_hclk	
	DCG_mpierclk_h2hp0_hclk	

This setting is applied to all channel of the ADVTMR. If the setting is done to each bit separately, the assigned bit should be set to 1.

DCG_PM_1 register: bit15 ADVTMR ch3
DCG_PM_1 register: bit13 ADVTMR ch2
DCG_PM_1 register: bit11 ADVTMR ch1
DCG_PM_1 register: bit9 ADVTMR ch0
DCG_PM_1 register: bit7 ADVTMR bus clock

The setting of the dynamic clock gating can be cleared by writing 0 to the corresponding bit.

- ADVTMR dynamic clock gating clear

PMU register	Bit name	value
DCG_PM_1	DCG_ppier0clk_tmr_ch3_timclk	0x****0003
	DCG_ppier0clk_tmr_ch2_timclk	
	DCG_ppier0clk_tmr_ch1_timclk	
	DCG_ppier0clk_tmr_ch0_timclk	
	DCG_ppier0clk_tmr_pclk	

6. Details of Registers

6.1. ADVTMR_T0LOAD

ADVTMR_T0LOAD				
Description	T0 Load Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 0000			
Physical address View0	0x4004 1000			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:16	Reserved	-	-	-
15:0	Load	Initial or reload value of the counter (0x0001 to 0xFFFF settable) The 0x0000 setting does not operate the counter. Setting any numeric value other than that enables counting. (Note) Writing to this register writes the same value to Timer0BGLoad.	RW modify	0x0000

6.2. ADVTMR_T0VALUE

ADVTMR_T0VALUE				
Description	T0 Current value Register			
Address Region	advtmr	**Type:**	RO	
Offset	0x0000 0004			
Physical address View0	0x4004 1004			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:16	Reserved	-	-	-
15:0	value	Count value of the counter at the current time	RO	0xFFFF

6.3. ADVTMR_T0CONTROL

ADVTMR_T0CONTROL				
Description	T0 Control Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 0008			
Physical address View0	0x4004 1008			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:10	Reserved	-	-	-
9:8	Event_Mode	Event counter operation control 11: Event timer (event timer) count source: External terminal T0EVCNTSRC 10: Event timer (event timer) count	RW modify	0x0

		source: Internal prescaler 0*: Normal timer (normal timer)		
7	Enable	Timer operation control 1: Enable 0: Disable	RW modify	0
6	Interrupt_Enable	Interrupt control 1: Interrupt enable 0: Interrupt disable	RW modify	0
5	Periodic_Mode	Timer operation mode 1: Periodic timer (periodic timer) 0: Free-run timer (free-run timer)	RW modify	0
4	One_Shot_Count	Timer wrapping/one-shot selection 1: One-shot (one time only) 0: Wrapping (wrapping)	RW modify	0
3	Timer_size	Timer bit width selection 1: Operation as a 16-bit timer 0: Operation as an 8-bit timer (high-order bits not used)	RW modify	1
2:0	Clock_divid	Prescaler (clock frequency division) 111: 1/1024 frequency division 110: 1/512 frequency division 101: 1/128 frequency division 100: 1/32 frequency division 011: 1/8 frequency division 010: 1/4 frequency division 001: 1/2 frequency division 000: No frequency division (same magnification)	RW modify	0x0

6.4. ADVTMR_T0INTCLR

ADVTMR_T0INTCLR			
Description	T0 Interrupt clear Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 000C		
Physical address View0	0x4004 100C		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	IntClr	Interrupt clear After the T0TIMINT interrupt occurs, it can be cleared by write access to this register.	RW clear	-

6.5. ADVTMR_T0RIS

ADVTMR_T0RIS				
Description	T0 Raw Interrupt Status Register			
Address Region	advtmr	**Type:**	RO	
Offset	0x0000 0010			
Physical address View0	0x4004 1010			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	RIS	A timer interrupt before masking (T0TIMINT) is occurring. (The interrupt occurs when the counter becomes 0x0000.) 1: Interrupt request available 0: No interrupt request	RO	0

6.6. ADVTMR_T0MIS

ADVTMR_T0MIS				
Description	T0 Masked Interrupt Status Register			
Address Region	advtmr	**Type:**	RO	
Offset	0x0000 0014			
Physical address View0	0x4004 1014			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	MIS	A timer interrupt after masking (T0TIMINT) is occurring. 1: Interrupt request available 0: No interrupt request	RO	0

6.7. ADVTMR_T0BGLOAD

ADVTMR_T0BGLOAD				
Description	T0 BackGround Load Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 0018			
Physical address View0	0x4004 1018			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:16	Reserved	-	-	-
15:0	BGLoad	Background Load register A count value set in this register is reloaded after the counter becomes 0x0000 (terminal count). The count value to be reloaded can be	RW modify	0x0000

		changed safely during counting. (Note) Writing to this register does not allow writing to Timer0Load.		

6.8. ADVTMR_T0INTCNT

ADVTMR_T0INTCNT				
Description	T0 Interrupt Count Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 001C			
Physical address View0	0x4004 101C			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	IntCount	Count value for the number of times it became a terminal count of the counter main body. <At read> A count value for the number of times it became a terminal count can be read. <At write> A counter value of Timer0IntCnt can be made to become 0x00 by write access to this register with regard to the timer interrupt generation counter. This register is not cleared by write access of Timer0IntClr. It is not affected by the Timer0Control: Interrupt Enable bit.	RW clear	0x00

6.9. ADVTMR_T0CAPTURE

ADVTMR_T0CAPTURE				
Description	T0 Capture value Register			
Address Region	advtmr	**Type:**	RO	
Offset	0x0000 0020			
Physical address View0	0x4004 1020			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:16	Reserved	-	-	-
15:0	CapReg	Stores a count value when the T0CAPREQ signal is input. If the T0CAPREQ[x] signal is input during capture data reading, the count value is immediately stored after capture data reading ends.	RO	0x0000

6.10. ADVTMR_T0CAPINTCLR

ADVTMR_T0CAPINTCLR			
Description	T0 Capture Interrupt clear Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0040		
Physical address View0	0x4004 1040		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:0	CapIntClr	After a capture interrupt (T0CAPINT[x]) occurs, it can be cleared by write access to this register.	RW clear	-

6.11. ADVTMR_T0CAPRIS

ADVTMR_T0CAPRIS			
Description	T0 Capture Raw Interrupt Status Register		
Address Region	advtmr	**Type:**	RO
Offset	0x0000 0060		
Physical address View0	0x4004 1060		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:1	Reserved	-	-	-
0	CapRIS	A capture interrupt before masking (T0CAPINT[x]) is occurring. 1: Interrupt request available 0: No interrupt request	RO	0

6.12. ADVTMR_T0CAPMIS

ADVTMR_T0CAPMIS			
Description	T0 Capture Masked Interrupt Status Register		
Address Region	advtmr	**Type:**	RO
Offset	0x0000 0064		
Physical address View0	0x4004 1064		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:1	Reserved	-	-	-
0	CapMIS	A capture interrupt after masking (T0CAPINTx) is occurring. 1: Interrupt request available 0: No interrupt request	RO	0

6.13. ADVTMR_T0CAPINTEN

ADVTMR_T0CAPINTEN			
Description	T0 Capture Interrupt Enable Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0068		
Physical address View0	0x4004 1068		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CapIntEn	Capture operation interrupt control 1: Interrupt enable 0: Interrupt disable	RW modify	0

6.14. ADVTMR_T0CAPEN

ADVTMR_T0CAPEN			
Description	T0 Capture Enable Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 006C		
Physical address View0	0x4004 106C		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CapEn	Capture operation control 1: Capture enable 0: Capture disable	RW modify	0

6.15. ADVTMR_T0CAPRELOAD

ADVTMR_T0CAPRELOAD			
Description	T0 Capture Reload Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0074		
Physical address View0	0x4004 1074		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CapReload	Capture operation reload control. A counter value is reloaded to Timer0Load (Timer0BGLoad) due to capture generation. 1: Reloads the counter value upon capture generation. 0: Does not reload the counter value upon capture generation.	RW modify	0

6.16. ADVTMR_T0CAPCTRL

ADVTMR_T0CAPCTRL			
Description	T0 Capture Control Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0078		
Physical address View0	0x4004 1078		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:2	Reserved	-	-	-
1:0	CapCtrl0	Selection of capture input operation 11: Capture operation at both the rising and falling edges 10: Capture operation at the falling edge 01: Capture operation at the rising edge 00: Capture operation with pulse input	RW modify	0x0

6.17. ADVTMR_T0CAPSYNC

ADVTMR_T0CAPSYNC			
Description	T0 Capture Synchronization Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 007C		
Physical address View0	0x4004 107C		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:1	Reserved	-	-	-
0	CapSync	Capture input synchronization control 1: Synchronizes capture input (for external input with clock not synchronized) 0: Does not synchronize capture input (for external input with clock synchronized)	RW modify	0

6.18. ADVTMR_T0BGCOMPARE

ADVTMR_T0BGCOMPARE			
Description	T0 BackGround Compare Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0080		
Physical address View0	0x4004 1080		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:16	BGLoad	Background load register This register is the same as the 0x018 register. However, it is write-only. It is set in this area for DMA transfer. It can	RW modify	0x0000

		be accessed only for TCDMASelx=1. (Note) This register appears on the memory map only for TCDMASelx=1. (Note) This register can be accessed from either of the CPU and DMAC. (Note) If this register is accessed in halfword units, a wrong value is written to a register not accessed. So, only access in word units is permitted.		
15:0	BGCompare	Background compare register that stores a compare value to be compared with a count value A count value set in this register is reloaded after the counter becomes 0 (terminal count). The count value to be reloaded can be changed safely during counting. (Note) Writing to this register does not allow writing to Timer0Compare.	RW modify	0x0000

6.19. ADVTMR_T0COMPARE

ADVTMR_T0COMPARE			
Description	T0 Compare value Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 00A0		
Physical address View0	0x4004 10A0		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:16	Reserved	-	-	-
15:0	CmpReg	Stores a compare value to be compared with a count value. (Note) This register cannot be read immediately after writing to it because a transfer to other clocks (PCLK->TIMCLK) is required. Reading after writing is required for up to one cycle of TIMCLK. (Note) Writing to the Timer0Compare register writes the same value to Timer0BGCompare.	RW modify	0x0000

6.20. ADVTMR_T0CMPINTCLR

ADVTMR_T0CMPINTCLR			
Description	T0 Compare Interrupt clear Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 00C0		
Physical address View0	0x4004 10C0		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	CmpIntClr	After a compare interrupt occurs, it can be cleared by write access to this register.	RW clear	-

6.21. ADVTMR_T0CMPRIS

ADVTMR_T0CMPRIS			
Description	T0 Compare Raw Interrupt Status Register		
Address Region	advtmr	**Type:**	RO
Offset	0x0000 00E0		
Physical address View0	0x4004 10E0		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CmpRIS	A compare interrupt before masking (T0CMPINTx) is occurring. 1: Interrupt request available 0: No interrupt request	RO	0

6.22. ADVTMR_T0CMPMIS

ADVTMR_T0CMPMIS			
Description	T0 Compare Masked Interrupt Status Register		
Address Region	advtmr	**Type:**	RO
Offset	0x0000 00E4		
Physical address View0	0x4004 10E4		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CmpMIS	A compare interrupt after masking (T0CMPINT) is occurring. 1: Interrupt request available 0: No interrupt request	RO	0

6.23. ADVTMR_T0CMPINTEN

ADVTMR_T0CMPINTEN			
Description	T0 Compare Interrupt Enable Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 00E8		
Physical address View0	0x4004 10E8		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CmpIntEn	Compare operation interrupt control 1: Interrupt enable 0: Interrupt disable	RW modify	0

6.24. ADVTMR_T0CMPEN

ADVTMR_T0CMPEN			
Description	T0 Compare Enable Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 00EC		
Physical address View0	0x4004 10EC		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CmpEn	Compare operation control 1: Compare enable 0: Compare disable	RW modify	0

6.25. ADVTMR_T1LOAD

ADVTMR_T1LOAD			
Description	T1 Load Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0100		
Physical address View0	0x4004 1100		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:16	Reserved	-	-	-
15:0	Load	Initial or reload value of the counter (0x0001 to 0xFFFF settable)	RW modify	0x0000

6.26. ADVTMR_T1VALUE

ADVTMR_T1VALUE				
Description	T1 Current value Register			
Address Region	advtmr	**Type:**	RO	
Offset	0x0000 0104			
Physical address View0	0x4004 1104			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:16	Reserved	-	-	-
15:0	value	Count value of the counter at the current time	RO	0xFFFF

6.27. ADVTMR_T1CONTROL

ADVTMR_T1CONTROL				
Description	T1 Control Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 0108			
Physical address View0	0x4004 1108			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:10	Reserved	-	-	-
9:8	Event_Mode	Event counter operation control	RW modify	0x0
7	Enable	Timer operation control	RW modify	0
6	Interrupt_Enable	Interrupt control	RW modify	0
5	Periodic_Mode	Timer operation mode	RW modify	0
4	One_Shot_Count	Selection of timer wrapping and one-shot	RW modify	0
3	Timer_size	Selection of timer bit width	RW modify	1
2:0	Clock_divid	Prescaler (clock frequency division)	RW modify	0x0

6.28. ADVTMR_T1INTCLR

ADVTMR_T1INTCLR				
Description	T1 Interrupt clear Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 010C			
Physical address View0	0x4004 110C			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	IntClr	Interrupt clear	RW clear	-

6.29. ADVTMR_T1RIS

ADVTMR_T1RIS				
Description	T1 Raw Interrupt Status Register			
Address Region	advtmr	**Type:**	RO	
Offset	0x0000 0110			
Physical address View0	0x4004 1110			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	RIS	A timer interrupt before masking (T1TIMINT) is occurring. (The interrupt occurs when the counter becomes 0x0000.)	RO	0

6.30. ADVTMR_T1MIS

ADVTMR_T1MIS				
Description	T1 Masked Interrupt Status Register			
Address Region	advtmr	**Type:**	RO	
Offset	0x0000 0114			
Physical address View0	0x4004 1114			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	MIS	A timer interrupt after masking (T1TIMINT) is occurring.	RO	0

6.31. ADVTMR_T1BGLOAD

ADVTMR_T1BGLOAD			
Description	T1 BackGround Load Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0118		
Physical address View0	0x4004 1118		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:16	Reserved	-	-	-
15:0	BGLoad	Background Load register	RW modify	0x0000

6.32. ADVTMR_T1INTCNT

ADVTMR_T1INTCNT			
Description	T1 Interrupt Count Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 011C		
Physical address View0	0x4004 111C		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	IntCount	Count value for the number of times it became a terminal count of the counter main body	RW modify	0x00

6.33. ADVTMR_T1CAPTURE

ADVTMR_T1CAPTURE			
Description	T1 Capture value Register		
Address Region	advtmr	**Type:**	RO
Offset	0x0000 0120		
Physical address View0	0x4004 1120		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:16	Reserved	-	-	-
15:0	CapReg	Stores a count value when the T1CAPREQ signal is input.	RO	0x0000

6.34. ADVTMR_T1CAPINTCLR

ADVTMR_T1CAPINTCLR			
Description	T1 Capture Interrupt clear Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0140		
Physical address View0	0x4004 1140		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	CapIntClr	After a capture interrupt occurs, it can be cleared by write access to this register.	RW clear	-

6.35. ADVTMR_T1CAPRIS

ADVTMR_T1CAPRIS			
Description	T1 Capture Raw Interrupt Status Register		
Address Region	advtmr	**Type:**	RO
Offset	0x0000 0160		
Physical address View0	0x4004 1160		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CapRIS	A capture interrupt before masking (T1CAPINT[x]) is occurring.	RO	0

6.36. ADVTMR_T1CAPMIS

ADVTMR_T1CAPMIS			
Description	T1 Capture Masked Interrupt Status Register		
Address Region	advtmr	**Type:**	RO
Offset	0x0000 0164		
Physical address View0	0x4004 1164		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CapMIS	A capture interrupt after masking (T1CAPINTx) is occurring.	RO	0

6.37. ADVTMR_T1CAPINTEN

ADVTMR_T1CAPINTEN				
Description	T1 Capture Interrupt Enable Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 0168			
Physical address View0	0x4004 1168			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CapIntEn	Capture operation interrupt control	RW modify	0

6.38. ADVTMR_T1CAPEN

ADVTMR_T1CAPEN				
Description	T1 Capture Enable Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 016C			
Physical address View0	0x4004 116C			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CapEn	Capture operation control	RW modify	0

6.39. ADVTMR_T1CAPRELOAD

ADVTMR_T1CAPRELOAD				
Description	T1 Capture Reload Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 0174			
Physical address View0	0x4004 1174			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CapReload	Capture operation reload control. A counter value is reloaded to Timer1Load (Timer1BGLoad) due to capture generation.	RW modify	0

6.40. ADVTMR_T1CAPCTRL

ADVTMR_T1CAPCTRL				
Description	T1 Capture Control Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 0178			
Physical address View0	0x4004 1178			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:2	Reserved	-	-	-
1:0	CapCtrl0	Capture input operation selection	RW modify	0x0

6.41. ADVTMR_T1CAPSYNC

ADVTMR_T1CAPSYNC				
Description	T1 Capture Synchronization Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 017C			
Physical address View0	0x4004 117C			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CapSync	Capture input synchronization control	RW modify	0

6.42. ADVTMR_T1BGCOMPARE

ADVTMR_T1BGCOMPARE				
Description	T1 BackGround Compare Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 0180			
Physical address View0	0x4004 1180			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:16	BGLoad	Background Load register	RW modify	0x0000
15:0	BGCompare	Background compare register. Stores a compare value to be compared with a count value.	RW modify	0x0000

6.43. ADVTMR_T1COMPARE

ADVTMR_T1COMPARE			
Description	T1 Compare value Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 01A0		
Physical address View0	0x4004 11A0		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:16	Reserved	-	-	-
15:0	CmpReg	Stores a compare value to be compared with a count value.	RW modify	0x0000

6.44. ADVTMR_T1CMPINTCLR

ADVTMR_T1CMPINTCLR			
Description	T1 Compare Interrupt clear Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 01C0		
Physical address View0	0x4004 11C0		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	CmpIntClr	After a compare interrupt occurs, it can be cleared by write access to this register.	RW clear	-

6.45. ADVTMR_T1CMPRIS

ADVTMR_T1CMPRIS			
Description	T1 Compare Raw Interrupt Status Register		
Address Region	advtmr	**Type:**	RO
Offset	0x0000 01E0		
Physical address View0	0x4004 11E0		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CmpRIS	A compare interrupt before masking (T1CMPINTx) is occurring.	RO	0

6.46. ADVTMR_T1CMPMIS

ADVTMR_T1CMPMIS				
Description	T1 Compare Masked Interrupt Status Register			
Address Region	advtmr	**Type:**	RO	
Offset	0x0000 01E4			
Physical address View0	0x4004 11E4			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CmpMIS	A compare interrupt before masking (T1CMPINT) is occurring.	RO	0

6.47. ADVTMR_T1CMPINTEN

ADVTMR_T1CMPINTEN				
Description	T1 Compare Interrupt Enable Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 01E8			
Physical address View0	0x4004 11E8			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CmpIntEn	Compare operation interrupt control	RW modify	0

6.48. ADVTMR_T1CMPEN

ADVTMR_T1CMPEN				
Description	T1 Compare Enable Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 01EC			
Physical address View0	0x4004 11EC			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CmpEn	Compare operation control	RW modify	0

6.49. ADVTMR_T2LOAD

ADVTMR_T2LOAD			
Description	T2 Load Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0200		
Physical address View0	0x4004 1200		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:16	Reserved	-	-	-
15:0	Load	Initial or reload value of the counter (0x0001 to 0xFFFF settable)	RW modify	0x0000

6.50. ADVTMR_T2VALUE

ADVTMR_T2VALUE			
Description	T2 Current value Register		
Address Region	advtmr	**Type:**	RO
Offset	0x0000 0204		
Physical address View0	0x4004 1204		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:16	Reserved	-	-	-
15:0	value	Count value of the counter at the current time	RO	0xFFFF

6.51. ADVTMR_T2CONTROL

ADVTMR_T2CONTROL			
Description	T2 Control Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0208		
Physical address View0	0x4004 1208		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:10	Reserved	-	-	-
9:8	Event_Mode	Event counter operation control	RW modify	0x0
7	Enable	Timer operation control	RW modify	0
6	Interrupt_Enable	Interrupt control	RW modify	0
5	Periodic_Mode	Timer operation mode	RW modify	0
4	One_Shot_Count	Selection of timer wrapping and one-shot	RW modify	0

3	Timer_size	Selection of timer bit width	RW modify	1
2:0	Clock_divid	Prescaler (clock frequency division)	RW modify	0x0

6.52. ADVTMR_T2INTCLR

ADVTMR_T2INTCLR				
Description	T2 Interrupt clear Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 020C			
Physical address View0	0x4004 120C			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	IntClr	Interrupt clear	RW clear	-

6.53. ADVTMR_T2RIS

ADVTMR_T2RIS				
Description	T2 Raw Interrupt Status Register			
Address Region	advtmr	**Type:**	RO	
Offset	0x0000 0210			
Physical address View0	0x4004 1210			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	RIS	A timer interrupt before masking (T2TIMINT) is occurring. (The interrupt occurs when the counter becomes 0x0000.)	RO	0

6.54. ADVTMR_T2MIS

ADVTMR_T2MIS				
Description	T2 Masked Interrupt Status Register			
Address Region	advtmr	**Type:**	RO	
Offset	0x0000 0214			
Physical address View0	0x4004 1214			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	MIS	A timer interrupt after masking (T2TIMINT) is occurring.	RO	0

6.55. ADVTMR_T2BGLOAD

ADVTMR_T2BGLOAD				
Description	T2 BackGround Load Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 0218			
Physical address View0	0x4004 1218			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:16	Reserved	-	-	-
15:0	BGLoad	Background Load register	RW modify	0x0000

6.56. ADVTMR_T2INTCNT

ADVTMR_T2INTCNT				
Description	T2 Interrupt Count Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 021C			
Physical address View0	0x4004 121C			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	IntCount	Count value for the number of times it became a terminal count of the counter main body	RW modify	0x00

6.57. ADVTMR_T2CAPTURE

ADVTMR_T2CAPTURE				
Description	T2 Capture value Register			
Address Region	advtmr	**Type:**	RO	
Offset	0x0000 0220			
Physical address View0	0x4004 1220			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:16	Reserved	-	-	-
15:0	CapReg	Stores a count value when the T2CAPREQ signal is input.	RO	0x0000

6.58. ADVTMR_T2CAPINTCLR

ADVTMR_T2CAPINTCLR			
Description	T2 Capture Interrupt clear Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0240		
Physical address View0	0x4004 1240		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	CapIntClr	After a capture interrupt occurs, it can be cleared by write access to this register.	RW clear	-

6.59. ADVTMR_T2CAPRIS

ADVTMR_T2CAPRIS			
Description	T2 Capture Raw Interrupt Status Register		
Address Region	advtmr	**Type:**	RO
Offset	0x0000 0260		
Physical address View0	0x4004 1260		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CapRIS	A capture interrupt before masking (T2CAPINT[x]) is occurring.	RO	0

6.60. ADVTMR_T2CAPMIS

ADVTMR_T2CAPMIS			
Description	T2 Capture Masked Interrupt Status Register		
Address Region	advtmr	**Type:**	RO
Offset	0x0000 0264		
Physical address View0	0x4004 1264		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CapMIS	A capture interrupt after masking (T2CAPINTx) is occurring.	RO	0

6.61. ADVTMR_T2CAPINTEN

ADVTMR_T2CAPINTEN				
Description	T2 Capture Interrupt Enable Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 0268			
Physical address View0	0x4004 1268			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CapIntEn	Capture operation interrupt control	RW modify	0

6.62. ADVTMR_T2CAPEN

ADVTMR_T2CAPEN				
Description	T2 Capture Enable Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 026C			
Physical address View0	0x4004 126C			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CapEn	Capture operation control	RW modify	0

6.63. ADVTMR_T2CAPRELOAD

ADVTMR_T2CAPRELOAD				
Description	T2 Capture Reload Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 0274			
Physical address View0	0x4004 1274			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CapReload	Capture operation reload control. A counter value is reloaded to Timer2Load (Timer2BGLoad) due to capture generation.	RW modify	0

6.64. ADVTMR_T2CAPCTRL

ADVTMR_T2CAPCTRL			
Description	T2 Capture Control Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0278		
Physical address View0	0x4004 1278		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:2	Reserved	-	-	-
1:0	CapCtrl0	Capture input operation selection	RW modify	0x0

6.65. ADVTMR_T2CAPSYNC

ADVTMR_T2CAPSYNC			
Description	T2 Capture Synchronization Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 027C		
Physical address View0	0x4004 127C		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CapSync	Capture input synchronization control	RW modify	0

6.66. ADVTMR_T2BGCOMPARE

ADVTMR_T2BGCOMPARE			
Description	T2 BackGround Compare Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0280		
Physical address View0	0x4004 1280		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:16	BGLoad	Background Load register	RW modify	0x0000
15:0	BGCompare	Background compare register. Stores a compare value to be compared with a count value.	RW modify	0x0000

6.67. ADVTMR_T2COMPARE

ADVTMR_T2COMPARE			
Description	T2 Compare value Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 02A0		
Physical address View0	0x4004 12A0		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:16	Reserved	-	-	-
15:0	CmpReg	Stores a compare value to be compared with a count value.	RW modify	0x0000

6.68. ADVTMR_T2CMPINTCLR

ADVTMR_T2CMPINTCLR			
Description	T2 Compare Interrupt clear Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 02C0		
Physical address View0	0x4004 12C0		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	CmpIntClr	After a compare interrupt occurs, it can be cleared by write access to this register.	RW clear	-

6.69. ADVTMR_T2CMPRIS

ADVTMR_T2CMPRIS			
Description	T2 Compare Raw Interrupt Status Register		
Address Region	advtmr	**Type:**	RO
Offset	0x0000 02E0		
Physical address View0	0x4004 12E0		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CmpRIS	A compare interrupt before masking (T2CMPINTx) is occurring.	RO	0

6.70. ADVTMR_T2CMPMIS

ADVTMR_T2CMPMIS				
Description	T2 Compare Masked Interrupt Status Register			
Address Region	advtmr	**Type:**	RO	
Offset	0x0000 02E4			
Physical address View0	0x4004 12E4			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CmpMIS	A compare interrupt after masking (T2CMPINT) is occurring.	RO	0

6.71. ADVTMR_T2CMPINTEN

ADVTMR_T2CMPINTEN				
Description	T2 Compare Interrupt Enable Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 02E8			
Physical address View0	0x4004 12E8			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CmpIntEn	Compare operation interrupt control	RW modify	0

6.72. ADVTMR_T2CMPEN

ADVTMR_T2CMPEN				
Description	T2 Compare Enable Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 02EC			
Physical address View0	0x4004 12EC			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CmpEn	Compare operation control	RW modify	0

6.73. ADVTMR_T3LOAD

ADVTMR_T3LOAD			
Description	T3 Load Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0300		
Physical address View0	0x4004 1300		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:16	Reserved	-	-	-
15:0	Load	Initial or reload value of the counter (0x0001 to 0xFFFF settable)	RW modify	0x0000

6.74. ADVTMR_T3VALUE

ADVTMR_T3VALUE			
Description	T3 Current value Register		
Address Region	advtmr	**Type:**	RO
Offset	0x0000 0304		
Physical address View0	0x4004 1304		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:16	Reserved	-	-	-
15:0	value	Count value of the counter at the current time	RO	0xFFFF

6.75. ADVTMR_T3CONTROL

ADVTMR_T3CONTROL			
Description	T3 Control Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0308		
Physical address View0	0x4004 1308		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:10	Reserved	-	-	-
9:8	Event_Mode	Event counter operation control	RW modify	0x0
7	Enable	Timer operation control	RW modify	0
6	Interrupt_Enable	Interrupt control	RW modify	0
5	Periodic_Mode	Timer operation mode	RW modify	0
4	One_Shot_Count	Selection of timer wrapping and one-shot	RW modify	0

3	Timer_size	Selection of timer bit width	RW modify	1
2:0	Clock_divid	Prescaler (clock frequency division)	RW modify	0x0

6.76. ADVTMR_T3INTCLR

ADVTMR_T3INTCLR				
Description	T3 Interrupt clear Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 030C			
Physical address View0	0x4004 130C			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	IntClr	Interrupt clear	RW clear	-

6.77. ADVTMR_T3RIS

ADVTMR_T3RIS				
Description	T3 Raw Interrupt Status Register			
Address Region	advtmr	**Type:**	RO	
Offset	0x0000 0310			
Physical address View0	0x4004 1310			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	RIS	A timer interrupt before masking (T3TIMINT) is occurring. (The interrupt occurs when the counter becomes 0x0000.)	RO	0

6.78. ADVTMR_T3MIS

ADVTMR_T3MIS				
Description	T3 Masked Interrupt Status Register			
Address Region	advtmr	**Type:**	RO	
Offset	0x0000 0314			
Physical address View0	0x4004 1314			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	MIS	A timer interrupt after masking (T3TIMINT) is occurring.	RO	0

6.79. ADVTMR_T3BGLOAD

ADVTMR_T3BGLOAD				
Description	T3 BackGround Load Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 0318			
Physical address View0	0x4004 1318			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:16	Reserved	-	-	-
15:0	BGLoad	Background load register	RW modify	0x0000

6.80. ADVTMR_T3INTCNT

ADVTMR_T3INTCNT				
Description	T3 Interrupt Count Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 031C			
Physical address View0	0x4004 131C			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	IntCount	Count value for the number of times it became a terminal count of the counter main body	RW modify	0x00

6.81. ADVTMR_T3CAPTURE

ADVTMR_T3CAPTURE				
Description	T3 Capture value Register			
Address Region	advtmr	**Type:**	RO	
Offset	0x0000 0320			
Physical address View0	0x4004 1320			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:16	Reserved	-	-	-
15:0	CapReg	Stores a count value when the T3CAPREQ signal is input.	RO	0x0000

6.82. ADVTMR_T3CAPINTCLR

ADVTMR_T3CAPINTCLR				
Description	T3 Capture Interrupt clear Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 0340			
Physical address View0	0x4004 1340			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	CapIntClr	After a capture interrupt occurs, it can be cleared by write access to this register.	RW clear	-

6.83. ADVTMR_T3CAPRIS

ADVTMR_T3CAPRIS				
Description	T3 Capture Raw Interrupt Status Register			
Address Region	advtmr	**Type:**	RO	
Offset	0x0000 0360			
Physical address View0	0x4004 1360			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CapRIS	A capture interrupt before masking (T3CAPINT[x]) is occurring.	RO	0

6.84. ADVTMR_T3CAPMIS

ADVTMR_T3CAPMIS				
Description	T3 Capture Masked Interrupt Status Register			
Address Region	advtmr	**Type:**	RO	
Offset	0x0000 0364			
Physical address View0	0x4004 1364			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CapMIS	A capture interrupt after masking (T3CAPINTx) is occurring.	RO	0

6.85. ADVTMR_T3CAPINTEN

ADVTMR_T3CAPINTEN				
Description	T3 Capture Interrupt Enable Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 0368			
Physical address View0	0x4004 1368			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CapIntEn	Capture operation interrupt control	RW modify	0

6.86. ADVTMR_T3CAPEN

ADVTMR_T3CAPEN				
Description	T3 Capture Enable Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 036C			
Physical address View0	0x4004 136C			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CapEn	Capture operation control	RW modify	0

6.87. ADVTMR_T3CAPRELOAD

ADVTMR_T3CAPRELOAD				
Description	T3 Capture Reload Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 0374			
Physical address View0	0x4004 1374			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CapReload	Capture operation reload control. A counter value is reloaded to Timer3Load (Timer3BGLoad) due to capture generation.	RW modify	0

6.88. ADVTMR_T3CAPCTRL

ADVTMR_T3CAPCTRL				
Description	T3 Capture Control Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 0378			
Physical address View0	0x4004 1378			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:2	Reserved	-	-	-
1:0	CapCtrl0	Capture input operation selection	RW modify	0x0

6.89. ADVTMR_T3CAPSYNC

ADVTMR_T3CAPSYNC				
Description	T3 Capture Synchronization Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 037C			
Physical address View0	0x4004 137C			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CapSync	Capture input synchronization control	RW modify	0

6.90. ADVTMR_T3BGCOMPARE

ADVTMR_T3BGCOMPARE				
Description	T3 BackGround Compare Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 0380			
Physical address View0	0x4004 1380			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:16	BGLoad	Background load register	RW modify	0x0000
15:0	BGCompare	Background compare register. Stores a compare value to be compared with a count value.	RW modify	0x0000

6.91. ADVTMR_T3COMPARE

ADVTMR_T3COMPARE			
Description	T3 Compare value Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 03A0		
Physical address View0	0x4004 13A0		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:16	Reserved	-	-	-
15:0	CmpReg	Stores a compare value to be compared with a count value.	RW modify	0x0000

6.92. ADVTMR_T3CMPINTCLR

ADVTMR_T3CMPINTCLR			
Description	T3 Compare Interrupt clear Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 03C0		
Physical address View0	0x4004 13C0		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	CmpIntClr	After a compare interrupt occurs, it can be cleared by write access to this register.	RW clear	-

6.93. ADVTMR_T3CMPRIS

ADVTMR_T3CMPRIS			
Description	T3 Compare Raw Interrupt Status Register		
Address Region	advtmr	**Type:**	RO
Offset	0x0000 03E0		
Physical address View0	0x4004 13E0		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CmpRIS	A compare interrupt before masking (T3CMPINTx) is occurring.	RO	0

6.94. ADVTMR_T3CMPMIS

ADVTMR_T3CMPMIS				
Description	T3 Compare Masked Interrupt Status Register			
Address Region	advtmr	**Type:**	RO	
Offset	0x0000 03E4			
Physical address View0	0x4004 13E4			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CmpMIS	A compare interrupt after masking (T3CMPINT) is occurring.	RO	0

6.95. ADVTMR_T3CMPINTEN

ADVTMR_T3CMPINTEN				
Description	T3 Compare Interrupt Enable Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 03E8			
Physical address View0	0x4004 13E8			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CmpIntEn	Compare operation interrupt control	RW modify	0

6.96. ADVTMR_T3CMPEN

ADVTMR_T3CMPEN				
Description	T3 Compare Enable Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 03EC			
Physical address View0	0x4004 13EC			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CmpEn	Compare operation control	RW modify	0

6.97. ADVTMR_T0TFFEN

ADVTMR_T0TFFEN			
Description	T0 TFF Enable Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0400		
Physical address View0	0x4004 1400		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:1	Reserved	-	-	-
0	TFFEn	TFF (Toggle Flip-Flop) operation control 1: TFF function enable 0: TFF function disable (TFF output is fixed at 0.)	RW modify	0

6.98. ADVTMR_T0TFFSTAT

ADVTMR_T0TFFSTAT			
Description	T0 TFF Status Register		
Address Region	advtmr	**Type:**	RO
Offset	0x0000 0404		
Physical address View0	0x4004 1404		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:1	Reserved	-	-	-
0	TFFStat	TFF (Toggle Flip-Flop) output status (indicating the status before the last stage of Timer0TFFInv) 1: High TFF output 0: Low TFF output	RO	0

6.99. ADVTMR_T0TFFZERO

ADVTMR_T0TFFZERO			
Description	T0 TFF Zero Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0408		
Physical address View0	0x4004 1408		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:1	Reserved	-	-	-
0	TFFZero	TFF (Toggle Flip-Flop) operation control (to select whether to toggle TFF at a falling edge when the Timer counter is 0) This setting is required for PWM operation.	RW modify	0

		1: Toggle with Compare and Timer counter 0x0000 (terminal count) (the Timer0TFFCtrl setting disabled) 0: Toggle only with Compare (the Timer0TFFCtrl setting enabled)		

6.100. ADVTMR_T0TFFINV

ADVTMR_T0TFFINV			
Description	T0 TFF Invert Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 040C		
Physical address View0	0x4004 140C		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:1	Reserved	-	-	-
0	TFFInv	TFF (Toggle Flip-Flop) operation control (to select whether the output is reversed at its last stage) 1: Reverses the TFF output at its last stage for output. 0: TFF output without reverse.	RW modify	0

6.101. ADVTMR_T0TFFCTRL

ADVTMR_T0TFFCTRL			
Description	T0 TFF Control Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0410		
Physical address View0	0x4004 1410		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:2	Reserved	-	-	-
1:0	TFFCtrl	Selection of TFF (Toggle Flip-Flop) output operation 11: Pulse operation. Compare output becomes TFF output as is. 10: Toggle operation. TFF output is reversed for the relevant Compare output. 01: Operation for becoming "1". No change for TFF=1. 00: Operation for becoming "0". No change for TFF=0.	RW modify	0x3

6.102. ADVTMR_T0TFFINIT

ADVTMR_T0TFFINIT			
Description	T0 TFF Init Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0414		
Physical address View0	0x4004 1414		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	TFFInit	TFF (Toggle Flip-Flop) operation control (selection of output initial value) 1: Sets the initial value of TFF output to 1. 0: Sets the initial value of TFF output to 0.	RW modify	0

6.103. ADVTMR_T0EVCONTROL

ADVTMR_T0EVCONTROL			
Description	T0 Event Control Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0420		
Physical address View0	0x4004 1420		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:6	Reserved	-	-	-
5:4	Event_Select	Event counter operation selection 11: EventEn + external terminal input (edge) 10: EventEn + external terminal input (level) 0*: EventEn bit only	RW modify	0x0
3	EvSync	Selection of event counter input synchronization 1: Synchronized 0: Not synchronized	RW modify	1
2	Reserved	-	-	-
1	EvDelay	Selection of count start delay of the event counter 1: Start delay by 1 TIMCLK 0: No start delay	RW modify	0
0	EventEn	Event counter control 1: Event counter enable 0: Event counter disable	RW modify	0

6.104. ADVTMR_T0EVSEL

ADVTMR_T0EVSEL			
Description	T0 EV Select Control Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0430		
Physical address View0	0x4004 1430		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:7	Reserved	-	-	-
6:4	EVCNTSRC_Sel	EVCNTSRC I/O control Input selection signal: Generation of the output level of the T0EVSRCSEL signals. 111: ADVTMR:T3TFFOUT 110: ADVTMR:T2TFFOUT 101: ADVTMR:T1TFFOUT 100: ADVTMR:T3TIMINT(ch3->ch0 cascade connect) 011: PIN:MCU_I2C0_CLK(Pin share=FMOD2) 010: PIN:MCU_I2C0_DATA(Pin share=FMOD2) 001: PIN:MCU_UA0_TXD(Pin share=FMOD2), PIN:MCU_GPIO_13(Pin share=FMOD3) 000: PIN:MCU_UA0_RXD(Pin share=FMOD2), PIN:MCU_GPIO_12(Pin share=FMOD3)	RW modify	0x0
3	Reserved	-	-	-
2:0	EVCNTEN_Sel	EVCNTEN I/O control Input selection signal: Generation of the output level of the T0EVENSEL signals. 111: ADVTMR:T3TFFOUT 110: ADVTMR:T2TFFOUT 101: ADVTMR:T1TFFOUT 100: ADVTMR:T3TIMINT(ch3->ch0 cascade connect) 011: PIN:MCU_I2C0_CLK(Pin share=FMOD2) 010: PIN:MCU_I2C0_DATA(Pin share=FMOD2) 001: PIN:MCU_UA0_TXD(Pin share=FMOD2), PIN:MCU_GPIO_13(Pin share=FMOD3) 000: PIN:MCU_UA0_RXD(Pin share=FMOD2), PIN:MCU_GPIO_12(Pin share=FMOD3)	RW modify	0x0

6.105. ADVTMR_T0IOSEL

ADVTMR_T0IOSEL			
Description	T0 IO Select Control Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0434		
Physical address View0	0x4004 1434		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	IOSel	T0TFFOUT I/O control 1: T0TFFOUT output 0: Input from external pin or not output	RW modify	0

6.106. ADVTMR_T0CAPSEL

ADVTMR_T0CAPSEL			
Description	T0 Capture Select Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0438		
Physical address View0	0x4004 1438		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:3	Reserved	-	-	-
2:0	CapSel	Capture input selection Input selection signal: Generates the output level of the T0CAPSEL signals. 111: ADVTMR:T3TFFOUT 110: ADVTMR:T2TFFOUT 101: ADVTMR:T1TFFOUT 100: EVM:evm_advtimer_capture[0] 011: PIN:MCU_I2C0_CLK(Pin share=FMOD2) 010: PIN:MCU_I2C0_DATA(Pin share=FMOD2) 001: PIN:MCU_UA0_TXD(Pin share=FMOD2), PIN:MCU_GPIO_13(Pin share=FMOD3) 000: PIN:MCU_UA0_RXD(Pin share=FMOD2), PIN:MCU_GPIO_12(Pin share=FMOD3)	RW modify	0x0

6.107. ADVTMR_T0CAPDMAEN

ADVTMR_T0CAPDMAEN			
Description	T0 CapDMA Enable Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0480		
Physical address View0	0x4004 1480		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:1	Reserved	-	-	-
0	CapDMAEn	T0CAPDMAREQ control 1: CapDMA request enable 0: CapDMA request disable	RW modify	0

6.108. ADVTMR_T0CAPDMASTAT

ADVTMR_T0CAPDMASTAT			
Description	T0 CapDMA Status Register		
Address Region	advtmr	**Type:**	RO
Offset	0x0000 0490		
Physical address View0	0x4004 1490		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:1	Reserved	-	-	-
0	CapDMAStat	CapDMA transfer status After start of DMA transfer, status "1" continues until T0CAPDMACTC arrives. It changes to "0" after T0CAPDMACTC arrives. 1: DMA request in progress 0: No DMA request	RO	0

6.109. ADVTMR_T0CMPDMASTAT

ADVTMR_T0CMPDMASTAT			
Description	T0 CmpDMA Status Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0498		
Physical address View0	0x4004 1498		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:1	Reserved	-	-	-
0	CmpDMAStat	CmpDMA transfer status After start of DMA transfer, status "1" continues until T0CMPDMACTC arrives. It changes to "0" after T0CMPDMACTC	RW modify	0

		arrives. 1: DMA request in progress 0: No DMA request		

6.110. ADVTMR_T0TCDMASEL

ADVTMR_T0TCDMASEL					
Description	T0 Terminal Count DMA Request Select Register				
Address Region	advtmr		**Type:**	RW	
Offset	0x0000 049C				
Physical address View0	0x4004 149C				
Physical address View1	-				
Bitfield Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:1	Reserved	-		-	-
0	TCDMASel	Selection of a T0CMPDMAREQ signal request condition 1: Sets a T0CMPDMAREQ signal request at terminal count occurrence. 0: Sets a T0CMPDMAREQ signal request at compare occurrence.		RW modify	0

6.111. ADVTMR_T0CMPDMAEN

ADVTMR_T0CMPDMAEN					
Description	T0 CmpDMA Enable Register				
Address Region	advtmr		**Type:**	RW	
Offset	0x0000 04A0				
Physical address View0	0x4004 14A0				
Physical address View1	-				
Bitfield Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:1	Reserved	-		-	-
0	CmpDMAEn	T0CMPDMAREQ control 1: CmpDMA request enable 0: CmpDMA request disable		RW modify	0

6.112. ADVTMR_T0CAPDMASYNC

ADVTMR_T0CAPDMASYNC			
Description	T0 CapDMAC signals Synchronization Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 04B8		
Physical address View0	0x4004 14B8		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:1	Reserved	-	-	-
0	CapDMASync	Synchronization control of T0CAPDMACLR and T0CAPDMATC 1: Synchronizes input (for external input with clock not synchronized) 0: Does not synchronize input (for external input with clock synchronized)	RW modify	0

6.113. ADVTMR_T0CMPDMASYNC

ADVTMR_T0CMPDMASYNC			
Description	T0 CmpDMAC signals Synchronization Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 04BC		
Physical address View0	0x4004 14BC		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:1	Reserved	-	-	-
0	CmpDMASync	Synchronization control of T0CMPDMACLR and T0CMPDMATC 1: Synchronizes input (for external input with clock not synchronized) 0: Does not synchronize input (for external input with clock synchronized)	RW modify	0

6.114. ADVTMR_T0CAPDMACLR

ADVTMR_T0CAPDMACLR			
Description	T0 CapDMA clear Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 04F0		
Physical address View0	0x4004 14F0		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:1	Reserved	-	-	-
0	CapDMAClr	Can forcibly clear a generated CapDMA request.	RW oneToClear	0

		1: Clears the DMA request. 0: Does nothing. (The request can be cleared only for CAPDMAEN=1.)		

6.115. ADVTMR_T0CMPDMACLR

ADVTMR_T0CMPDMACLR			
Description	T0 CmpDMA clear Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 04F4		
Physical address View0	0x4004 14F4		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CmpDMAClr	Can forcibly clear a generated CmpDMA request. 1: Clears the DMA request. 0: Does nothing. (The request can be cleared only for CMPDMAEN=1.)	RW oneToClear	0

6.116. ADVTMR_T1TFFEN

ADVTMR_T1TFFEN			
Description	T1 TFF Enable Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0500		
Physical address View0	0x4004 1500		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	TFFEn	TFF (Toggle Flip-Flop) operation control	RW modify	0

6.117. ADVTMR_T1TFFSTAT

ADVTMR_T1TFFSTAT			
Description	T1 TFF Status Register		
Address Region	advtmr	**Type:**	RO
Offset	0x0000 0504		
Physical address View0	0x4004 1504		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-

0	TFFStat	TFF (Toggle Flip-Flop) output status (indicating the status before the last stage of Timer1TFFInv)	RO	0

6.118. ADVTMR_T1TFFZERO

ADVTMR_T1TFFZERO				
Description	T1 TFF Zero Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 0508			
Physical address View0	0x4004 1508			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	TFFZero	TFF (Toggle Flip-Flop) operation control (selection of whether or not TFF is toggled at the falling edge when the timer counter is 0)	RW modify	0

6.119. ADVTMR_T1TFFINV

ADVTMR_T1TFFINV				
Description	T1 TFF Invert Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 050C			
Physical address View0	0x4004 150C			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	TFFInv	TFF (Toggle Flip-Flop) operation control (selection of whether or not the output is reversed at its last stage)	RW modify	0

6.120. ADVTMR_T1TFFCTRL

ADVTMR_T1TFFCTRL				
Description	T1 TFF Control Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 0510			
Physical address View0	0x4004 1510			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:2	Reserved	-	-	-
1:0	TFFCtrl	Selection of TFF (Toggle Flip-Flop) output operation	RW modify	0x3

6.121. ADVTMR_T1TFFINIT

ADVTMR_T1TFFINIT			
Description	T1 TFF Init Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0514		
Physical address View0	0x4004 1514		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	TFFInit	TFF (Toggle Flip-Flop) operation control (selection of output initial value)	RW modify	0

6.122. ADVTMR_T1EVCONTROL

ADVTMR_T1EVCONTROL			
Description	T1 Event Control Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0520		
Physical address View0	0x4004 1520		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:6	Reserved	-	-	-
5:4	Event_Select	Event counter operation selection	RW modify	0x0
3	EvSync	Selection of event counter input synchronization	RW modify	1
2	Reserved	-	-	-
1	EvDelay	Selection of event counter count start delay	RW modify	0
0	EventEn	Event counter control	RW modify	0

6.123. ADVTMR_T1EVSEL

ADVTMR_T1EVSEL			
Description	T1 EV Select Control Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0530		
Physical address View0	0x4004 1530		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:7	Reserved	-	-	-
6:4	EVCNTSRC_Sel	EVCNTSRC I/O control Input selection signal: Generation of the output level of the T1EVSRCSEL	RW modify	0x0

		signals. 111: ADVTMR:T3TFFOUT 110: ADVTMR:T2TFFOUT 101: ADVTMR:T0TIMINT(ch0->ch1 cascade connect) 100: ADVTMR:T0TFFOUT 011: PIN:MCU_I2C0_CLK(Pin share=FMOD2) 010: PIN:MCU_I2C0_DATA(Pin share=FMOD2) 001: PIN:MCU_UA0_TXD(Pin share=FMOD2), PIN:MCU_GPIO_13(Pin share=FMOD3) 000: PIN:MCU_UA0_RXD(Pin share=FMOD2), PIN:MCU_GPIO_12(Pin share=FMOD3)		
3	Reserved	-	-	-
2:0	EVCNTEN_Sel	EVCNTEN I/O control Input selection signal: Generation of the output level of the T1EVENSEL signals. 111: ADVTMR:T3TFFOUT 110: ADVTMR:T2TFFOUT 101: ADVTMR:T0TIMINT(ch0->ch1 cascade connect) 100: ADVTMR:T0TFFOUT 011: PIN:MCU_I2C0_CLK(Pin share=FMOD2) 010: PIN:MCU_I2C0_DATA(Pin share=FMOD2) 001: PIN:MCU_UA0_TXD(Pin share=FMOD2), PIN:MCU_GPIO_13(Pin share=FMOD3) 000: PIN:MCU_UA0_RXD(Pin share=FMOD2), PIN:MCU_GPIO_12(Pin share=FMOD3)	RW modify	0x0

6.124. ADVTMR_T1IOSEL

ADVTMR_T1IOSEL			
Description	T1 IO Select Control Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0534		
Physical address View0	0x4004 1534		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	IOSel	T1TFFOUT I/O control 1: T1TFFOUT output 0: Input from external pin or not output	RW modify	0

6.125. ADVTMR_T1CAPSEL

ADVTMR_T1CAPSEL			
Description	T1 Capture Select Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0538		
Physical address View0	0x4004 1538		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:3	Reserved	-	-	-
2:0	CapSel	Capture input selection Input selection signal: Generates the output level of the T1CAPSEL signals. 111: ADVTMR:T3TFFOUT 110: ADVTMR:T2TFFOUT 101: EVM:evm_advtimer_capture[1] 100: ADVTMR:T0TFFOUT 011: PIN:MCU_I2C0_CLK(Pin share=FMOD2) 010: PIN:MCU_I2C0_DATA(Pin share=FMOD2) 001: PIN:MCU_UA0_TXD(Pin share=FMOD2), PIN:MCU_GPIO_13(Pin share=FMOD3) 000: PIN:MCU_UA0_RXD(Pin share=FMOD2), PIN:MCU_GPIO_12(Pin share=FMOD3)	RW modify	0x0

6.126. ADVTMR_T1CAPDMAEN

ADVTMR_T1CAPDMAEN			
Description	T1 CapDMA Enable Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0580		
Physical address View0	0x4004 1580		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CapDMAEn	T1CAPDMAREQ control	RW modify	0

6.127. ADVTMR_T1CAPDMASTAT

ADVTMR_T1CAPDMASTAT				
Description	T1 CapDMA Status Register			
Address Region	advtmr	**Type:**	RO	
Offset	0x0000 0590			
Physical address View0	0x4004 1590			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CapDMAStat	CapDMA transfer status	RO	0

6.128. ADVTMR_T1CMPDMASTAT

ADVTMR_T1CMPDMASTAT				
Description	T1 CmpDMA Status Register			
Address Region	advtmr	**Type:**	RO	
Offset	0x0000 0598			
Physical address View0	0x4004 1598			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CmpDMAStat	CmpDMA transfer status	RO	0

6.129. ADVTMR_T1TCDMASEL

ADVTMR_T1TCDMASEL				
Description	T1 Terminal Count DMA Request Select Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 059C			
Physical address View0	0x4004 159C			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	TCDMASel	Selection of a T1CMPDMAREQ signal request condition	RW modify	0

6.130. ADVTMR_T1CMPDMAEN

ADVTMR_T1CMPDMAEN			
Description	T1 CmpDMA Enable Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 05A0		
Physical address View0	0x4004 15A0		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CmpDMAEn	T1CMPDMAREQ control	RW modify	0

6.131. ADVTMR_T1CAPDMASYNC

ADVTMR_T1CAPDMASYNC			
Description	T1 CapDMAC signals Synchronization Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 05B8		
Physical address View0	0x4004 15B8		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CapDMASync	Synchronization control of T1CAPDMACLR and T1CAPDMATC inputs	RW modify	0

6.132. ADVTMR_T1CMPDMASYNC

ADVTMR_T1CMPDMASYNC			
Description	T1 CmpDMAC signals Synchronization Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 05BC		
Physical address View0	0x4004 15BC		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CmpDMASync	Synchronization control of T1CMPDMACLR and T1CMPDMATC inputs	RW modify	0

6.133. ADVTMR_T1CAPDMACLR

ADVTMR_T1CAPDMACLR				
Description	T1 CapDMA clear Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 05F0			
Physical address View0	0x4004 15F0			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CapDMAClr	Can clear a CapDMA request forcibly.	RW oneToClear	0

6.134. ADVTMR_T1CMPDMACLR

ADVTMR_T1CMPDMACLR				
Description	T1 CmpDMA clear Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 05F4			
Physical address View0	0x4004 15F4			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CmpDMAClr	Can clear a CmpDMA request forcibly.	RW oneToClear	0

6.135. ADVTMR_T2TFFEN

ADVTMR_T2TFFEN				
Description	T2 TFF Enable Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 0600			
Physical address View0	0x4004 1600			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	TFFEn	TFF (Toggle Flip-Flop) operation control	RW modify	0

6.136. ADVTMR_T2TFFSTAT

ADVTMR_T2TFFSTAT			
Description	T2 TFF Status Register		
Address Region	advtmr	**Type:**	RO
Offset	0x0000 0604		
Physical address View0	0x4004 1604		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	TFFStat	TFF (Toggle Flip-Flop) output status (indicating the status before the last stage of Timer2TFFInv)	RO	0

6.137. ADVTMR_T2TFFZERO

ADVTMR_T2TFFZERO			
Description	T2 TFF Zero Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0608		
Physical address View0	0x4004 1608		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	TFFZero	TFF (Toggle Flip-Flop) operation control (selection of whether or not TFF is toggled at the falling edge when the timer counter is 0)	RW modify	0

6.138. ADVTMR_T2TFFINV

ADVTMR_T2TFFINV			
Description	T2 TFF Invert Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 060C		
Physical address View0	0x4004 160C		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	TFFInv	TFF (Toggle Flip-Flop) operation control (selection of whether or not the output is reversed at its last stage)	RW modify	0

6.139. ADVTMR_T2TFFCTRL

ADVTMR_T2TFFCTRL			
Description	T2 TFF Control Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0610		
Physical address View0	0x4004 1610		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:2	Reserved	-	-	-
1:0	TFFCtrl	Selection of TFF (Toggle Flip-Flop) output operation	RW modify	0x3

6.140. ADVTMR_T2TFFINIT

ADVTMR_T2TFFINIT			
Description	T2 TFF Init Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0614		
Physical address View0	0x4004 1614		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	TFFInit	TFF (Toggle Flip-Flop) operation control (selection of output initial value)	RW modify	0

6.141. ADVTMR_T2EVCONTROL

ADVTMR_T2EVCONTROL			
Description	T2 Event Control Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0620		
Physical address View0	0x4004 1620		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:6	Reserved	-	-	-
5:4	Event_Select	Event counter operation selection	RW modify	0x0
3	EvSync	Selection of event counter input synchronization	RW modify	1
2	Reserved	-	-	-
1	EvDelay	Selection of event counter count start delay	RW modify	0
0	EventEn	Event counter control	RW modify	0

6.142. ADVTMR_T2EVSEL

ADVTMR_T2EVSEL			
Description	T2 EV Select Control Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0630		
Physical address View0	0x4004 1630		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:7	Reserved	-	-	-
6:4	EVCNTSRC_Sel	EVCNTSRC I/O control Input selection signal: Generation of the output level of the T2EVSRCSEL signals. 111: ADVTMR:T3TFFOUT 110: ADVTMR:T1TIMINT(ch1->ch2 cascade connect) 101: ADVTMR:T1TFFOUT 100: ADVTMR:T0TFFOUT 011: PIN:MCU_I2C0_CLK(Pin share=FMOD2) 010: PIN:MCU_I2C0_DATA(Pin share=FMOD2) 001: PIN:MCU_UA0_TXD(Pin share=FMOD2), PIN:MCU_GPIO_13(Pin share=FMOD3) 000: PIN:MCU_UA0_RXD(Pin share=FMOD2), PIN:MCU_GPIO_12(Pin share=FMOD3)	RW modify	0x0
3	Reserved	-	-	-
2:0	EVCNTEN_Sel	EVCNTEN I/O control Input selection signal: Generation of the output level of the T2EVENSEL signals. 111: ADVTMR:T3TFFOUT 110: ADVTMR:T1TIMINT(ch1->ch2 cascade connect) 101: ADVTMR:T1TFFOUT 100: ADVTMR:T0TFFOUT 011: PIN:MCU_I2C0_CLK(Pin share=FMOD2) 010: PIN:MCU_I2C0_DATA(Pin share=FMOD2) 001: PIN:MCU_UA0_TXD(Pin share=FMOD2), PIN:MCU_GPIO_13(Pin share=FMOD3) 000: PIN:MCU_UA0_RXD(Pin share=FMOD2), PIN:MCU_GPIO_12(Pin share=FMOD3)	RW modify	0x0

6.143. ADVTMR_T2IOSEL

ADVTMR_T2IOSEL			
Description	T2 IO Select Control Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0634		
Physical address View0	0x4004 1634		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	IOSel	T2TFFOUT I/O control 1: T2TFFOUT output 0: Input from external pin or not output	RW modify	0

6.144. ADVTMR_T2CAPSEL

ADVTMR_T2CAPSEL			
Description	T2 Capture Select Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0638		
Physical address View0	0x4004 1638		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:3	Reserved	-	-	-
2:0	CapSel	Capture input selection Input selection signal: Generates the output level of the T2CAPSEL signals. 111: ADVTMR:T3TFFOUT 110: EVM:evm_advtimer_capture[2] 101: ADVTMR:T1TFFOUT 100: ADVTMR:T0TFFOUT 011: PIN:MCU_I2C0_CLK(Pin share=FMOD2) 010: PIN:MCU_I2C0_DATA(Pin share=FMOD2) 001: PIN:MCU_UA0_TXD(Pin share=FMOD2), PIN:MCU_GPIO_13(Pin share=FMOD3) 000: PIN:MCU_UA0_RXD(Pin share=FMOD2), PIN:MCU_GPIO_12(Pin share=FMOD3)	RW modify	0x0

6.145. ADVTMR_T2CAPDMAEN

ADVTMR_T2CAPDMAEN			
Description	T2 CapDMA Enable Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0680		
Physical address View0	0x4004 1680		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CapDMAEn	T2CAPDMAREQ control	RW modify	0

6.146. ADVTMR_T2CAPDMASTAT

ADVTMR_T2CAPDMASTAT			
Description	T2 CapDMA Status Register		
Address Region	advtmr	**Type:**	RO
Offset	0x0000 0690		
Physical address View0	0x4004 1690		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CapDMAStat	CapDMA transfer status	RO	0

6.147. ADVTMR_T2CMPDMASTAT

ADVTMR_T2CMPDMASTAT			
Description	T2 CmpDMA Status Register		
Address Region	advtmr	**Type:**	RO
Offset	0x0000 0698		
Physical address View0	0x4004 1698		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CmpDMAStat	CmpDMA transfer status	RO	0

6.148. ADVTMR_T2TCDMASEL

ADVTMR_T2TCDMASEL				
Description	T2 Terminal Count DMA Request Select Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 069C			
Physical address View0	0x4004 169C			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	TCDMASel	Selection of a T2CMPDMAREQ signal request condition	RW modify	0

6.149. ADVTMR_T2CMPDMAEN

ADVTMR_T2CMPDMAEN				
Description	T2 CmpDMA Enable Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 06A0			
Physical address View0	0x4004 16A0			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CmpDMAEn	T2CMPDMAREQ control	RW modify	0

6.150. ADVTMR_T2CAPDMASYNC

ADVTMR_T2CAPDMASYNC				
Description	T2 CapDMAC signals Synchronization Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 06B8			
Physical address View0	0x4004 16B8			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CapDMASync	Synchronization control of T2CAPDMACLR and T2CAPDMATC inputs	RW modify	0

6.151. ADVTMR_T2CMPDMASYNC

ADVTMR_T2CMPDMASYNC				
Description	T2 CmpDMAC signals Synchronization Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 06BC			
Physical address View0	0x4004 16BC			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CmpDMASync	Synchronization control of T2CMPDMACLR and T2CMPDMATC inputs	RW modify	0

6.152. ADVTMR_T2CAPDMACLR

ADVTMR_T2CAPDMACLR				
Description	T2 CapDMA clear Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 06F0			
Physical address View0	0x4004 16F0			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CapDMAClr	Can clear a CapDMA request forcibly.	RW oneToClear	0

6.153. ADVTMR_T2CMPDMACLR

ADVTMR_T2CMPDMACLR				
Description	T2 CmpDMA clear Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 06F4			
Physical address View0	0x4004 16F4			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CmpDMAClr	Can clear a CmpDMA request forcibly.	RW oneToSet	0

6.154. ADVTMR_T3TFFEN

ADVTMR_T3TFFEN			
Description	T3 TFF Enable Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0700		
Physical address View0	0x4004 1700		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	TFFEn	TFF (Toggle Flip-Flop) operation control	RW modify	0

6.155. ADVTMR_T3TFFSTAT

ADVTMR_T3TFFSTAT			
Description	T3 TFF Status Register		
Address Region	advtmr	**Type:**	RO
Offset	0x0000 0704		
Physical address View0	0x4004 1704		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	TFFStat	TFF (Toggle Flip-Flop) output status (indicating the status before the last stage of Timer3TFFInv)	RO	0

6.156. ADVTMR_T3TFFZERO

ADVTMR_T3TFFZERO			
Description	T3 TFF Zero Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0708		
Physical address View0	0x4004 1708		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	TFFZero	TFF (Toggle Flip-Flop) operation control (selection of whether or not TFF is toggled at the falling edge when the timer counter is 0)	RW modify	0

6.157. ADVTMR_T3TFFINV

ADVTMR_T3TFFINV			
Description	T3 TFF Invert Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 070C		
Physical address View0	0x4004 170C		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	TFFInv	TFF (Toggle Flip-Flop) operation control (selection of whether or not the output is reversed at its last stage)	RW modify	0

6.158. ADVTMR_T3TFFCTRL

ADVTMR_T3TFFCTRL			
Description	T3 TFF Control Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0710		
Physical address View0	0x4004 1710		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:2	Reserved	-	-	-
1:0	TFFCtrl	Selection of TFF (Toggle Flip-Flop) output operation	RW modify	0x3

6.159. ADVTMR_T3TFFINIT

ADVTMR_T3TFFINIT			
Description	T3 TFF Init Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0714		
Physical address View0	0x4004 1714		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	TFFInit	TFF (Toggle Flip-Flop) operation control (selection of output initial value)	RW modify	0

6.160. ADVTMR_T3EVCONTROL

ADVTMR_T3EVCONTROL			
Description	T3 Event Control Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0720		
Physical address View0	0x4004 1720		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:6	Reserved	-	-	-
5:4	Event_Select	Event counter operation selection	RW modify	0x0
3	EvSync	Selection of event counter input synchronization	RW modify	1
2	Reserved	-	-	-
1	EvDelay	Selection of event counter count start delay	RW modify	0
0	EventEn	Event counter control	RW modify	0

6.161. ADVTMR_T3EVSEL

ADVTMR_T3EVSEL			
Description	T3 EV Select Control Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0730		
Physical address View0	0x4004 1730		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:7	Reserved	-	-	-
6:4	EVCNTSRC_Sel	EVCNTSRC I/O control Input selection signal: Generation of the output level of the T3EVSRCSEL signals. 111: ADVTMR:T2TIMINT(ch2->ch3 cascade connect) 110: ADVTMR:T2TFFOUT 101: ADVTMR:T1TFFOUT 100: ADVTMR:T0TFFOUT 011: PIN:MCU_I2C0_CLK(Pin share=FMOD2) 010: PIN:MCU_I2C0_DATA(Pin share=FMOD2) 001: PIN:MCU_UA0_TXD(Pin share=FMOD2), PIN:MCU_GPIO_13(Pin share=FMOD3) 000: PIN:MCU_UA0_RXD(Pin share=FMOD2), PIN:MCU_GPIO_12(Pin share=FMOD3)	RW modify	0x0
3	Reserved	-	-	-
2:0	EVCNTEN_Sel	EVCNTEN I/O control Input selection signal: Generation of the	RW modify	0x0

		output level of the T3EVENSEL signals. 111: ADVTMR:T3TFFOUT 110: ADVTMR:T2TFFOUT 101: ADVTMR:T1TFFOUT 100: ADVTMR:T0TFFOUT 011: PIN:MCU_I2C0_CLK(Pin share=FMOD2) 010: PIN:MCU_I2C0_DATA(Pin share=FMOD2) 001: PIN:MCU_UA0_TXD(Pin share=FMOD2), PIN:MCU_GPIO_13(Pin share=FMOD3) 000: PIN:MCU_UA0_RXD(Pin share=FMOD2), PIN:MCU_GPIO_12(Pin share=FMOD3)		

6.162. ADVTMR_T3IOSEL

ADVTMR_T3IOSEL					
Description	T3 IO Select Control Register				
Address Region	advtmr		**Type:**	RW	
Offset	0x0000 0734				
Physical address View0	0x4004 1734				
Physical address View1	-				
Bitfield Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:1	Reserved	-		-	-
0	IOSel	T3TFFOUT I/O control		RW modify	0

6.163. ADVTMR_T3CAPSEL

ADVTMR_T3CAPSEL					
Description	T3 Capture Select Register				
Address Region	advtmr		**Type:**	RW	
Offset	0x0000 0738				
Physical address View0	0x4004 1738				
Physical address View1	-				
Bitfield Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:3	Reserved	-		-	-
2:0	CapSel	Capture input selection Input selection signal: Generates the output level of the T3CAPSEL signals. 111: EVM:evm_advtimer_capture[3] 110: ADVTMR:T3TFFOUT 101: ADVTMR:T1TFFOUT 100: ADVTMR:T0TFFOUT 011: PIN:MCU_I2C0_CLK(Pin share=FMOD2) 010: PIN:MCU_I2C0_DATA(Pin share=FMOD2) 001: PIN:MCU_UA0_TXD(Pin		RW modify	0x0

		share=FMOD2), PIN:MCU_GPIO_13(Pin share=FMOD3) 000: PIN:MCU_UA0_RXD(Pin share=FMOD2), PIN:MCU_GPIO_12(Pin share=FMOD3)		

6.164. ADVTMR_T3CAPDMAEN

ADVTMR_T3CAPDMAEN					
Description	T3 CapDMA Enable Register				
Address Region	advtmr		**Type:**	RW	
Offset	0x0000 0780				
Physical address View0	0x4004 1780				
Physical address View1	-				
Bitfield Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:1	Reserved	-		-	-
0	CapDMAEn	T3CAPDMAREQ control 1: T3TFFOUT output 0: Input from external pin or not output		RW modify	0

6.165. ADVTMR_T3CAPDMASTAT

ADVTMR_T3CAPDMASTAT					
Description	T3 CapDMA Status Register				
Address Region	advtmr		**Type:**	RO	
Offset	0x0000 0790				
Physical address View0	0x4004 1790				
Physical address View1	-				
Bitfield Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:1	Reserved	-		-	-
0	CapDMAStat	CapDMA transfer status		RO	0

6.166. ADVTMR_T3CMPDMASTAT

ADVTMR_T3CMPDMASTAT			
Description	T3 CmpDMA Status Register		
Address Region	advtmr	**Type:**	RO
Offset	0x0000 0798		
Physical address View0	0x4004 1798		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CmpDMAStat	CmpDMA transfer status	RO	0

6.167. ADVTMR_T3TCDMASEL

ADVTMR_T3TCDMASEL			
Description	T3 Terminal Count DMA Request Select Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 079C		
Physical address View0	0x4004 179C		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	TCDMASel	Selection of a T3CMPDMAREQ signal request condition	RW modify	0

6.168. ADVTMR_T3CMPDMAEN

ADVTMR_T3CMPDMAEN			
Description	T3 CmpDMA Enable Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 07A0		
Physical address View0	0x4004 17A0		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	-	-	-
0	CmpDMAEn	T3CMPDMAREQ control	RW modify	0

6.169. ADVTMR_T3CAPDMASYNC

ADVTMR_T3CAPDMASYNC			
Description	T3 CapDMAC signals Synchronization Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 07B8		
Physical address View0	0x4004 17B8		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:1	Reserved	-	-	-
0	CapDMASync	Synchronization control of T3CAPDMACLR and T3CAPDMATC inputs	RW modify	0

6.170. ADVTMR_T3CMPDMASYNC

ADVTMR_T3CMPDMASYNC			
Description	T3 CmpDMAC signals Synchronization Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 07BC		
Physical address View0	0x4004 17BC		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:1	Reserved	-	-	-
0	CmpDMASync	Synchronization control of T3CMPDMACLR and T3CMPDMATC inputs	RW modify	0

6.171. ADVTMR_T3CAPDMACLR

ADVTMR_T3CAPDMACLR			
Description	T3 CapDMA clear Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 07F0		
Physical address View0	0x4004 17F0		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:1	Reserved	-	-	-
0	CapDMAClr	Can clear a CapDMA request forcibly.	RW oneToClear	0

6.172. ADVTMR_T3CMPDMACLR

ADVTMR_T3CMPDMACLR			
Description	T3 CmpDMA clear Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 07F4		
Physical address View0	0x4004 17F4		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:1	Reserved	-	-	-
0	CmpDMAClr	Can clear a CmpDMA request forcibly.	RW oneToClear	0

6.173. ADVTMR_TITCR

ADVTMR_TITCR			
Description	Timer Integration test control Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0F00		
Physical address View0	0x4004 1F00		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:1	Reserved	-	-	-
0	Test_Mode_Enable	Test mode control 1: Test mode status 0: Normal operation status	RW modify	0

6.174. ADVTMR_TITOP

ADVTMR_TITOP			
Description	Timer Integration test output set Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0F04		
Physical address View0	0x4004 1F04		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:4	Reserved	-	-	-
3	TestT3TIMINT	T3TIMINT signal output (only in test mode) 1: T3TIMINT="1" 0: T3TIMINT="0"	RW modify	0
2	TestT2TIMINT	T2TIMINT signal output (only in test mode) 1: T2TIMINT="1" 0: T2TIMINT="0"	RW modify	0
1	TestT1TIMINT	T1TIMINT signal output (only in test	RW	0

		mode) 1: T1TIMINT="1" 0: T1TIMINT="0"	modify	
0	TestT0TIMINT	T0TIMINT signal output (only in test mode) 1: T0TIMINT="1" 0: T0TIMINT="0"	RW modify	0

6.175. ADVTMR_TOTSYNC

ADVTMR_TOTSYNC			
Description	Timer Other Timer Synchronization Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0F10		
Physical address View0	0x4004 1F10		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:8	Reserved	-	-	-
7:0	OTSync	Controls TIMCLKEN of other timers. The timer that can be controlled depends on connection. To establish synchronization with multiple timers, OTSYNC[x] output from this timer should be connected to TxTIMCLKEN of each timer. TxTIMCLKEN of this timer should be connected to OTSYNC[x]. Each timer should have the same setting value. The timer can be synchronously operated by writing 1 to connected OTSYNC[x:x] at the same time. (The following shows a connection of TZ1000.) OTSYNC[0]-->ADVTMR:T0TIMCLKEN OTSYNC[1]-->ADVTMR:T1TIMCLKEN OTSYNC[2]-->ADVTMR:T2TIMCLKEN OTSYNC[3]-->ADVTMR:T3TIMCLKEN OTSYNC[4]-->not connect OTSYNC[5]-->not connect OTSYNC[6]-->not connect OTSYNC[7]-->not connect	RW modify	0xFF

6.176. ADVTMR_T0ITCMPCAPINT

ADVTMR_T0ITCMPCAPINT				
Description	T0 ITCompare_Capture Interrupt set Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 0F20			
Physical address View0	0x4004 1F20			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:9	Reserved	-	-	-
8	TestT0CMPINT	T0CMPINT output control 1: T0CMPINT="1" 0: T0CMPINT="0"	RW modify	0
7:1	Reserved	-	-	-
0	TestT0CAPINT	T0CAPINT output control 1: T0CAMPINT="1" 0: T0CAPINT="0"	RW modify	0

6.177. ADVTMR_T1ITCMPCAPINT

ADVTMR_T1ITCMPCAPINT				
Description	T1 ITCompare_Capture Interrupt set Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 0F24			
Physical address View0	0x4004 1F24			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:9	Reserved	-	-	-
8	TestT1CMPINT	T1CMPINT output control 1: T1CMPINT="1" 0: T1CMPINT="0"	RW modify	0
7:1	Reserved	-	-	-
0	TestT1CAPINT	T1CAPINT output control 1: T1CAPINT="1" 0: T1CAPINT="0"	RW modify	0

6.178. ADVTMR_T2ITCMPCAPINT

ADVTMR_T2ITCMPCAPINT				
Description	T2 ITCompare_Capture Interrupt set Register			
Address Region	advtmr	**Type:**	RW	
Offset	0x0000 0F28			
Physical address View0	0x4004 1F28			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:9	Reserved	-	-	-

8	TestT2CMPINT	T2CMPINT output control 1: T2CMPINT="1" 0: T2CMPINT="0"	RW modify	0
7:1	Reserved	-	-	-
0	TestT2CAPINT	T2CAPINT output control 1: T2CAPINT="1" 0: T2CAPINT="0"	RW modify	0

6.179. ADVTMR_T3ITCMPCAPINT

ADVTMR_T3ITCMPCAPINT			
Description	T3 ITCompare_Capture Interrupt set Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0F2C		
Physical address View0	0x4004 1F2C		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:9	Reserved	-	-	-
8	TestT3CMPINT	T3CMPINT output control 1: T3CMPINT="1" 0: T3CMPINT="0"	RW modify	0
7:1	Reserved	-	-	-
0	TestT3CAPINT	T3CAPINT output control 1: T3CAPINT="1" 0: T3CAPINT="0"	RW modify	0

6.180. ADVTMR_T0ITEVCNT

ADVTMR_T0ITEVCNT			
Description	T0 ITEVCNT Input Register		
Address Region	advtmr	**Type:**	RO
Offset	0x0000 0F40		
Physical address View0	0x4004 1F40		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:2	Reserved	-	-	-
1	Test_T0EVCNTSRC	T0EVCNTSRC input status 1: T0EVCNTSRC="1" 0: T0EVCNTSRC="0"	RO	0
0	Test_T0EVCNTEN	T0EVCNTEN input status 1: T0EVCNTEN="1" 0: T0EVCNTEN="0"	RO	0

6.181. ADVTMR_T1ITEVCNT

ADVTMR_T1ITEVCNT			
Description	T1 ITEVCNT Input Register		
Address Region	advtmr	**Type:**	RO
Offset	0x0000 0F44		
Physical address View0	0x4004 1F44		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:2	Reserved	-	-	-
1	Test_T1EVCNTSRC	T1EVCNTSRC input status 1: T1EVCNTSRC="1" 0: T1EVCNTSRC="0"	RO	0
0	Test_T1EVCNTEN	T1EVCNTEN input status 1: T1EVCNTEN="1" 0: T1EVCNTEN="0"	RO	0

6.182. ADVTMR_T2ITEVCNT

ADVTMR_T2ITEVCNT			
Description	T2 ITEVCNT Input Register		
Address Region	advtmr	**Type:**	RO
Offset	0x0000 0F48		
Physical address View0	0x4004 1F48		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:2	Reserved	-	-	-
1	Test_T2EVCNTSRC	T2EVCNTSRC input status 1: T2EVCNTSRC="1" 0: T2EVCNTSRC="0"	RO	0
0	Test_T2EVCNTEN	T2EVCNTEN input status 1: T2EVCNTEN="1" 0: T2EVCNTEN="0"	RO	0

6.183. ADVTMR_T3ITEVCNT

ADVTMR_T3ITEVCNT			
Description	T3 ITEVCNT Input Register		
Address Region	advtmr	**Type:**	RO
Offset	0x0000 0F4C		
Physical address View0	0x4004 1F4C		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:2	Reserved	-	-	-
1	Test_T3EVCNTSRC	T3EVCNTSRC input status 1: T3EVCNTSRC="1" 0: T3EVCNTSRC="0"	RO	0

0	Test_T3EVCNTEN	T3EVCNTEN input status 1: T3EVCNTEN="1" 0: T3EVCNTEN="0"	RO	0

6.184. ADVTMR_T0ITCAPDRQCAPRQ

ADVTMR_T0ITCAPDRQCAPRQ			
Description	T0 ITCAPDMAREQ_CAPREQ Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0F60		
Physical address View0	0x4004 1F60		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:9	Reserved	-	-	-
8	TestT0CAPDREQ	T0CAPDREQ output control 1: T0CAPDMAREQ="1" 0: T0CAPDMAREQ="0"	RW modify	0
7:1	Reserved	-	-	-
0	TestT0CAPREQ	T0CAPREQ input status 1: T0CAPREQ="1" 0: T0CAPREQ="0"	RO	0

6.185. ADVTMR_T0ITCAPDTCDCLR

ADVTMR_T0ITCAPDTCDCLR			
Description	T0 ITCAPDMATC_CAPDMACLR Register		
Address Region	advtmr	**Type:**	RO
Offset	0x0000 0F64		
Physical address View0	0x4004 1F64		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:9	Reserved	-	-	-
8	TestT0CAPDTC	T0CAPDTC input status 1: T0CAPDMATC="1" 0: T0CAPDMATC="0"	RO	0
7:1	Reserved	-	-	-
0	TestT0CAPDCLR	T0CAPDCLR input status 1: T0CAPDMACLR="1" 0: T0CAPDMACLR="0"	RO	0

6.186. ADVTMR_T1ITCAPDRQCAPRQ

ADVTMR_T1ITCAPDRQCAPRQ			
Description	T1 ITCAPDMAREQ_CAPREQ Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0F68		
Physical address View0	0x4004 1F68		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:9	Reserved	-	-	-
8	TestT1CAPDREQ	T1CAPDREQ output control 1: T1CAPDMAREQ="1" 0: T1CAPDMAREQ="0"	RW modify	0
7:1	Reserved	-	-	-
0	TestT1CAPREQ	T1CAPREQ input status 1: T1CAPREQ="1" 0: T1CAPREQ="0"	RO	0

6.187. ADVTMR_T1ITCAPDTCDCLR

ADVTMR_T1ITCAPDTCDCLR			
Description	T1 ITCAPDMATC_CAPDMACLR Register		
Address Region	advtmr	**Type:**	RO
Offset	0x0000 0F6C		
Physical address View0	0x4004 1F6C		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:9	Reserved	-	-	-
8	TestT1CAPDTC	T1CAPDTC input status 1: T1CAPDMATC="1" 0: T1CAPDMATC="0"	RO	0
7:1	Reserved	-	-	-
0	TestT1CAPDCLR	T1CAPDCLR input status 1: T1CAPDMACLR="1" 0: T1CAPDMACLR="0"	RO	0

6.188. ADVTMR_T2ITCAPDRQCAPRQ

ADVTMR_T2ITCAPDRQCAPRQ			
Description	T2 ITCAPDMAREQ_CAPREQ Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0F70		
Physical address View0	0x4004 1F70		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:9	Reserved	-	-	-

8	TestT2CAPDREQ	T2CAPDREQ output control 1: T2CAPDMAREQ="1" 0: T2CAPDMAREQ="0"	RW modify	0
7:1	Reserved	-	-	-
0	TestT2CAPREQ	T2CAPREQ input status 1: T2CAPREQ="1" 0: T2CAPREQ="0"	RO	0

6.189. ADVTMR_T2ITCAPDTCDCLR

ADVTMR_T2ITCAPDTCDCLR			
Description	T2 ITCAPDMATC_CAPDMACLR Register		
Address Region	advtmr	**Type:**	RO
Offset	0x0000 0F74		
Physical address View0	0x4004 1F74		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:9	Reserved	-	-	-
8	TestT2CAPDTC	T2CAPDTC input status 1: T2CAPDMATC="1" 0: T2CAPDMATC="0"	RO	0
7:1	Reserved	-	-	-
0	TestT2CAPDCLR	T2CAPDCLR input status 1: T2CAPDMACLR="1" 0: T2CAPDMACLR="0"	RO	0

6.190. ADVTMR_T3ITCAPDRQCAPRQ

ADVTMR_T3ITCAPDRQCAPRQ			
Description	T3 ITCAPDMAREQ_CAPREQ Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0F78		
Physical address View0	0x4004 1F78		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:9	Reserved	-	-	-
8	TestT3CAPDREQ	T3CAPDREQ output control 1: T3CAPDMAREQ="1" 0: T3CAPDMAREQ="0"	RW modify	0
7:1	Reserved	-	-	-
0	TestT3CAPREQ	T3CAPREQ input status 1: T3CAPREQ="1" 0: T3CAPREQ="0"	RO	0

6.191. ADVTMR_T3ITCAPDTCDCLR

ADVTMR_T3ITCAPDTCDCLR			
Description	T3 ITCAPDMATC_CAPDMACLR Register		
Address Region	advtmr	**Type:**	RO
Offset	0x0000 0F7C		
Physical address View0	0x4004 1F7C		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:9	Reserved	-	-	-
8	TestT3CAPDTC	T3CAPDTC input status 1: T3CAPDMATC="1" 0: T3CAPDMATC="0"	RO	0
7:1	Reserved	-	-	-
0	TestT3CAPDCLR	T3CAPDCLR input status 1: T3CAPDMACLR="1" 0: T3CAPDMACLR="0"	RO	0

6.192. ADVTMR_T0ITCMPDRQTFF

ADVTMR_T0ITCMPDRQTFF			
Description	T0 ITCMPDMAREQ_TFFOUT Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0FA0		
Physical address View0	0x4004 1FA0		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:9	Reserved	-	-	-
8	TestT0CMPDREQ	T0CMPDREQ output control 1: T0CMPDMAREQ="1" 0: T0CMPDMAREQ="0"	RW modify	0
7:1	Reserved	-	-	-
0	TestT0TFFOUT	T0TFFOUT output control 1: T0TFFOUT="1" 0: T0TFFOUT="0"	RW modify	0

6.193. ADVTMR_T0ITCMPDTCDCLR

ADVTMR_T0ITCMPDTCDCLR			
Description	T0 ITCMPDMATC_CMPDMACLR Register		
Address Region	advtmr	**Type:**	RO
Offset	0x0000 0FA4		
Physical address View0	0x4004 1FA4		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:9	Reserved	-	-	-

8	TestT0CMPDTC	T0CMPDTC input status 1: T0CMPDMATC="1" 0: T0CMPDMATC="0"	RO	0
7:1	Reserved	-	-	-
0	TestT0CMPDCLR	T0CMPDCLR input status 1: T0CMPDMACLR="1" 0: T0CMPDMACLR="0"	RO	0

6.194. ADVTMR_T1ITCMPDRQTFF

ADVTMR_T1ITCMPDRQTFF			
Description	T1 ITCMPDMAREQ_TFFOUT Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0FA8		
Physical address View0	0x4004 1FA8		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:9	Reserved	-	-	-
8	TestT1CMPDREQ	T1CMPDREQ output control 1: T1CMPDMAREQ="1" 0: T1CMPDMAREQ="0"	RW modify	0
7:1	Reserved	-	-	-
0	TestT1TFFOUT	T1TFFOUT output control 1: T1TFFOUT="1" 0: T1TFFOUT="0"	RW modify	0

6.195. ADVTMR_T1ITCMPDTCDCLR

ADVTMR_T1ITCMPDTCDCLR			
Description	T1 ITCMPDMATC_CMPDMACLR Register		
Address Region	advtmr	**Type:**	RO
Offset	0x0000 0FAC		
Physical address View0	0x4004 1FAC		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:9	Reserved	-	-	-
8	TestT1CMPDTC	T1CMPDTC input status 1: T1CMPDMATC="1" 0: T1CMPDMATC="0"	RO	0
7:1	Reserved	-	-	-
0	TestT1CMPDCLR	T1CMPDCLR input status 1: T1CMPDMACLR="1" 0: T1CMPDMACLR="0"	RO	0

6.196. ADVTMR_T2ITCMPDRQTFF

ADVTMR_T2ITCMPDRQTFF			
Description	T2 ITCMPDMAREQ_TFFOUT Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0FB0		
Physical address View0	0x4004 1FB0		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:9	Reserved	-	-	-
8	TestT2CMPDREQ	T2CMPDREQ output control 1: T2CMPDMAREQ="1" 0: T2CMPDMAREQ="0"	RW modify	0
7:1	Reserved	-	-	-
0	TestT2TFFOUT	T2TFFOUT output control 1: T2TFFOUT="1" 0: T2TFFOUT="0"	RW modify	0

6.197. ADVTMR_T2ITCMPDTCDCLR

ADVTMR_T2ITCMPDTCDCLR			
Description	T2 ITCMPDMATC_CMPDMACLR Register		
Address Region	advtmr	**Type:**	RO
Offset	0x0000 0FB4		
Physical address View0	0x4004 1FB4		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:9	Reserved	-	-	-
8	TestT2CMPDTC	T2CMPDTC input status 1: T2CMPDMATC="1" 0: T2CMPDMATC="0"	RO	0
7:1	Reserved	-	-	-
0	TestT2CMPDCLR	T2CMPDCLR input status 1: T2CMPDMACLR="1" 0: T2CMPDMACLR="0"	RO	0

6.198. ADVTMR_T3ITCMPDRQTFF

ADVTMR_T3ITCMPDRQTFF			
Description	T3 ITCMPDMAREQ_TFFOUT Register		
Address Region	advtmr	**Type:**	RW
Offset	0x0000 0FB8		
Physical address View0	0x4004 1FB8		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:9	Reserved	-	-	-

8	TestT3CMPDREQ	T3CMPDREQ output control 1: T3CMPDMAREQ="1" 0: T3CMPDMAREQ="0"	RW modify	0
7:1	Reserved	-	-	-
0	TestT3TFFOUT	T3TFFOUT output control 1: T3TFFOUT="1" 0: T3TFFOUT="0"	RW modify	0

6.199. ADVTMR_T3ITCMPDTCDCLR

ADVTMR_T3ITCMPDTCDCLR			
Description	T3 ITCMPDMATC_CMPDMACLR Register		
Address Region	advtmr	**Type:**	RO
Offset	0x0000 0FBC		
Physical address View0	0x4004 1FBC		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:9	Reserved	-	-	-
8	TestT3CMPDTC	T3CMPDTC input status 1: T3CMPDMATC="1" 0: T3CMPDMATC="0"	RO	0
7:1	Reserved	-	-	-
0	TestT3CMPDCLR	T3CMPDCLR input status 1: T3CMPDMACLR="1" 0: T3CMPDMACLR="0"	RO	0

6.200. ADVTMR_TPERIPHID0

ADVTMR_TPERIPHID0			
Description	Timer Peripheral ID0 Register		
Address Region	advtmr	**Type:**	RO
Offset	0x0000 0FE0		
Physical address View0	0x4004 1FE0		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:8	Reserved	-	-	-
7:0	Partnumber0	Peripheral ID (this register stores a value from a hardware viewpoint.) Partnumber (Lower) SP804=>04	RO	0x04

6.201. ADVTMR_TPERIPHID1

ADVTMR_TPERIPHID1			
Description	Timer Peripheral ID1 Register		
Address Region	advtmr	**Type:**	RO
Offset	0x0000 0FE4		
Physical address View0	0x4004 1FE4		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:4	Designer0	Peripheral ID (this register stores a value from a hardware viewpoint.) Designer(Lower) 54=>4	RO	0x4
3:0	Partnumber1	Peripheral ID (this register stores a value from a hardware viewpoint.) Partnumber(Lower) SP804=>8	RO	0x8

6.202. ADVTMR_TPERIPHID2

ADVTMR_TPERIPHID2			
Description	Timer Peripheral ID2 Register		
Address Region	advtmr	**Type:**	RO
Offset	0x0000 0FE8		
Physical address View0	0x4004 1FE8		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:4	Revision_number	Peripheral ID (this register stores a value from a hardware viewpoint.) Revision: 2nd=>2	RO	0x2
3:0	Designer1	Peripheral ID (this register stores a value from a hardware viewpoint.) Designer(Upper) 54=>5	RO	0x5

6.203. ADVTMR_TPERIPHID3

ADVTMR_TPERIPHID3			
Description	Timer Peripheral ID3 Register		
Address Region	advtmr	**Type:**	RO
Offset	0x0000 0FEC		
Physical address View0	0x4004 1FEC		
Physical address View1	-		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:16	Reserved	-	-	-
15:0	Configuration	Peripheral ID (this register stores a value from a hardware viewpoint.) Configuration: ba6 => 0216	RO	0x0216

6.204. ADVTMR_TPCELLID0

ADVTMR_TPCELLID0				
Description	Timer PrimeCell ID0 Register			
Address Region	advtmr	**Type:**	RO	
Offset	0x0000 0FF0			
Physical address View0	0x4004 1FF0			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	ADVTMR_TPCellID0	Peripheral ID (this register stores a value from a hardware viewpoint.)	RO	0x0D

6.205. ADVTMR_TPCELLID1

ADVTMR_TPCELLID1				
Description	Timer PrimeCell ID1 Register			
Address Region	advtmr	**Type:**	RO	
Offset	0x0000 0FF4			
Physical address View0	0x4004 1FF4			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	ADVTMR_TPCellID1	Peripheral ID (this register stores a value from a hardware viewpoint.)	RO	0xF0

6.206. ADVTMR_TPCELLID2

ADVTMR_TPCELLID2				
Description	Timer PrimeCell ID2 Register			
Address Region	advtmr	**Type:**	RO	
Offset	0x0000 0FF8			
Physical address View0	0x4004 1FF8			
Physical address View1	-			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:8	Reserved	-	-	-
7:0	ADVTMR_TPCellID2	Peripheral ID (this register stores a value from a hardware viewpoint.)	RO	0x05

6.207. ADVTMR_TPCELLID3

ADVTMR_TPCELLID3			
Description	Timer PrimeCell ID3 Register		
Address Region	advtmr	**Type:**	RO
Offset	0x0000 0FFC		
Physical address View0	0x4004 1FFC		
Physical address View1	-		

Bitfield Details

Bits	Name	Description	Access	Reset
31:8	Reserved	-	-	-
7:0	TimerPCellID3	Peripheral ID (this register stores a value from a hardware viewpoint.)	RO	0xB1

7. Precaution for Usage

7.1. Access Restriction Associated with Register Access

The registers in this module are assigned to a 4 KB space with 32-bit interval in the little endian format. The bit locations are as follows.

This module is connected to the bus with 32-bit wide. When 8-bit or 16-bit data is accessed, the operation is in units of 32-bit only. This means that 8-bit or 16-bit access results in reading or writing the other bits than the content bits. So, 32-bit access is recommended. Otherwise, a read error or a write error may occur.

The write to a non-existing bit in a register is ignored. The read of the bit returns 0.

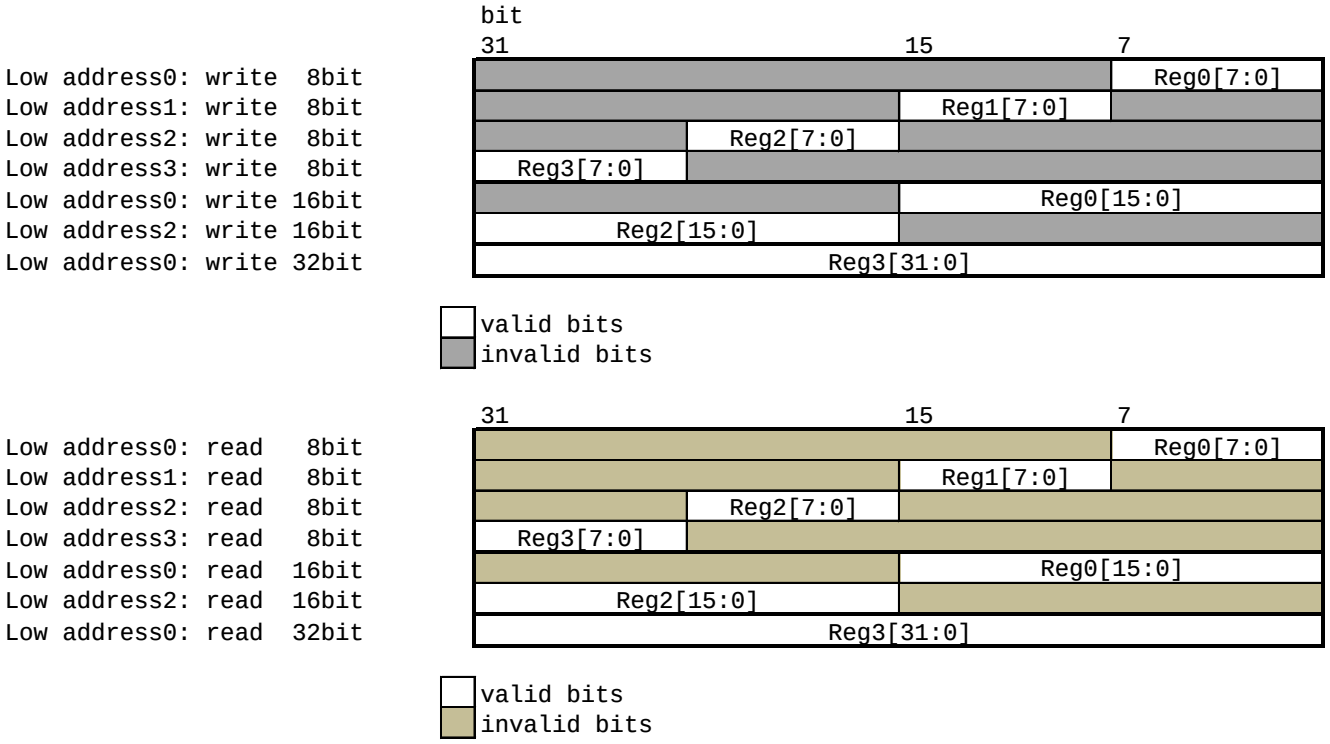

Figure 7.1 Bit location at register access

7.2. Precaution for Dynamic Clock Gating

When the dynamic clock gating is set, the following should be noted. When the interrupt generation and the interrupt cause are cleared, the count clock (**TIMCLK**) of the ADVTMR is necessary. The clear can be done only when the operation is enabled (Enable = 1 in the control register ***[ADVTMR_TnCONTROL]*** (**n** is a channel number: 0, 1, 2, or 3)).

7.3. Using SIOSC4M as the source clock for timer clock

Although SIOSC4M can be selected as the source of TIMCLK, frequency of SIOSC4M may have variation of 4 MHz +/- 3.5% due to temperature and/or voltage change. Note that the frequency variation is inherent in TIMCLK and affect timer operation such as interval time when SIOSC4M is used as the source of TIMCLK.

8. Revision History

Table 8.1 Revision History

Revision	Date	Description
0.1	2014-03-10	Newly released
0.2	2014-03-18	Corrected the register details.
0.3	2014-10-03	Corrected T1CONTROL values in Examples.
0.4	2014-11-17	Added the constraint about the clock frequency setting change.
0.5	2014-11-21	Modified Output Comparison procedure (5.4.2, 5.4.3)
1.0	2015-01-22	Official version
1.1	2015-11-24	Added Section 7.3
1.2	2018-02-05	Changed header, footer and the last page. Changed corporate name and descriptions. Modified Arm logo and descriptions.
1.3	2019-01-29	Added clearing capture register to DMA (Input Capture) operation procedure (5.7.1) Modified descriptions of the trademark and added trademarks. Revised the last page “RESTRICTIONS ON PRODUCT USE” and added URL.

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