

Application Processor Lite *ApP Lite*

TZ1000 Series

Reference Manual

MCU 12-bit Analog to Digital Converter

Revision 1.3

2018-02

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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Preface

This document provides the specification for the MCU 12-bit Analog to Digital Converter designed for the TZ1000 Series.

Intended Audience

This document is intended for the following users.

Driver software developers.

System designers

Conventions in this Document

- The following notational conventions apply to numbers:
 - Hexadecimal number: 0xABC
 - Decimal number: 123 or 0d123 - Only when it should be explicitly indicated that the number is decimal.
 - Binary number: 0b111 - It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- Low active signals are indicated with a name suffixed with "_N."
- A signal is asserted when it goes to its active level while it is deasserted when it goes to its inactive level.
- A set of multiple signals may be referred to as [m:n].
Example: S[3:0] indicates four signals, S3, S2, S1 and S0, collectively.
- In the text, register names are enclosed in brackets [].
Example: [ABCD]
- A set of multiple registers, fields or bits of the same type may be described collectively using "n."
Example: [XYZ1], [XYZ2], and [XYZ3] to [XYZn]
- A range of register bits are referred to as [m:n].
Example: [3:0] indicates a range from bit 3 to bit 0.
- Values set in registers are indicated using either a hexadecimal or binary number.
- Example: [ABCD].EFG = 0x01 (hexadecimal), [XYZn].VW = 1 (binary)
- Words and bytes are defined as follows:
 - Byte: 8 bits
 - Halfword: 16 bits
 - Word: 32 bits
 - Doubleword: 64 bits
- Register bit attributes are defined as follows:
 - R: Read-only
 - W: Write-only
 - W1C: Clear by write of 1 - A write of "1" clears the corresponding bit to 0.
 - W1S: Set by write of 1 - A write of "1" sets the corresponding bit to 1.
 - R/W: Read/Write
 - R/W0C: Read/Clear by write of 0
 - R/W1C: Read/Clear by write of 1
 - R/W1S: Read/Set by write of 1
 - RS/WC: Set by read/Clear by write - Set after a read and cleared after a data write.
- Registers only support word access unless otherwise specified.
- Any registers defined as Reserved in the text must not be rewritten. Also, any values read from such registers should not be used.
- Any bits for which default values are defined as "—" would return undefined values if read.
- When a data is written to a register containing both writable and read-only (R) bit fields, its default values should be written to read-only (R) bit fields. For any bit fields with default values defined as "—," refer to the definitions of the relevant register.
- Default values should be written to any reserved bit fields in a write-only register. For any bit fields with default values defined as "—," refer to the definitions of the relevant register.

1. Overview

This module is an AD converter which consists of an AD conversion part and a control logic part.
The feature is as follows.

- AD conversion type: Successive approximation ADC
- Resolution: 12 bits
- Number of channels: 4 channels
- ADC clock: 1 MHz to 12 MHz, selectable
- Conversion time: 19 clock cycles
- Conversion mode: Single mode and Scan mode
- FIFO capacity: 8 Words (12 bits) per channel
- Conversion data format: a signed or unsigned integer, selectable
- Adjustment of Conversion data
- Comparison of Conversion data

2. Block Diagram

2.1. Internal Block Diagram

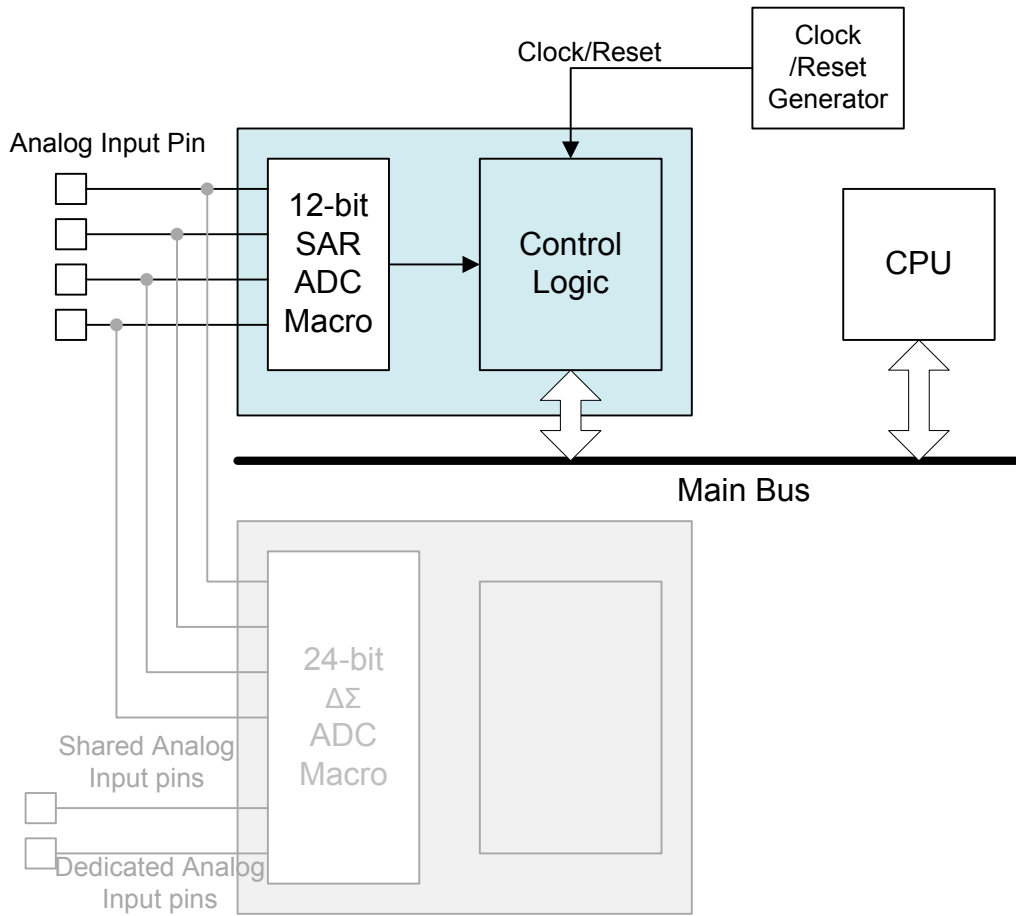


Figure 2.1 Connection between adcc12 and external blocks

2.2. Internal Blocks and Data Flow

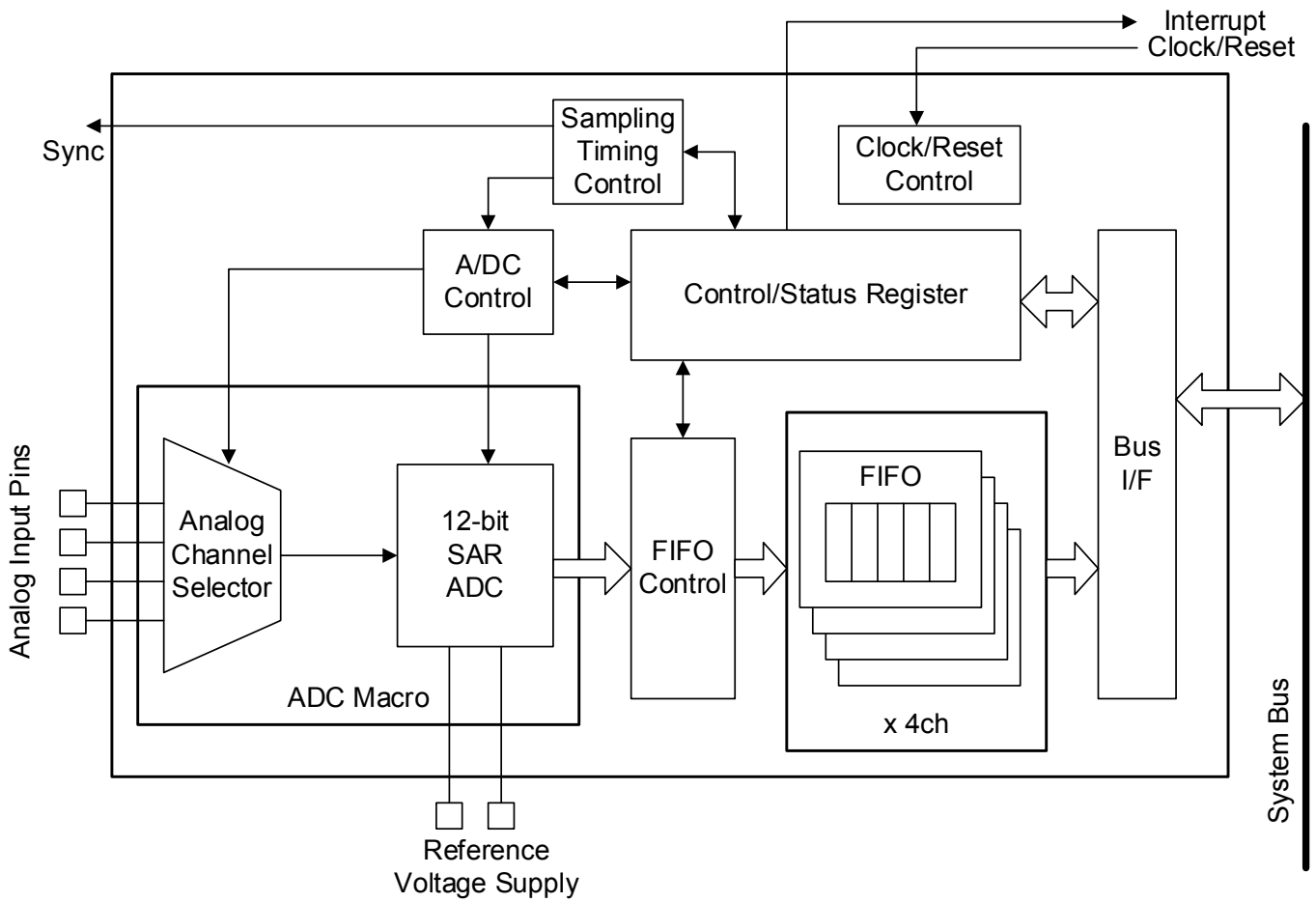


Figure 2.2 Adcc12 internal block diagram

2.3. External Pins

The following table shows the external pins related to this ADC controller.

Pin Name	I/O	Description
MCU_ADC_AIN0	I	Analog input channel 0 (*1)
MCU_ADC_AIN1	I	Analog input channel 1 (*1)
MCU_ADC_AIN2	I	Analog input channel 2 (*1)
MCU_ADC_AIN3	I	Analog input channel 3 (*1)
MCU_VREFH_ADC12	I	Higher reference voltage (3.3 V typ.)
MCU_VREFL_ADC12	I	Lower reference voltage (0 V)
MCU_AVDD33_ADC	POWER	Power supply for ADC macro (3.3 V typ.)
MCU_AVSS_ADC	POWER	Ground for ADC macro

*1: In order to sample an analog input signal accurately for ADC12, it is necessary for driving source of ADC12 to be satisfied with Case (a) or (b) as below.

Case (a) It's recommended to add more than 0.01 μF capacitor between MCU_ADC_AIN pin and MCU_AVSS_ADC.

Case (b) The output impedance of ADC driving source should be less than 250 Ω .

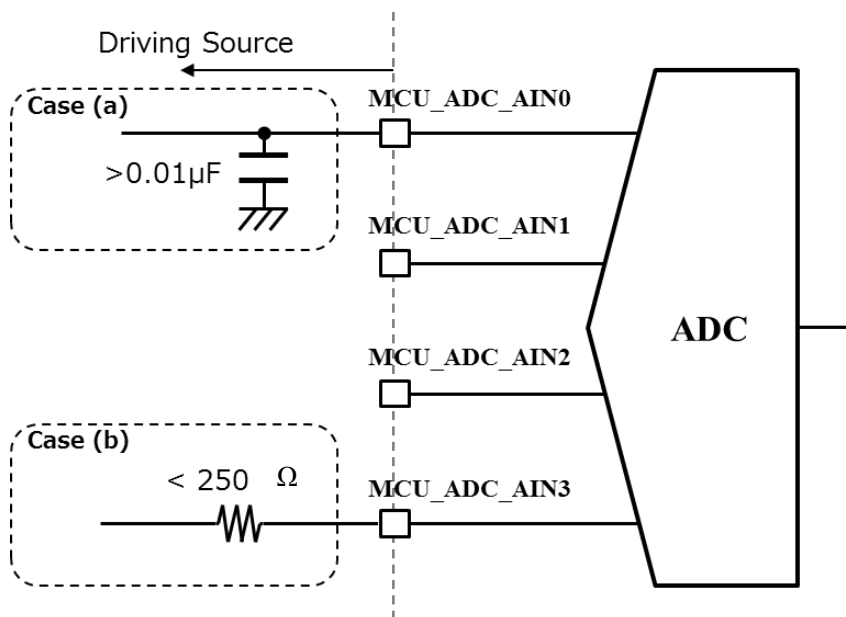


Figure 2.3 ADC12 driving source

3. Address map

Table 3.1 MCU 12-bit Analog to Digital Converter Register map

Register Name	Type	Width	Reset Value	Address Offset
MODESEL	RW	32	0x0000 0000	0x0000 0000
ADCCTL	RW	32	0x0000 0000	0x0000 0004
ADCINTEN	RW	32	0x0000 0000	0x0000 0008
ADCINTSTS	RW	32	0x0000 0000	0x0000 000C
SPLT_CTLCTL	RW	32	0x0000 0000	0x0000 0010
SPLT_PER	RW	32	0x0000 0000	0x0000 0014
SPLT_WAVCFG	RW	32	0x0000 0000	0x0000 0018
SPLT_SYNC_WAVCFG	RW	32	0x0000 0000	0x0000 001C
CMPDATA_0	RW	32	0x0000 0000	0x0000 0020
CMPDATA_1	RW	32	0x0000 0000	0x0000 0024
EXT_CTL	RW	32	0x0000 0000	0x0000 0040
CH0_MODE	RW	32	0x0007 0700	0x0000 0100
CH0_INTEN	RW	32	0x0000 0000	0x0000 0104
CH0_INTSTS	RW	32	0x0000 0000	0x0000 0108
CH0_OFFSET	RW	32	0x0000 0000	0x0000 010C
CH0_FIFOSTS	RO	32	0x0000 0000	0x0000 0110
CH1_MODE	RW	32	0x0007 0700	0x0000 0120
CH1_INTEN	RW	32	0x0000 0000	0x0000 0124
CH1_INTSTS	RW	32	0x0000 0000	0x0000 0128
CH1_OFFSET	RW	32	0x0000 0000	0x0000 012C
CH1_FIFOSTS	RO	32	0x0000 0000	0x0000 0130
CH2_MODE	RW	32	0x0007 0700	0x0000 0140
CH2_INTEN	RW	32	0x0000 0000	0x0000 0144
CH2_INTSTS	RW	32	0x0000 0000	0x0000 0148
CH2_OFFSET	RW	32	0x0000 0000	0x0000 014C
CH2_FIFOSTS	RO	32	0x0000 0000	0x0000 0150
CH3_MODE	RW	32	0x0007 0700	0x0000 0160
CH3_INTEN	RW	32	0x0000 0000	0x0000 0164
CH3_INTSTS	RW	32	0x0000 0000	0x0000 0168
CH3_OFFSET	RW	32	0x0000 0000	0x0000 016C
CH3_FIFOSTS	RO	32	0x0000 0000	0x0000 0170
CH0_DATA	RO	32	0x0000 0000	0x0000 0800-
CH1_DATA	RO	32	0x0000 0000	0x0000 0840-
CH2_DATA	RO	32	0x0000 0000	0x0000 0880-
CH3_DATA	RO	32	0x0000 0000	0x0000 08C0-

4. Function and Control

4.1. Function

This module converts the voltage of an analog input (MCU_ADC_AIN0 to 3) to digital data comparing with a reference voltage (MCU_VREFH_ADC12 - MCU_VREFL_ADC12).

Each channel has its own FIFO buffer and the result of the AD conversion is stored in the FIFO.

The AD conversion mode, the FIFO control, and others are selected by a control register.

3 conversion modes and 2 FIFO operation modes are supported. The mode is selected by a mode setting register.

4 analog input channels are supported. The channel is selected by a control register.

4.1.1. Conversion Mode

3 conversion modes as follows;

- Single mode: The conversion is done for the specified channel only.
- One-Time Scan mode: The conversion is done once for multiple channels in the order.
- Cyclic Scan mode: The conversion repeats for multiple channels in the order.

4.1.1.1. Single Mode

The conversion is done for the specified channel only.

[MODESEL].ConvMd selects the Single mode.

[MODESEL].ChSel specifies the channel.

When *[ADCCTL].Start* is set to 1, the conversion starts. When the conversion finishes, the conversion end interrupt is generated and the data is stored in the specified channel FIFO register.

When the conversion finishes, *[ADCCTL].Start* returns to 0.

The data in the FIFO can be read by the *[CHn_DATA]* read.

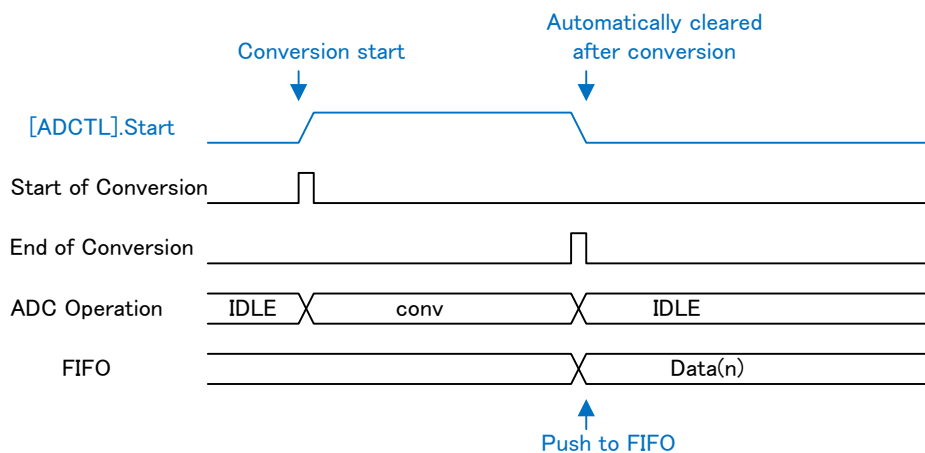


Figure 4.1 Single mode operation

Even though *[MODESEL].ChSel* is set to un-existing channel, the conversion is done and the ConvEnd interrupt is generated. The conversion data, however, is not stored because no FIFO register for the channel.

4.1.1.2. One-Time Scan Mode

The conversion for the specified multiple channels is done once in the order.

[MODESEL].ConvMd is set to One-Time Scan mode.

[CHn_MODE].ChEn is set to 1 for all target channels.

When **[ADCCTL].Start** is set to 1, the conversion starts. From Ch0 to Ch3 in the order, **[CHn_MODE]** is checked, and the conversion is done for the channel whose ChEn bit is 1. When the conversion finishes, the conversion end interrupt is generated and the data is stored in the target channel FIFO register.

The conversion for all target channels finishes, the Scan end interrupt is generated and **[ADCCTL].Start** returns to 0.

The data in the FIFO can be read by the **[CHn_DATA]** read.

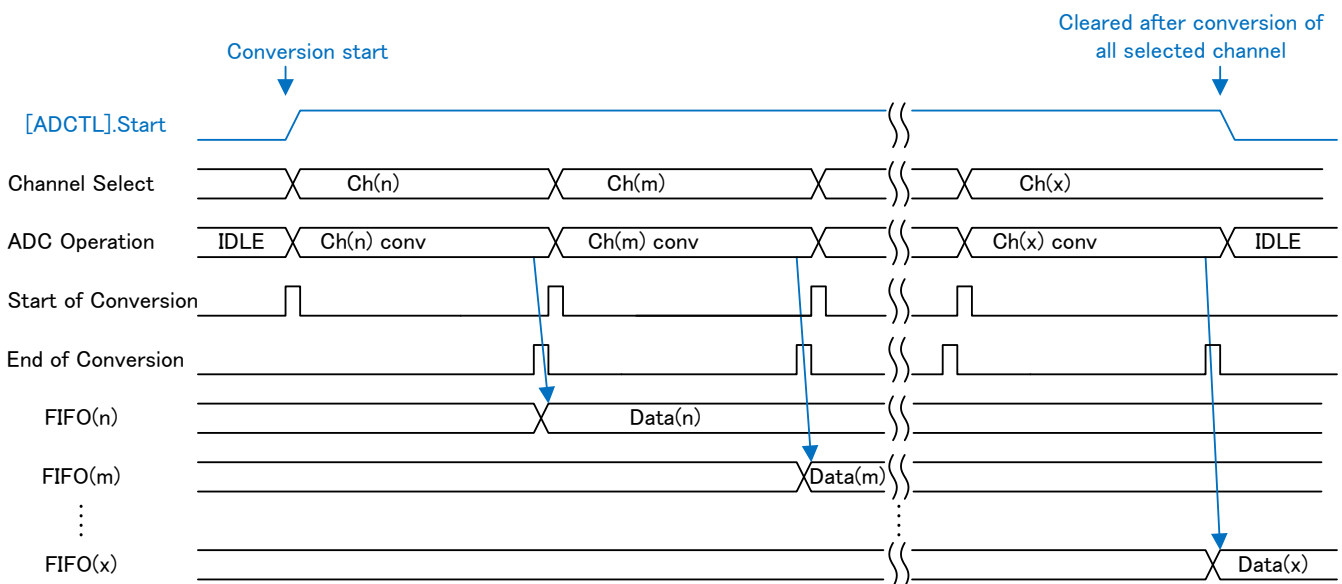


Figure 4.2 One-Time Scan mode operation

At least one channel should be enabled (**[CHn_MODE].ChEn** = 1). If **[CHn_MODE].ChEn** = 0 is set to all channels and the Scan mode starts, **[ADCCTL].Start** returns to 0 immediately, and the Scan end interrupt is generated.

4.1.1.3. Cyclic Scan Mode

The conversion for the specified multiple channels is done repeatedly in the order.

[MODESEL].ConvMd is set to the Cyclic Scan mode.

[CHn_MODE].ChEn is set to 1 for all target channels.

[ADCCTL].Start is set to 1. And the sampling timing signal starts the conversion. From Ch0 to Ch3 in the order, **[CHn_MODE]** is checked, and the conversion is done for the channel whose ChEn bit is 1. When the conversion finishes, the data is stored in the target channel FIFO register.

When the conversion is done for the Ch3, the ADC macro enters the IDLE state. The next sampling timing signal starts the conversion in the same manner of the previous one.

The channel which is not enabled (**[CHn_MODE].ChEn** = 0) is skipped.

When **[ADCCTL].Stop** is set to 1, the conversion stops after the completion of the current conversion under operating. Then, the Scan operation stops and **[ADCCTL].Start** returns to 0.

The data in the FIFO can be read by the **[CHn_DATA]** read.

The following chart shows an example of the conversion in the cycle order Ch(n) ⇒ Ch(m) ⇒ ... ⇒ Ch(x).

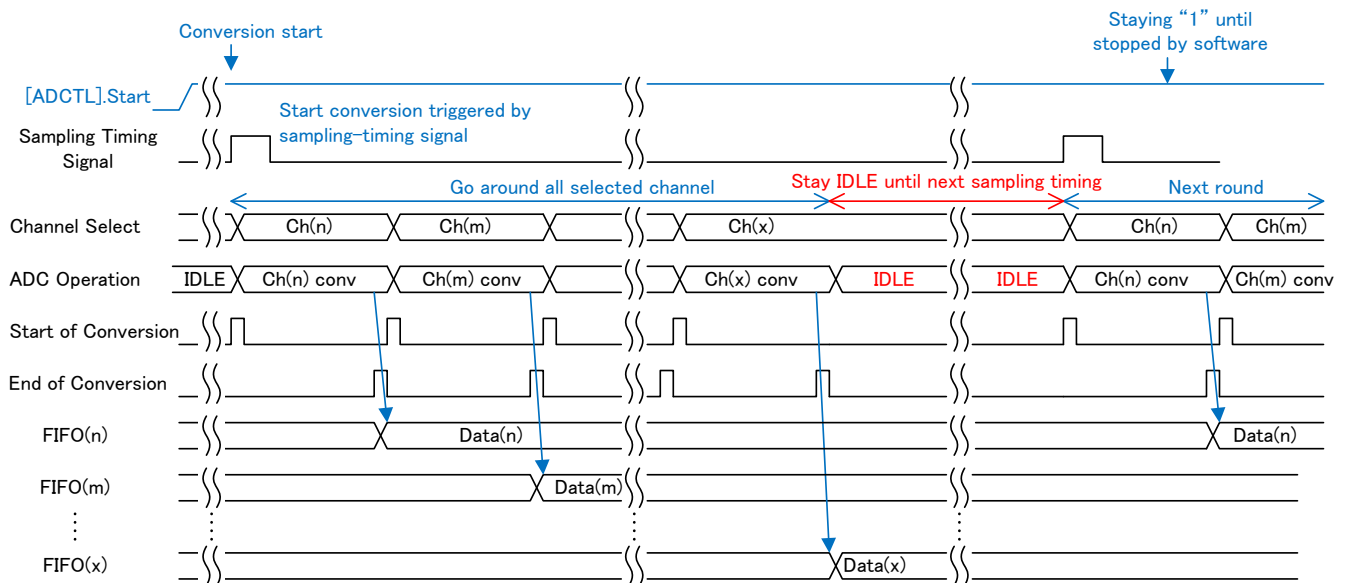


Figure 4.3 Cyclic Scan mode operation

4.1.1.4. Conversion Stop

In the One-Time and Cyclic Scan modes, if the conversion is forced to stop, $[ADCCTL].Stop$ should be set to 1. When this bit is written to 1, the current conversion under operating completes and the Scan operation stop. Then, $[ADCCTL].Start$ returns to 0, and the Scan end interrupt is generated.

4.1.1.5. AD Conversion Timing

Before the ADC starts the conversion, ADC macro is in the power-down state. When it starts to operate, some wait time is necessary for the macro to enable the conversion after its power-up. The wait time is set by $[MODESEL].PupToChSet$ and $[MODESEL].ChSetToStart$.

$[MODESEL].PupToChSet$ sets the interval time from the power-up of the ADC to the setting of the input channel. $[MODESEL].ChSetToStart$ sets the interval time from the setting of the input channel to the start of the AD conversion. The setting value is the cycle counts of the reference clock. The reference clock of this ADC is the ADC clock.

The AD conversion operation is shown in the following figure.

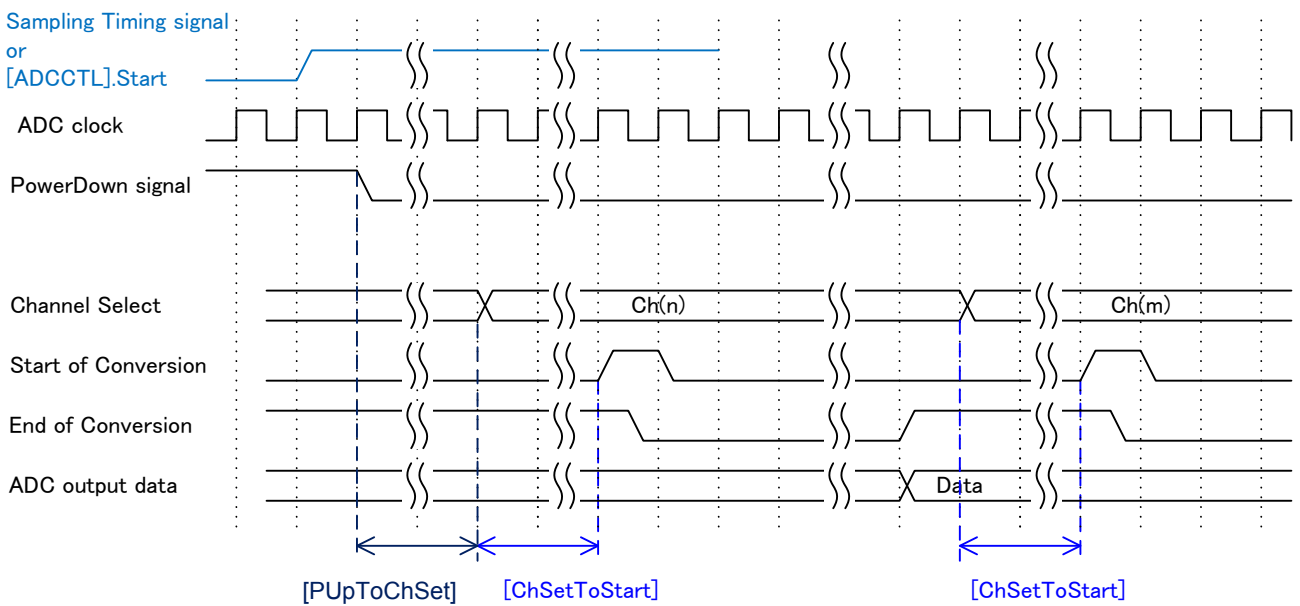


Figure 4.4 AD conversion operation

4.1.2. FIFO Operation

An FIFO buffer is implemented for each channel to store the conversion data. The stage number of the FIFO is 8 Words (12 bits). The FIFO data is read by the $[CH_n_DATA]$ read.

The AD conversion data is stored sequentially into the FIFO. When the FIFO data count reaches the value set by $[CH_n_MODE].WaterMark$, the WaterMark interrupt is generated. This interrupt is used to read all the conversion data at once. Even though the interrupt is cleared, the interrupt is re-generated if more data than the value set by $[CH_n_MODE].WaterMark$ are left in the FIFO. It is recommended that when WaterMark interrupt is detected, all the FIFO data should be read out. The data count of the FIFO can be checked with the $[CH_n_FIFOSTS]$ register.

When the data count becomes the FIFO stage number, the FIFO Full interrupt is generated. And, when the FIFO is empty and it is read, the FIFO underrun interrupt is generated.

Two FIFO operation modes are supported; Stream mode and FIFO Stop mode. The mode selection is done by $[MODESEL].FIFOMd$.

- Stream mode

When the FIFO is full and a new data comes, the previous data is discarded and the new data is stored.

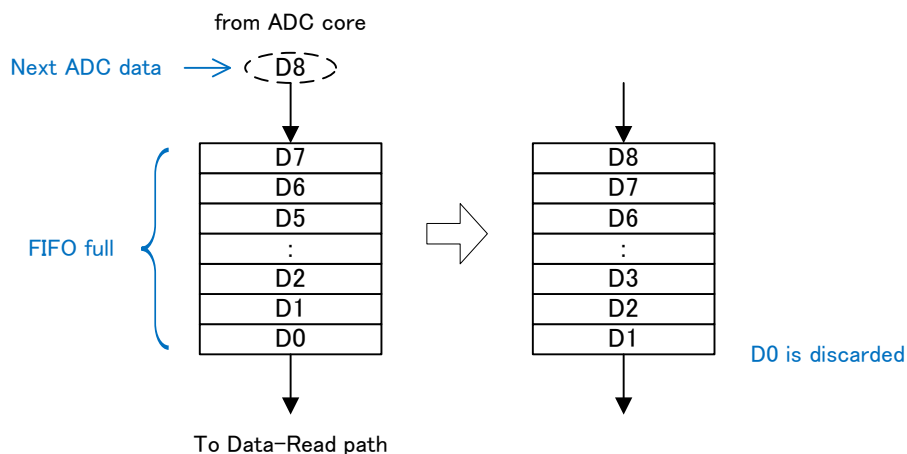


Figure 4.5 Stream mode

- FIFO Stop mode

When the FIFO is full and a new data comes, the new data is not stored and discarded.

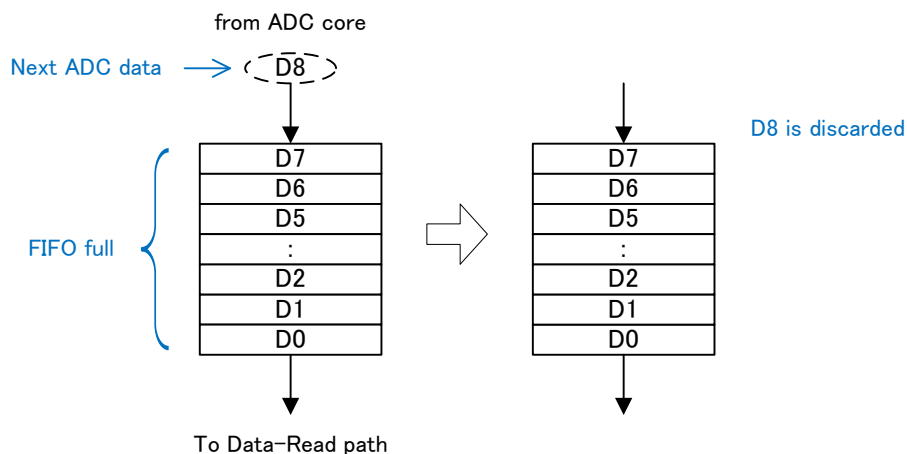


Figure 4.6 FIFO Stop mode

4.1.3. Sampling

4.1.3.1. Sampling Generation Counter

A 16-bit counter is implemented to generate the periodical sampling timing in the Cyclic Scan mode. An expected sampling timing signal can be obtained by using this counter. This signal determines the sampling rate in the Cyclic Scan mode.

The block diagram of the sampling timing generation counter is shown in the following figure.

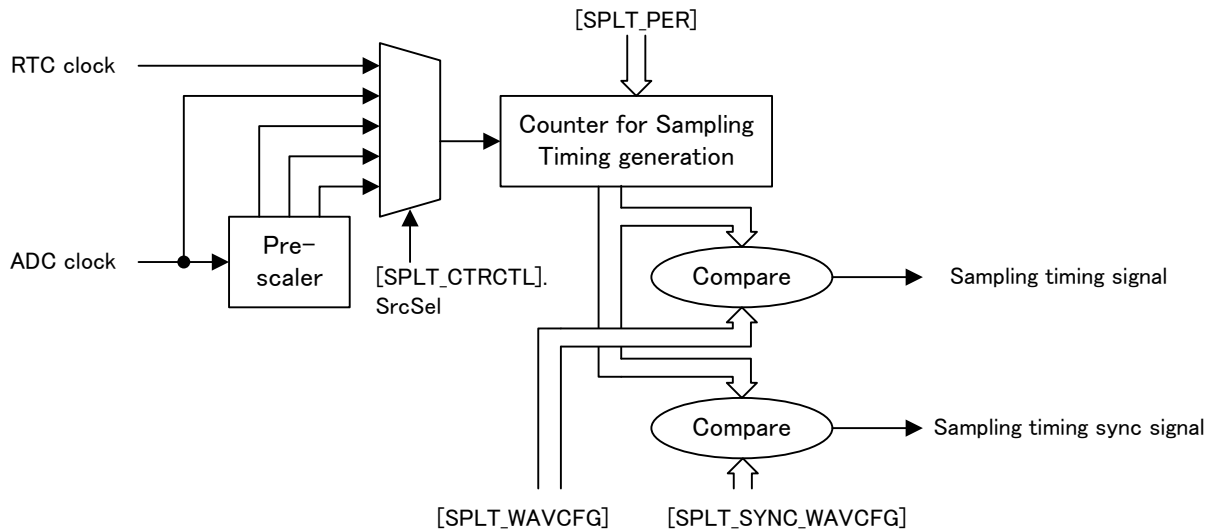


Figure 4.7 Block diagram of sampling timing generation counter

For the counter input clock, a prescaler which divides the ADC clock and a selector of the counter source clock are implemented in this module.

The counter source clock is selected by $[SPLT_CTRCTL].SrcSel$ among the ADC clock, the prescaler output, and the RTC clock. The counter period is set to $[SPLT_PER]$ register.

The prescaler and the counter start when $[ADCCTL].Start$ is set to 1 in the Cyclic Scan mode.

The $[SPLT_WAVCFG]$ register generates the sampling timing signal. When the counter value becomes the $[SPLT_PER]$ value, the sampling timing signal is set to 1. When the counter value becomes the period time set in the $[SPLT_WAVCFG]$ register, the sampling timing signal returns to 0.

The $[SPLT_SYNC_WAVCFG]$ register generates a signal which is synchronous to the sampling timing signal. This synchronous signal is outputted to the external and is used for arbitrary application.

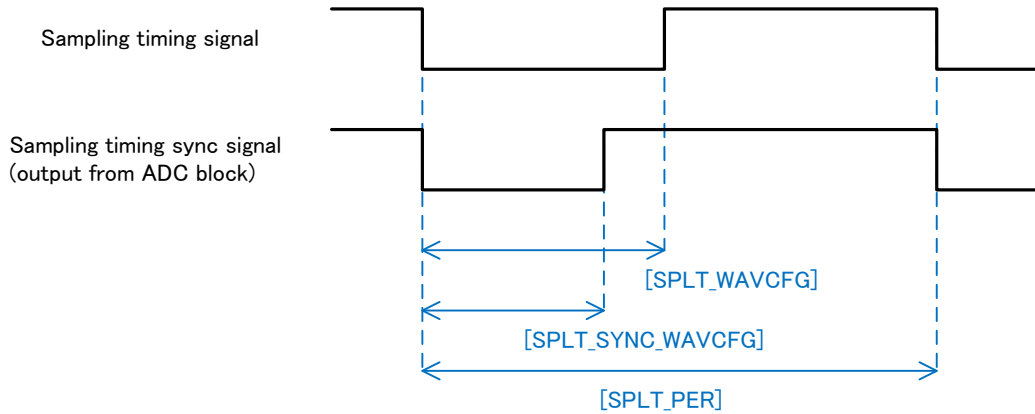


Figure 4.8 Sampling timing signal

The sampling timing synchronous signal is controlled by the *[EXT_CTL]* register to be output to the external.

When *[EXT_CTL].SelExt* = 10 or 11 is set, the synchronous signal is output to the external. If *[EXT_CTL].SelExt* = 00 is set, the output is fixed to 0, and, if *[EXT_CTL].SelExt* = 01 is set, the output is fixed to 1.

The *[EXT_CTL].InvExt* can select between the inverse and non-inverse of the output.

[EXT_CTL].InvExt = 1 selects the inverse output of the sampling timing synchronous signal.

The sampling timing synchronous signal is connected to the BGR in this product. When the signal is High, the amplifier monitoring the BGR is enabled, and the internal reference voltage is output from the BGR_OUT pin.

4.1.3.2. Sampling Rate

In the Cyclic Scan mode, the conversion is triggered by the signal generated by the sampling timing generation counter. This signal is the timing when the AD conversion starts the AD conversion. The conversion is cyclic, so the frequency of the signal determines the sampling rate for each channel.

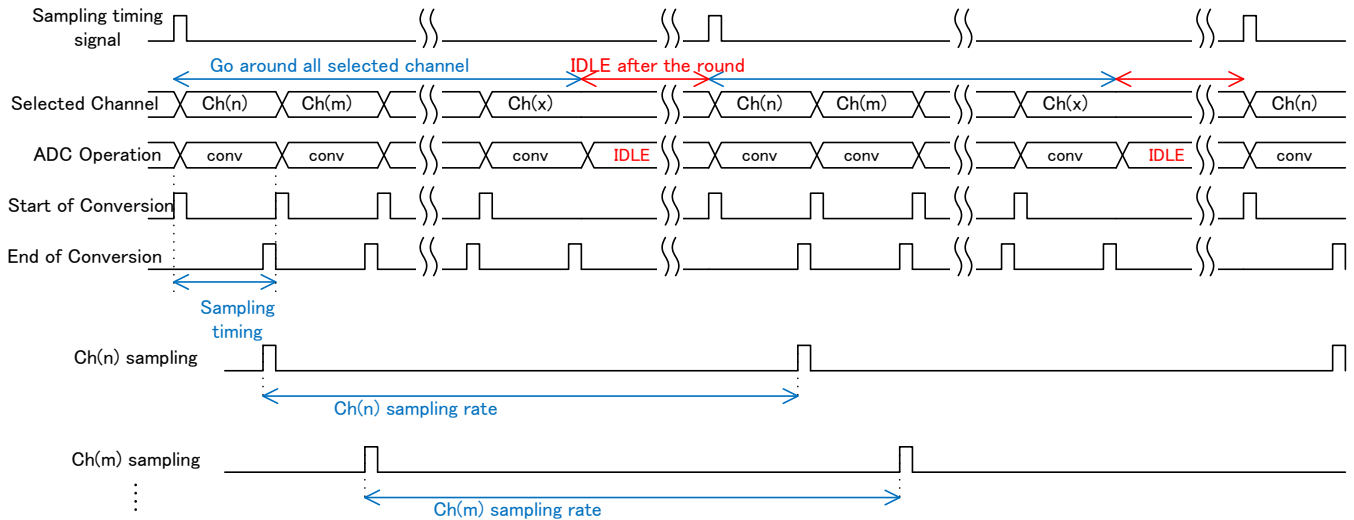


Figure 4.9 Sampling rate

The channel which is not set to enable ($[CHn_MODE].ChEn = 0$) skips the conversion. For example, if Ch0, 1, and 3 are enabled and Ch2, 4 to 15 are disabled, the conversion is done for Ch0, 1, and 3 (only 3 times). (Note: This product has only 4 channels; Ch0 to 3.)

The following table shows the relation between the value of the sampling timing setting register and the period of the sampling timing signal at 12 MHz of the ADC clock.

Table 4.1 Sampling timing setting value and the period

[SPLT_CTL]. SrcSel Value	Source Clock	[SPLT_PER] Value		
		Min 0x0001	Max 0xFFFF	Resolution
000	12 MHz	166.7 ns	5.46 ms	83.3 ns
001	3 MHz	666.7 ns	21.8 ms	333.3 ns
010	750 kHz	2.67 μ s	87.4 ms	1.33 μ s
011	187.5 kHz	10.67 μ s	349.5 ms	5.33 μ s
100	32.768 kHz	61.04 μ s	2.00 s	30.52 μ s

The period of the sampling timing signal should be greater than the following value.

(AD conversion time per channel in the ADC macro + $[MODESEL].ChSetToStart$ value)

* (enabled channel number) + α

AD conversion time per channel: 19 cycles in this 12-bit ADC.

α : (The overhead time for the ADC power-down control)

= $[MODESEL].PUptoStart$ value + 5

Unless this condition is satisfied, the operation is not guaranteed.

And, the High width of the sampling timing signal should be equal to or greater than two cycles of the ADC clock.

4.1.3.3. Down Sampling Function

The AD conversion is done for the selected channel every sampling timing. The down-sampling is supported for each channel.

The setting in `[CHn_MODE].DownSpl` specifies the sampling once out of n times (n = 1 to 8).

The sampling rate can be set for each channel independently.

The following figure shows the example that every one sampling out of two times is skipped for the channel n (Ch(n)).

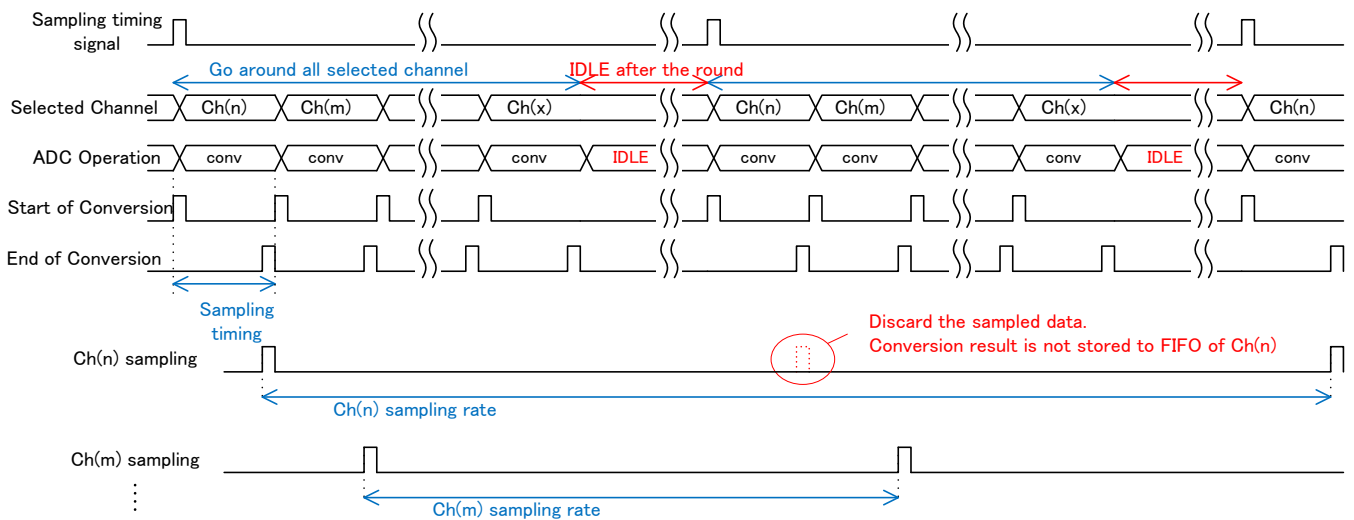


Figure 4.10 Sampling thinning operation

The down-sampling function executes the AD conversion but does not store the conversion data to the FIFO. The comparison of the conversion data does not execute, either.

When the sampling is skipped, the channel conversion end interrupt (ChEocEn) is not generated, but the conversion end interrupt (ConvEnd) is generated. When the Scan mode is forced to stop during the conversion and the last conversion is the skipped timing, the Scan end interrupt is generated.

4.1.4. Interrupt

The interrupt causes in the ADC are as follows.

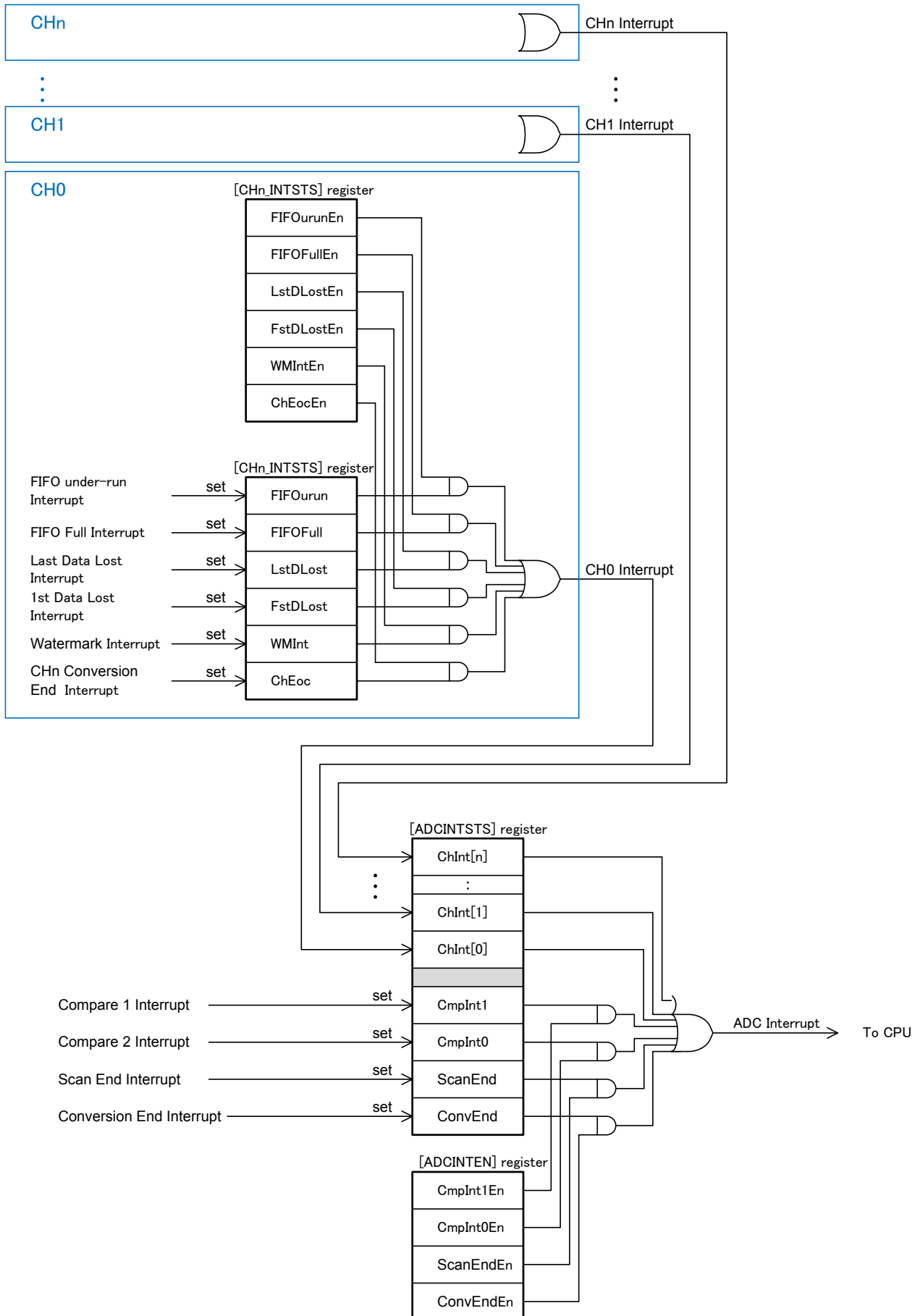
- Conversion end interrupt:
When the AD conversion finishes, this interrupt is generated.
- Scan end interrupt:
When the Scan operation (One-Time or Cyclic) completes for all the enabled channels, this interrupt is generated.
- Conversion value comparison interrupt:
The data stored into the FIFO is compared with the comparison data register *[CMPDATA_m]* (m=0 or 1). The interrupt is generated depending on the comparison result, bigger or smaller. The target channel is selected by *[CMPDATA_m].CmpCh*. This interrupt is generated when the conversion value is bigger if *[CMPDATA_m].CmpSel* is set to 0. If the register value is 1, the interrupt is generated when the conversion value is smaller.

The following interrupt causes for each channel are supported.

- Channel conversion end interrupt:
The conversion for the target channel completes. Then, this interrupt is generated when the conversion data is stored to the FIFO.
- WaterMark interrupt:
When the FIFO data count reaches the *[CHn_MODE].WaterMark* value, this interrupt is generated.
- 1st Data Lost interrupt (Stream mode only):
When the FIFO is full and a new data is stored, the oldest data is discarded in the Stream mode. And this interrupt is generated.
- Last Data Lost interrupt (the FIFO Stop mode only):
When the FIFO is full and a new data comes, the data is discarded in the FIFO stop mode. And this interrupt is generated.
- FIFO Full interrupt:
When the FIFO becomes full, this interrupt is generated.
- FIFO underrun interrupt:
When the FIFO is empty and the FIFO is read, this interrupt is generated. The FIFO has no change even the interrupt is generated.

Each interrupt cause can be enabled or disabled by the interrupt enable register. Even if it is disabled, the interrupt flag in the status register can be set. So the status can be checked by polling. Every interrupt can be cleared by writing 1 to the correspond flag bit. If the interrupt cause still remains, the interrupt is asserted again after its clear. (For example, when the WaterMark interrupt is generated and the data count is still more than the WaterMark value in the FIFO, the WaterMark interrupt is asserted again after the previous interrupt is cleared.)

All interrupt requests are Ored to one signal which is issued as an interrupt output to the external. The configuration diagram of the interrupt is shown in the following figure.



4.1.5. DMA Interface

The interface to the DMA controller supports the DMA request signal (output) and DMA acknowledge signal (input) for each channel.

The DMA request signal is enabled or disabled by $[CHn_INTEN].DMAEn$.

When the FIFO data count becomes the $[CHn_MODE].WaterMark$ value, the WaterMark interrupt is generated and the DMA request is also asserted simultaneously. When the DMA acknowledge is received, the DMA request is deasserted.

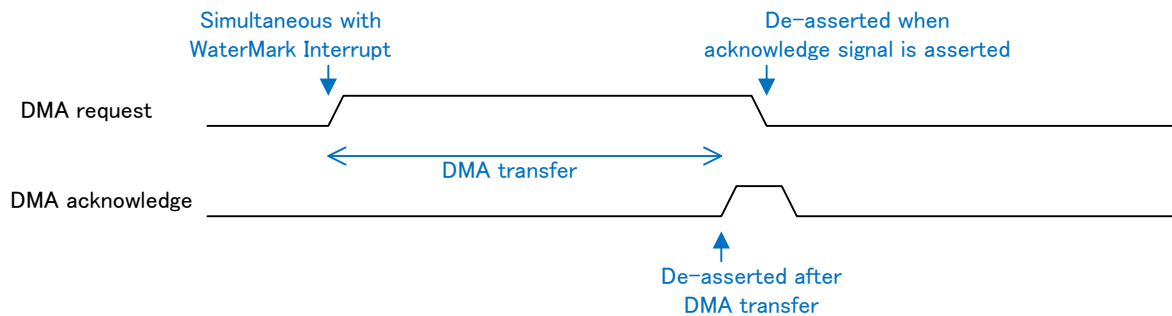


Figure 4.11 DMA interface signals

When the FIFO data count reaches the WaterMark value, the DMA request is asserted. The assertion continues until the DMA acknowledge is received. After the DMAC stops, the DMA request may remain asserted if there are data left in the FIFO. In this case, the FIFO data can be cleared by reading it to discard. And the asserted DMA request is cleared (deasserted) by writing 1 to $[CHn_INTSTS].DMAreq$.

4.1.6. Conversion Data Format

The ADCmacro's conversion data format is the zero scale of 0x000, the full scale of 0xFFFF, and unsigned integers. Sometimes it is necessary that $(VREFH-VREFL)/2$ should be 0 level. For that, the data format conversion is supported by this controller.

The selection of a signed or unsigned format is done by $[CHn_MODE].DtFmt$.

If the unsigned integer format is selected, the conversion data is directly stored to the FIFO. When the $[CHn_DATA]$ register is read, the reserved bits return 0.

If the signed integer format is selected, the MSB of the conversion data is reversed and stored to the FIFO. When the $[CHn_DATA]$ register is read, the reserved bits return 0.

Table 4.2 Conversion data format

ADC Analog Input	ADC Macro Conversion Data	DtFmt = 0		DtFmt = 1	
		FIFO Data	Register Read	FIFO Data	Register Read
Zero Scale	0x000	0x000	0x0000	0x800	0x8000
:	:	:	:	:	:
$(VREFH-VREFL)/2$	0x7FF	0x7FF	0x7FF0	0xFFF	0xFFF0
	0x800	0x800	0x8000	0x000	0x0000
:	:	:	:	:	:
Full Scale	0xFFF	0xFFF	0xFFF0	0x7FF	0x7FF0

4.1.7. Conversion Data Adjustment

The conversion result of the ADC macro can be adjusted before it is stored into the FIFO.

When this function is enabled, the value set in *[CH_n_OFFSET]* is added to the conversion data, and it is stored to the FIFO.

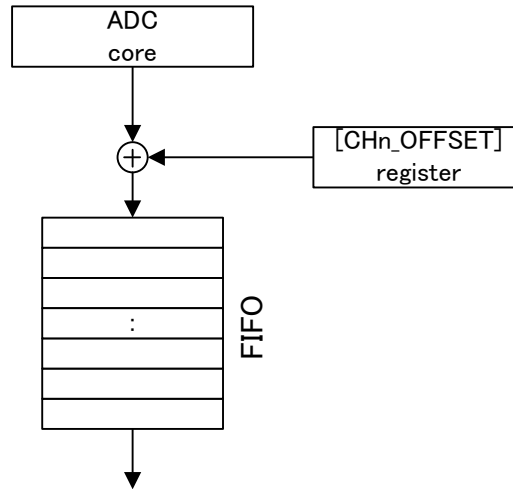


Figure 4.12 Conversion data adjustment

The adjusting function is enabled by *[CH_n_MODE].OfsEn*.

The offset data is an 8-bit and signed integer. The offset data is sign-extended and added to the conversion data that is 24-bit. If the calculation result exceeds the range of the conversion, the upper limit data or the lower limit data is stored into the FIFO.

- When *[CH_n_MODE].DataFmt = 0*:
 - (Calculation data) > 0xFFF ⇒ FIFO stores 0xFFF.
 - 0x000 ≤ (Calculation data) ≤ 0xFFF ⇒ FIFO stores the calculation data.
 - (Calculation data) < 0x000 ⇒ FIFO stores 0x000.

- When *[CH_n_MODE].DataFmt = 1*:
 - (Calculation data) > +0x7FF ⇒ FIFO stores 0x7FF.
 - 0x800 ≤ (Calculation data) ≤ 0x7FF ⇒ FIFO stores the calculation data.
 - (Calculation data) < -0x800 ⇒ FIFO stores 0x800.

4.1.8. Conversion Data Comparison

The data stored into the FIFO is compared with the compare data register $[CMPDATA_m]$ ($m = 0$ and 1). An interrupt is generated depending on the result of the magnitude comparison.

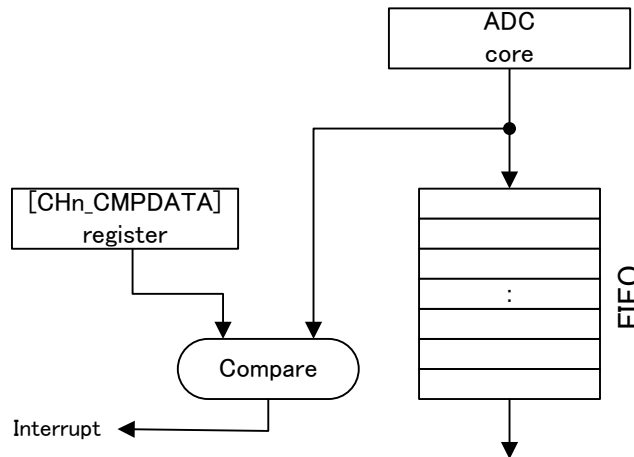


Figure 4.13 Conversion Data Comparison

This function is enabled by $[CMPDATA_m].CmpEn$. The target channel is selected by $[CMPDATA_m].CmpCh$. The condition of the interrupt generation is selected by $[CMPDATA_m].CmpSel$ as follows.

$[CMPDATA_m].CmpSel = 0 \Rightarrow$ Stored data $> [CMPDATA_m]$: Interrupt generation
 $[CMPDATA_m].CmpSel = 1 \Rightarrow$ Stored data $< [CMPDATA_m]$: Interrupt generation

The comparison is done after the data format conversion and the adjustment described in 4.1.6 Conversion Data Format and 4.1.7 Conversion Data Adjustment, respectively.

In the FIFO Stop mode, when the FIFO is full, the conversion data is not stored into the FIFO, but the comparison is executed.

4.1.9. Starting AD Conversion by External trigger

Beside setting the $[ADCCTL]$ register, AD conversion can be started by external event trigger. Please see EVM specification for the details of event sources and way to setting event trigger.

The event trigger has the same effect as setting "1" to $[ADCCTL].Start$.

4.2. Power Management

The operation of each power mode is shown as follows.

- SLEEP0/1: Normal operation
- SLEEP2/WAIT: The AD conversion is disabled because the bus clock and the ADC clock stop. Before transition to this mode, it should be confirmed that AD conversion operation is stopped by reading the *[ADCCTL]* register. On returning from this mode, the module comes back to the same state before the transition.
- RETENTION: The AD conversion is disabled because the bus clock and the ADC clock stop. Before transition to this mode, it should be confirmed that AD conversion operation is stopped by reading the *[ADCCTL]* register.
The ADC should be in the reset state in this mode. Before entering this mode, the *[SRST_ON_PA12]* register in the PMU should be set to assert the reset to the ADC. When returning from this mode, the *[SRST_OFF_PA12]* register should be set to deassert the reset.
- RTC/STOP: The ADC controller is disabled because the controller is not supplied with the power. Before transition to this mode, it should be confirmed that AD conversion operation is stopped by reading the *[ADCCTL]* register. And it is also recommended that the FIFO data should be read out and other necessary procedure should be done before the transition. When returning from this mode, the registers are initialized and the re-setting is necessary before starting the operation again.

4.3. Start-up and Stop Procedure

4.3.1. Clock and Reset Settings

Two supplies of the clock and reset are supported for this ADC controller; the Bus clock and the ADC clock. These clocks are asynchronous each other. The two reset signals are synchronized to the clocks, respectively.

These clocks and reset signals are controlled by the PMU (Power Management Unit).

The frequencies of the bus clock and the ADC clock can be selected outside of this module. Bus clock (APB clock) is the clock divided by the value set in *[PRESCAL_MAIN].PSEL_CD_PPIER0*, and the source clock selected by *[CSM_MAIN].CSMSEL_MAIN*. ADC clock is the clock divided by the value set in *[PRESCAL_ADCC12A].PSEL_CD_ADCC12A*, and the source clock selected by *[CSM_ADCC12A].CSMSEL_ADCC12A*. When you change the ADC clock frequency and/or clock source, ADC operation should be disabled. For details of the frequency setting, refer to the PMU specification.

The all combinations of frequencies of the bus clock and the ADC clock are not selectable. The following table shows the combinations available.

		Bus Clock						
		12 MHz	8 MHz	6 MHz	4 MHz	3 MHz	2 MHz	1 MHz
ADC Clock	16 MHz	—	—	—	—	—	—	—
	12 MHz	✓	—	—	—	—	—	—
	8 MHz	✓	✓	—	—	—	—	—
	6 MHz	✓	✓	✓	—	—	—	—
	4 MHz	✓	✓	✓	✓	—	—	—
	3 MHz	✓	✓	✓	✓	✓	—	—
	2 MHz	✓	✓	✓	✓	✓	✓	—
	1 MHz	✓	✓	✓	✓	✓	✓	✓

The ADC clock is the source clock of the AD conversion time and the sampling rate in the Cyclic Scan mode. Refer to 4.1.3.2 Sampling Rate.

4.3.2. Start-up Procedure

The start-up procedure of this ADC controller after the power-on of this product is shown as follows.

- (1) Set the power state of the PA12 domain to power-on.
 - Set the *[POWERDOMAIN_CTRL_MODE].PDMODE_PA12* bit to 0b00.
- (2) Start the sequence of power domain control.
 - Set the *[POWERDOMAIN_CTRL].START_PA12* bit to 1.
- (3) Check the finish of power state changing.
 - Check the *[POWERDOMAIN_CTRL].START_PA12* bit is 0.
- (4) Start supply of clocks to the controller.
[CG_OFF_POWERDOMAIN].CG_PA12 is set to 1, which starts to supply this ADC controller with the clock. The combination available between the bus clock and the ADC clock is shown in 4.3.1 Clock and Reset Settings.
- (5) Release reset of the controller
[SRST_OFF_POWERDOMAIN].SRST_PA12 is set to deassert the reset to this ADC controller.

For the PMU (Power Management Unit) registers, refer to the PMU specification.

4.3.3. Stop Procedure

The stop procedure of this controller is shown as follows.

- (1) Stop ADC controller:
If the ADC conversion is executing, wait until *[ADCCTL].Start* and *[ADCCTL].Stop* become 0. If the Scan mode is forced to stop, *[ADCCTL].Stop = 1* is set to stop the AD conversion. Then, confirm that *[ADCCTL].Start* and *[ADCCTL].Stop* become 0.
- (2) Reset controller:
[SRST_ON_POWERDOMAIN].SRST_PA12 is set to assert the software reset to this ADC controller.
- (3) Stop supply of the clocks to the controller:
[CG_ON_POWERDOMAIN].CG_PA12 is set to stop supplying the clock to this ADC controller.

If power domain of PA12 should be shut-off, follow the next step.

- (4) Set the power state of the PA12 domain to power-off.
 - Set the *[POWERDOMAIN_CTRL_MODE].PDMODE_PA12* bit to 0b01.
- (5) Start the sequence of power domain control.
 - Set the *[POWERDOMAIN_CTRL].START_PA12* bit to 1.

4.4. Precaution for Usage

- (1) The following registers should be set before the start of the AD conversion (before *[ADCTL].Start = 1* is set).
During the AD conversion (*[ADCTL].Start = 1*) the registers should not be updated.

Mode setting register *[MODESEL]*

AD conversion interrupt control register *[ADCINTEN]*

Sampling timing generation control register *[SPLT_CTRCTL]*

Sampling period setting register *[SPLT_PER]*

Sampling timing signal waveform setting register *[SPLT_WAVCFG]*

Sampling timing synchronous signal waveform setting register *[SPLT_SYNC_WAVCFG]*

Comparison data setting register *[CMPDATA_m]* (m = 0 and 1)

External output signal control register *[EXT_CTL]*

Channel n mode setting register *[CHn_MODE]* (n = 0 to 3)

Channel n interrupt control register *[CHn_INTEN]* (n = 0 to 3)

Channel n conversion data offset *[CHn_OFFSET]* (n = 0 to 3)

- (2) The register access should be done in 32 bits unit except the *[CHn_DATA]* register. 8-bit or 16-bit write access causes to write unexpected data to the bits other than the corresponding bits. 8-bit or 16-bit read access can read the corresponding bits correctly.
The *[CHn_DATA]* register should be accessed with units of 16 bits. This register has the FIFO structure. A read access to the FIFO changes the access to the next stage in the FIFO. This is the same as in the 8-bit access, so the bits other than the accessed 8 bits are discarded. When the read access is units of 32 bits, the read data of the upper 16 bits are the same as the lower 16 bits.
- (3) This product includes two AD converters, adcc12 and adcc24. These converters share the analog input pins. The analog input pins are ADC_AIN0 to 5. The correspondence between the input pins and the channels of adcc12 or adcc24 is shown in the following table.

Input Pin	adcc12	adcc24
ADC_AIN0	ch0	ch0
ADC_AIN1	ch1	
ADC_AIN2	ch2	ch1
ADC_AIN3	ch3	
ADC_AIN4	—	ch2
ADC_AIN5	—	

The input pins are used by adcc12 and adcc24 in the 3 ways as follows.

Input Pin	Case1	Case2	Case3
ADC_AIN0	adcc12 ch0	adcc12 ch0	adcc24 ch0
ADC_AIN1	adcc12 ch1	adcc12 ch1	
ADC_AIN2	adcc12 ch2	adcc24 ch1	adcc24 ch1
ADC_AIN3	adcc12 ch3		
ADC_AIN4	adcc24 ch2	adcc24 ch2	adcc24 ch2
ADC_AIN5			

- (4) Using SIOSC4M as the source clock for ADC clock
Although SIOSC4M can be selected as the source of ADC clock, frequency of SIOSC4M may have variation of $4\text{ MHz} \pm 3.5\%$ due to temperature and/or voltage change. Note that the frequency variation is inherent in the sampling rate when the source of ADC clock is SIOSC4M and ADC clock is used to generate the sampling rate.

5. Details of Registers

5.1. MODESEL

MODESEL				
Description	Mode set register			
Address Region	adcc12	Type:	RW	
Offset	0x0000 0000			
Physical address View0	0x4004 8000			
Physical address View1	-			
Bitfield Details				
Bits	Name	Description	Access	Reset
31:28	ChSetToStart	ADC Channel Select to Conversion Start Sets a period between ADC macro channel setting (switching) and start of conversion. The period is the number of cycles given by: (Settings) x reference clock *) Reference clock is ADC clocks.	RW modify	0x0
27:24	PUpToChSet	ADC PowerUp to Channel Set Sets a period between ADC macro power down release and channel set (start of conversion if ChSetToStart setting is "0") The period is the number of cycles given by: (Settings + 2) x reference clock *) Reference clock is ADC clocks.	RW modify	0x0
23:14	Reserved	-	-	-
13:12	Reserved	-	-	-
11:10	Reserved	-	-	-
9:8	ChSel	Channel selection Sets the channel number that the AD conversion is made. Used only when conversion mode is Single 00: Ch0 01: Ch1 10: Ch2 11: Ch3	RW modify	0x0
7:5	Reserved	-	-	-
4	FIFOMd	FIFO mode Sets the method of storing conversion data in FIFO. 0: Stream Discards the oldest data and stores the latest data in FIFO when FIFO is full. 1: FIFO stop Retains data in FIFO and discards the latest data when FIFO is full.	RW modify	0
3:2	Reserved	-	-	-
1:0	ConvMd	Conversion mode Sets ADC conversion modes. 00: Single Performs conversion of a channel specified by ChSel. 01: One-time scan	RW modify	0x0

		<p>Sequentially performs conversion for channels enabled by each channel set register. Comes to a stop after one round of conversions.</p> <p>10: Cyclic scan</p> <p>Sequentially performs conversion for channels enabled by each channel set register. Repeats conversion operation until a stop instruction is issued by a control register.</p> <p>11: Reserved</p>		
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5.2. ADCCTL

ADCCTL				
Description	AD conversion control register			
Address Region	adcc12	Type:	RW	
Offset	0x0000 0004			
Physical address View0	0x4004 8004			
Physical address View1	-			
Bitfield Details				
Bits	Name	Description	Access	Reset
31:2	Reserved	-	-	-
1	Stop	<p>Stop conversion</p> <p>Forcibly stops ADC conversion operation.</p> <p>[For read operation]</p> <p>0: ADC in operation or going to stop</p> <p>1: ADC conversion is stopped</p> <p>[For write operation]</p> <p>0: -</p> <p>1: Starts AD conversion stop operation</p> <p>Writing "1" to this bit can stop AD conversion. After conversion operation being executed has been completed, ADC comes to a stop and this bit is returned to "0".</p> <p>When ADC conversion is being stopped (Start bit is "0"), "1" cannot be written to this bit.</p> <p>"0" cannot be written to this bit (Even if "0" is written, stop operation cannot be cancelled.)</p>	RW oneToSet	0
0	Start	<p>Start of conversion</p> <p>Starts ADC conversion</p> <p>[For read operation]</p> <p>0: ADC conversion is stopped</p> <p>1: ADC conversion in operation</p> <p>[For write operation]</p> <p>0: -</p> <p>1: Starts AD conversion</p> <p>Writing "1" to this bit starts AD conversion operation. In the Single mode and One-Time Scan mode, this bit is automatically returned to "0" when all of conversion operations have been completed.</p>	RW oneToSet	0

		Writing "1" to the Stop bit during conversion operation causes the bit to return to "0" after conversion operation being executed has been completed. "0" cannot be written to this bit (Even if "0" is written, ADC conversion operation cannot be stopped.)		
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5.3. ADCINTEN

ADCINTEN				
Description	AD conversion interrupt control register			
Address Region	adcc12	Type:	RW	
Offset	0x0000 0008			
Physical address View0	0x4004 8008			
Physical address View1	-			
Bitfield Details				
Bits	Name	Description	Access	Reset
31:6	Reserved	-	-	-
5	CmpInt1En	Converted value comparison 1 interrupt 0: Disable 1: Enable	RW modify	0
4	CmpInt0En	Converted value comparison 0 interrupt 0: Disable 1: Enable	RW modify	0
3:2	Reserved	-	-	-
1	ScanEndEn	Scan operation termination interrupt 0: Disable 1: Enable	RW modify	0
0	ConvEndEn	Conversion termination interrupt 0: Disable 1: Enable	RW modify	0

5.4. ADCINTSTS

ADCINTSTS				
Description		AD conversion interrupt status register		
Address Region		adcc12	Type:	RW
Offset		0x0000 000C		
Physical address View0		0x4004 800C		
Physical address View1		-		
Bitfield Details				
Bits	Name	Description	Access	Reset
31:20	Reserved	-	-	-
19:16	ChInt	Channel interrupt Indicates interrupt occurrence status in each of Ch 0 to 3. 0: No interrupt occurred 1: Interrupt occurred Details of interrupt factors can be checked by an interrupt status register for each channel.	RO	0x0
15:6	Reserved	-	-	-
5	Cmplnt1	Converted value comparison 1 interrupt [For read] 0: No interrupt occurred 1: Interrupt occurred [For write] 0: - 1: Clear interrupt	RW oneToClear	0
4	Cmplnt0	Converted value comparison 0 interrupt [For read] 0: No interrupt occurred 1: Interrupt occurred [Write] 0: - 1: Clear interrupt	RW oneToClear	0
3:2	Reserved	-	-	-
1	ScanEnd	Scan operation termination interrupt [For read] 0: No interrupt occurred 1: Interrupt occurred [For write] 0: - 1: Clear interrupt	RW oneToClear	0
0	ConvEnd	Conversion termination interrupt [For read] 0: No interrupt occurred 1: Interrupt occurred [For write] 0: - 1: Clear interrupt	RW oneToClear	0

5.5. SPLT_CTL

SPLT_CTL				
Description	Sampling timing generation counter control register			
Address Region	adcc12	Type:	RW	
Offset	0x0000 0010			
Physical address View0	0x4004 8010			
Physical address View1	-			
Bitfield Details				
Bits	Name	Description	Access	Reset
31:7	Reserved	-	-	-
6:4	SrcSel	Source clock selection for sampling timing generation counter 000: ADC clock 001: 4 divisions of ADC clock 010: 16 divisions of ADC clock 011: 64 divisions of ADC clock 100: RTC clock Other than those above: Settings prohibited	RW modify	0x0
3:1	Reserved	-	-	-
0	Reserved	-	-	-

5.6. SPLT_PER

SPLT_PER				
Description	Sampling period setting register			
Address Region	adcc12	Type:	RW	
Offset	0x0000 0014			
Physical address View0	0x4004 8014			
Physical address View1	-			
Bitfield Details				
Bits	Name	Description	Access	Reset
31:16	Reserved	-	-	-
15:0	Period	Specifies the period of sampling timing signal Set the number of clock cycles of sampling timing generation counter. Setting of "0x0000" is prohibited. Set values in the range from "0x0001" to "0xFFFF".	RW modify	0x0000

5.7. SPLT_WAVCFG

SPLT_WAVCFG				
Description	Sampling timing signal waveform setting register			
Address Region	adcc12	Type:	RW	
Offset	0x0000 0018			
Physical address View0	0x4004 8018			
Physical address View1	-			
Bitfield Details				
Bits	Name	Description	Access	Reset
31:16	Reserved	-	-	-
15:0	CycToRise	Specifies the time to rise of sampling timing signal Set the number of clock cycles of sampling timing generation counter. Set values smaller than [SPLT_PER].	RW modify	0x0000

5.8. SPLT_SYNC_WAVCFG

SPLT_SYNC_WAVCFG				
Description	Sampling timing synchronous signal waveform setting register			
Address Region	adcc12	Type:	RW	
Offset	0x0000 001C			
Physical address View0	0x4004 801C			
Physical address View1	-			
Bitfield Details				
Bits	Name	Description	Access	Reset
31:16	Reserved	-	-	-
15:0	CycToRise	Specifies the time to rise of sampling timing synchronous signal Set the number of clock cycles of sampling timing generation counter. Set values smaller than [SPLT_PER].	RW modify	0x0000

5.9. CMPDATA_0

CMPDATA_0				
Description	Compare data setting register 0			
Address Region	adcc12	Type:	RW	
Offset	0x0000 0020			
Physical address View0	0x4004 8020			
Physical address View1	-			
Bitfield Details				
Bits	Name	Description	Access	Reset
31:30	Reserved	-	-	-
29	CmpSel	Compare mode select 0: An interrupt occurs when converted values is larger than compare data.	RW modify	0

		1: An interrupt occurs when converted values is smaller than converted values		
28	CmpEn	Compare enable 0: Converted values not compared 1: Converted values compared	RW modify	0
27:26	Reserved	-	-	-
25:24	CmpCh	Compare channel select Selects a channel where converted values are compared 00: Ch0 01: Ch1 10: Ch2 11: Ch3	RW modify	0x0
23:16	Reserved	-	-	-
15:4	CmpData	Compare data Converted values to be stored in FIFO and the value of this register field are compared, and an interrupt signal is generated according to the results of comparison as to which is greater or smaller. Comparison as to which is greater or smaller is specified by the CmpSel bit.	RW modify	0x000
3:0	Reserved	-	-	-

5.10. CMPDATA_1

CMPDATA_1				
Description	Compare data setting register 1			
Address Region	adcc12	Type:	RW	
Offset	0x0000 0024			
Physical address View0	0x4004 8024			
Physical address View1	-			
Bitfield Details				
Bits	Name	Description	Access	Reset
31:30	Reserved	-	-	-
29	CmpSel	Same as CMPDATA_0	RW modify	0
28	CmpEn	Same as CMPDATA_0	RW modify	0
27:26	Reserved	-	-	-
25:24	CmpCh	Same as CMPDATA_0	RW modify	0x0
23:16	Reserved	-	-	-
15:4	CmpData	Same as CMPDATA_0	RW modify	0x000
3:0	Reserved	-	-	-

5.11. EXT_CTL

EXT_CTL				
Description	External output signal control register			
Address Region	adcc12	Type:	RW	
Offset	0x0000 0040			
Physical address View0	0x4004 8040			
Physical address View1	-			
Bitfield Details				
Bits	Name	Description	Access	Reset
31:3	Reserved	-	-	-
2	InvExt	External output signal inversion select 0: Not inverted 1: Inverted *) Invert/Not invert process is performed on data selected by SelExt	RW modify	0
1:0	SelExt	External output signal data selection 00: "0" is always output 01: "1" is always output 10/11: Sampling timing synchronous signals are output	RW modify	0x0

5.12. CH0_MODE

CH0_MODE				
Description	Channel 0 mode setting register			
Address Region	adcc12	Type:	RW	
Offset	0x0000 0100			
Physical address View0	0x4004 8100			
Physical address View1	-			
Bitfield Details				
Bits	Name	Description	Access	Reset
31:19	Reserved	-	-	-
18:16	Reserved	-	-	-
15:11	Reserved	-	-	-
10:8	WaterMark	Watermark interrupt level count Selects the number of FIFO steps where Watermark interrupt is generated 000: 1 step 001: 2 steps 010: 3 steps 011: 4 steps ... 110: 7 steps 111: 8 steps	RW modify	0x7
7	DMAReq	DMA request status [For read] 0: No DMA request 1: DMA request asserted [For write] 0: - 1: Cancel DMA request	RW oneToClear	0
6:4	DownSpl	Down Sampling 000: No down sampling (sampling	RW modify	0x0

		done every time) 001: One sampling in two times 010: One sampling in three times ... 110: One sampling in seven times 111: One sampling in eight times		
3	DMAEn	DMA transfer request enable 0: Disable 1: Enable	RW modify	0
2	OfstEn	Offset for conversion data enable 0: Disable 1: Enable	RW modify	0
1	DtFmt	Conversion data format Selects formats of data to be stored in FIFO 0: Unsigned integer 1: Signed integer	RW modify	0
0	ChEn	Channel enable Determines whether an analog input of this channel is subjected to AD conversion. Enabled only in the One-Time and Cyclic Scan modes. In Single mode, the channel set to [MODESEL].ChSel are selected regardless of settings of this bit. 0: Disable 1: Enable	RW modify	0

5.13. CH0_INTEN

CH0_INTEN				
Description	Channel 0 interrupt control register			
Address Region	adcc12	Type:	RW	
Offset	0x0000 0104			
Physical address View0	0x4004 8104			
Physical address View1	-			
Bitfield Details				
Bits	Name	Description	Access	Reset
31:6	Reserved	-	-	-
5	FIFOurnEn	FIFO underrun interrupt 0: Disable 1: Enable	RW modify	0
4	FIFOFullEn	FIFO full interrupt 0: Disable 1: Enable	RW modify	0
3	LstDLostEn	Last data lost interrupt 0: Disable 1: Enable	RW modify	0
2	FstDLostEn	1st data lost interrupt 0: Disable 1: Enable	RW modify	0
1	WMIntEn	Watermark interrupt 0: Disable 1: Enable	RW modify	0
0	ChEocEn	End of Conversion interrupt 0: Disable 1: Enable	RW modify	0

5.14. CH0_INTSTS

CH0_INTSTS				
Description		Channel 0 interrupt status register		
Address Region		adcc12	Type:	RW
Offset		0x0000 0108		
Physical address View0		0x4004 8108		
Physical address View1		-		
Bitfield Details				
Bits	Name	Description	Access	Reset
31:6	Reserved	-	-	-
5	FIFOurun	FIFO underrun interrupt [For read] 0: No interrupt occurred 1: Interrupt occurred [For write] 0: - 1: Clear interrupt	RW oneToClear	0
4	FIFOFull	FIFO full interrupt [For read] 0: No interrupt occurred 1: Interrupt occurred [For write] 0: - 1: Clear interrupt	RW oneToClear	0
3	LstDLost	Last data lost interrupt [For read] 0: No interrupt occurred 1: Interrupt occurred [For write] 0: - 1: Clear interrupt	RW oneToClear	0
2	FstDLost	1st data lost interrupt [For read] 0: No interrupt occurred 1: Interrupt occurred [For write] 0: - 1: Clear interrupt	RW oneToClear	0
1	WMInt	Watermark interrupt [For read] 0: No interrupt occurred 1: Interrupt occurred [For write] 0: - 1: Clear interrupt	RW oneToClear	0
0	ChEoc	Conversion completion interrupt [For read] 0: No interrupt occurred 1: Interrupt occurred [For write] 0: - 1: Clear interrupt	RW oneToClear	0

5.15. CH0_OFFSET

CH0_OFFSET				
Description	Channel 0 conversion data offset			
Address Region	adcc12	Type:	RW	
Offset	0x0000 010C			
Physical address View0	0x4004 810C			
Physical address View1	-			
Bitfield Details				
Bits	Name	Description	Access	Reset
31:16	Reserved	-	-	-
15:12	Reserved	-	-	-
11:4	Offset	Offset data for adjusting conversion data If offset for conversion data is enabled, conversion result is added with this register's value and then stored to FIFO. MSB of this register is a sign bit (i.e. calculation with conversion result is done after sign extension). If arithmetic result is larger than the upper limit or smaller than lower limits of the conversion range, limit values are stored in FIFO.	RW modify	0x00
3:0	Reserved	-	-	-

5.16. CH0_FIFOSTS

CH0_FIFOSTS				
Description	Channel 0 FIFO status			
Address Region	adcc12	Type:	RO	
Offset	0x0000 0110			
Physical address View0	0x4004 8110			
Physical address View1	-			
Bitfield Details				
Bits	Name	Description	Access	Reset
31:4	Reserved	-	-	-
3:0	DataNum	Number of data frames in FIFO 0 to 8 frame(s)	RO	0x0

5.17. CH1_MODE

CH1_MODE				
Description	Channel 1 mode setting register			
Address Region	adcc12	Type:	RW	
Offset	0x0000 0120			
Physical address View0	0x4004 8120			
Physical address View1	-			
Bitfield Details				
Bits	Name	Description	Access	Reset
31:19	Reserved	-	-	-
18:16	Reserved	-	-	-
15:11	Reserved	-	-	-
10:8	WaterMark	Refer to the description of the corresponding field in CH0_MODE.	RW modify	0x7
7	DMAReq	Refer to the description of the corresponding field in CH0_MODE.	RW oneToClear	0
6:4	DownSpl	Refer to the description of the corresponding field in CH0_MODE.	RW modify	0x0
3	DMAEn	Refer to the description of the corresponding field in CH0_MODE.	RW modify	0
2	OfstEn	Refer to the description of the corresponding field in CH0_MODE.	RW modify	0
1	DtFmt	Refer to the description of the corresponding field in CH0_MODE.	RW modify	0
0	ChEn	Refer to the description of the corresponding field in CH0_MODE.	RW modify	0

5.18. CH1_INTEN

CH1_INTEN				
Description	Channel 1 interrupt control register			
Address Region	adcc12	Type:	RW	
Offset	0x0000 0124			
Physical address View0	0x4004 8124			
Physical address View1	-			
Bitfield Details				
Bits	Name	Description	Access	Reset
31:6	Reserved	-	-	-
5	FIFOurunEn	Refer to the description of the corresponding field in CH0_INTEN.	RW modify	0
4	FIFOFullEn	Refer to the description of the corresponding field in CH0_INTEN.	RW modify	0
3	LstDLostEn	Refer to the description of the corresponding field in CH0_INTEN.	RW modify	0
2	FstDLostEn	Refer to the description of the corresponding field in CH0_INTEN.	RW modify	0
1	WMIIntEn	Refer to the description of the corresponding field in CH0_INTEN.	RW modify	0
0	ChEocEn	Refer to the description of the corresponding field in CH0_INTEN.	RW modify	0

5.19. CH1_INTSTS

CH1_INTSTS				
Description	Channel 1 interrupt status register			
Address Region	adcc12	Type:	RW	
Offset	0x0000 0128			
Physical address View0	0x4004 8128			
Physical address View1	-			
Bitfield Details				
Bits	Name	Description	Access	Reset
31:6	Reserved	-	-	-
5	FIFOurn	Refer to the description of the corresponding field in CH0_INTSTS.	RW oneToClear	0
4	FIFOFull	Refer to the description of the corresponding field in CH0_INTSTS.	RW oneToClear	0
3	LstDLost	Refer to the description of the corresponding field in CH0_INTSTS.	RW oneToClear	0
2	FstDLost	Refer to the description of the corresponding field in CH0_INTSTS.	RW oneToClear	0
1	WMInt	Refer to the description of the corresponding field in CH0_INTSTS.	RW oneToClear	0
0	ChEoc	Refer to the description of the corresponding field in CH0_INTSTS.	RW oneToClear	0

5.20. CH1_OFFSET

CH1_OFFSET				
Description	Channel 1 conversion data offset			
Address Region	adcc12	Type:	RW	
Offset	0x0000 012C			
Physical address View0	0x4004 812C			
Physical address View1	-			
Bitfield Details				
Bits	Name	Description	Access	Reset
31:16	Reserved	-	-	-
15:12	Reserved	-	-	-
11:4	Offset	Refer to the description of the corresponding field in CH0_OFFSET.	RW modify	0x00
3:0	Reserved	-	-	-

5.21. CH1_FIFOSTS

CH1_FIFOSTS				
Description	Channel 1 FIFO status			
Address Region	adcc12	Type:	RO	
Offset	0x0000 0130			
Physical address View0	0x4004 8130			
Physical address View1	-			
Bitfield Details				
Bits	Name	Description	Access	Reset
31:4	Reserved	-	-	-
3:0	DataNum	Refer to the description of the corresponding field in CH0_FIFOSTS.	RO	0x0

5.22. CH2_MODE

CH2_MODE				
Description	Channel 2 mode setting register			
Address Region	adcc12	Type:	RW	
Offset	0x0000 0140			
Physical address View0	0x4004 8140			
Physical address View1	-			
Bitfield Details				
Bits	Name	Description	Access	Reset
31:19	Reserved	-	-	-
18:16	Reserved	-	-	-
15:11	Reserved	-	-	-
10:8	WaterMark	Refer to the description of the corresponding field in CH0_MODE.	RW modify	0x7
7	DMAReq	Refer to the description of the corresponding field in CH0_MODE.	RW oneToClear	0
6:4	DownSpl	Refer to the description of the corresponding field in CH0_MODE.	RW modify	0x0
3	DMAEn	Refer to the description of the corresponding field in CH0_MODE.	RW modify	0
2	OfstEn	Refer to the description of the corresponding field in CH0_MODE.	RW modify	0
1	DtFmt	Refer to the description of the corresponding field in CH0_MODE.	RW modify	0
0	ChEn	Refer to the description of the corresponding field in CH0_MODE.	RW modify	0

5.23. CH2_INTEN

CH2_INTEN				
Description	Channel 2 interrupt control register			
Address Region	adcc12	Type:	RW	
Offset	0x0000 0144			
Physical address View0	0x4004 8144			
Physical address View1	-			
Bitfield Details				
Bits	Name	Description	Access	Reset
31:6	Reserved	-	-	-
5	FIFOurnEn	Refer to the description of the corresponding field in CH0_INTEN.	RW modify	0
4	FIFOFullEn	Refer to the description of the corresponding field in CH0_INTEN.	RW modify	0
3	LstDLostEn	Refer to the description of the corresponding field in CH0_INTEN.	RW modify	0
2	FstDLostEn	Refer to the description of the corresponding field in CH0_INTEN.	RW modify	0
1	WMIntEn	Refer to the description of the corresponding field in CH0_INTEN.	RW modify	0
0	ChEocEn	Refer to the description of the corresponding field in CH0_INTEN.	RW modify	0

5.24. CH2_INTSTS

CH2_INTSTS				
Description	Channel 2 interrupt status register			
Address Region	adcc12	Type:	RW	
Offset	0x0000 0148			
Physical address View0	0x4004 8148			
Physical address View1	-			
Bitfield Details				
Bits	Name	Description	Access	Reset
31:6	Reserved	-	-	-
5	FIFOurn	Refer to the description of the corresponding field in CH0_INTSTS.	RW oneToClear	0
4	FIFOFull	Refer to the description of the corresponding field in CH0_INTSTS.	RW oneToClear	0
3	LstDLost	Refer to the description of the corresponding field in CH0_INTSTS.	RW oneToClear	0
2	FstDLost	Refer to the description of the corresponding field in CH0_INTSTS.	RW oneToClear	0
1	WMInt	Refer to the description of the corresponding field in CH0_INTSTS.	RW oneToClear	0
0	ChEoc	Refer to the description of the corresponding field in CH0_INTSTS.	RW oneToClear	0

5.25. CH2_OFFSET

CH2_OFFSET				
Description	Channel 2 conversion data offset			
Address Region	adcc12	Type:	RW	
Offset	0x0000 014C			
Physical address View0	0x4004 814C			
Physical address View1	-			
Bitfield Details				
Bits	Name	Description	Access	Reset
31:16	Reserved	-	-	-
15:12	Reserved	-	-	-
11:4	Offset	Refer to the description of the corresponding field in CH0_OFFSET.	RW modify	0x00
3:0	Reserved	-	-	-

5.26. CH2_FIFOSTS

CH2_FIFOSTS				
Description	Channel 2 FIFO status			
Address Region	adcc12	Type:	RO	
Offset	0x0000 0150			
Physical address View0	0x4004 8150			
Physical address View1	-			
Bitfield Details				
Bits	Name	Description	Access	Reset
31:4	Reserved	-	-	-
3:0	DataNum	Refer to the description of the corresponding field in CH0_FIFOSTS.	RO	0x0

5.27. CH3_MODE

CH3_MODE				
Description	Channel 3 mode setting register			
Address Region	adcc12	Type:	RW	
Offset	0x0000 0160			
Physical address View0	0x4004 8160			
Physical address View1	-			
Bitfield Details				
Bits	Name	Description	Access	Reset
31:19	Reserved	-	-	-
18:16	Reserved	-	-	-
15:11	Reserved	-	-	-
10:8	WaterMark	Refer to the description of the corresponding field in CH0_MODE.	RW modify	0x7
7	DMAReq	Refer to the description of the corresponding field in CH0_MODE.	RW oneToClear	0
6:4	DownSpl	Refer to the description of the corresponding field in CH0_MODE.	RW modify	0x0

3	DMAEn	Refer to the description of the corresponding field in CH0_MODE.	RW modify	0
2	OfstEn	Refer to the description of the corresponding field in CH0_MODE.	RW modify	0
1	DtFmt	Refer to the description of the corresponding field in CH0_MODE.	RW modify	0
0	ChEn	Refer to the description of the corresponding field in CH0_MODE.	RW modify	0

5.28. CH3_INTEN

CH3_INTEN				
Description	Channel 3 interrupt control register			
Address Region	adcc12	Type:	RW	
Offset	0x0000 0164			
Physical address View0	0x4004 8164			
Physical address View1	-			
Bitfield Details				
Bits	Name	Description	Access	Reset
31:6	Reserved	-	-	-
5	FIFOurunEn	Refer to the description of the corresponding field in CH0_INTEN.	RW modify	0
4	FIFOFullEn	Refer to the description of the corresponding field in CH0_INTEN.	RW modify	0
3	LstDLostEn	Refer to the description of the corresponding field in CH0_INTEN.	RW modify	0
2	FstDLostEn	Refer to the description of the corresponding field in CH0_INTEN.	RW modify	0
1	WMIntEn	Refer to the description of the corresponding field in CH0_INTEN.	RW modify	0
0	ChEocEn	Refer to the description of the corresponding field in CH0_INTEN.	RW modify	0

5.29. CH3_INTSTS

CH3_INTSTS				
Description	Channel 3 interrupt status register			
Address Region	adcc12	Type:	RW	
Offset	0x0000 0168			
Physical address View0	0x4004 8168			
Physical address View1	-			
Bitfield Details				
Bits	Name	Description	Access	Reset
31:6	Reserved	-	-	-
5	FIFOurun	Refer to the description of the corresponding field in CH0_INTSTS.	RW oneToClear	0
4	FIFOFull	Refer to the description of the corresponding field in CH0_INTSTS.	RW oneToClear	0
3	LstDLost	Refer to the description of the corresponding field in CH0_INTSTS.	RW oneToClear	0
2	FstDLost	Refer to the description of the corresponding field in CH0_INTSTS.	RW oneToClear	0
1	WMInt	Refer to the description of the corresponding field in CH0_INTSTS.	RW oneToClear	0

0	ChEoc	Refer to the description of the corresponding field in CH0_INTSTS.	RW oneToClear	0
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5.30. CH3_OFFSET

CH3_OFFSET				
Description	Channel 3 conversion data offset			
Address Region	adcc12	Type:	RW	
Offset	0x0000 016C			
Physical address View0	0x4004 816C			
Physical address View1	-			
Bitfield Details				
Bits	Name	Description	Access	Reset
31:16	Reserved	-	-	-
15:12	Reserved	-	-	-
11:4	Offset	Refer to the description of the corresponding field in CH0_OFFSET.	RW modify	0x00
3:0	Reserved	-	-	-

5.31. CH3_FIFOSTS

CH3_FIFOSTS				
Description	Channel 3 FIFO status			
Address Region	adcc12	Type:	RO	
Offset	0x0000 0170			
Physical address View0	0x4004 8170			
Physical address View1	-			
Bitfield Details				
Bits	Name	Description	Access	Reset
31:4	Reserved	-	-	-
3:0	DataNum	Refer to the description of the corresponding field in CH0_FIFOSTS.	RO	0x0

5.32. CH0_DATA

CH0_DATA				
Description	Channel 0 conversion result data register *) Though there is a 64-byte region ranging 0x800 to 0x83F, each address is allocated to the same FIFO output. Read should be done with 16-bit access. 8-bit read makes the FIFO to next level. 32-bit read does not make the FIFO pop operation twice. The same data is read for both the upper 16 bits and lower 16 bits.			
Address Region	adcc12	Type:	RO	
Offset	0x0000 0800-			
Physical address View0	0x4004 8800- 0x4004 883C			
Physical address View1	-			
Bitfield Details				
Bits	Name	Description	Access	Reset

31:16	Reserved	-	-	-
15:4	ChData	CH0 conversion data FIFO	RO	0x000
3:0	Reserved	-	-	-

5.33. CH1_DATA

CH1_DATA				
Description	Channel 1 conversion result data register			
	*) Though there is a 64-byte region ranging 0x840 to 0x87F, each address is allocated to the same FIFO output. Read should be done with 16-bit access. 8-bit read makes the FIFO to next level. 32-bit read does not make the FIFO pop operation twice. The same data is read for both the upper 16 bits and lower 16 bits.			
Address Region	adcc12	Type:	RO	
Offset	0x0000 0840-			
Physical address View0	0x4004 8840- 0x4004 887C			
Physical address View1	-			
Bitfield Details				
Bits	Name	Description	Access	Reset
31:16	Reserved	-	-	-
15:4	ChData	CH1 conversion data FIFO	RO	0x000
3:0	Reserved	-	-	-

5.34. CH2_DATA

CH2_DATA				
Description	Channel 2 conversion result data register			
	*) Though there is a 64-byte region ranging 0x880 to 0x8BF, each address is allocated to the same FIFO output. Read should be done with 16-bit access. 8-bit read makes the FIFO to next level. 32-bit read does not make the FIFO pop operation twice. The same data is read for both the upper 16 bits and lower 16 bits.			
Address Region	adcc12	Type:	RO	
Offset	0x0000 0880-			
Physical address View0	0x4004 8880- 0x4004 88BC			
Physical address View1	-			
Bitfield Details				
Bits	Name	Description	Access	Reset
31:16	Reserved	-	-	-
15:4	ChData	CH2 conversion data FIFO	RO	0x000
3:0	Reserved	-	-	-

5.35. CH3_DATA

CH3_DATA				
Description	Channel 3 conversion result data register *) Though there is a 64-byte region ranging 0x8C0 to 0x8FF, each address is allocated to the same FIFO output. Read should be done with 16-bit access. 8-bit read makes the FIFO to next level. 32-bit read does not make the FIFO pop operation twice. The same data is read for both the upper 16 bits and lower 16 bits.			
Address Region	adcc12	Type:	RO	
Offset	0x0000 08C0-			
Physical address View0	0x4004 88C0- 0x4004 88FC			
Physical address View1	-			
Bitfield Details				
Bits	Name	Description	Access	Reset
31:16	Reserved	-	-	-
15:4	ChData	CH3 conversion data FIFO	RO	0x000
3:0	Reserved	-	-	-

6. Revision History

Table 6.1 Revision History

Revision	Date	Description
0.1	2014-03-31	Newly released
0.2	2014-04-10	Changed expression in some parts.
0.3	2014-10-07	Added reference voltage pins into the block figure. Table of external pins are added. Added explanation about reference voltage. Added a section "Starting AD Conversion by External trigger". Modified wrong description of Start-up/Stop procedure. Added description about clock frequency setting.
0.4	2014-12-15	Deleted unnecessary procedure in transition to/from RETENTION mode.
1.0	2015-01-22	Official version
1.1	2014-07-16	Added Figure 2.3 and description in 2.3.External Pins.
1.2	2015-11-24	Added Section 4.4 (4)
1.3	2018-02-06	Changed header, footer and the last page. Changed corporate name and descriptions. Modified Arm logo and descriptions.

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