Application Processor Lite *ApP Lite*

TZ1000 Series

Reference Manual

MCU Power Management Unit

Revision 1.6

2018-02

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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Preface

This document provides the specification for the MCU Power Management Unit designed for the TZ1000 Series.

Intended Audience

This document is intended for the following users.

Driver software developers.

System designers

Conventions in this document

- The following notational conventions apply to numbers:
  Hexadecimal number: 0xABC
  Decimal number: 123 or 0d123 - Only when it should be explicitly indicated that the number is decimal.
  Binary number: 0b111 - It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- Low active signals are indicated with a name suffixed with "_N".
- A signal is asserted when it goes to its active level while it is deasserted when it goes to its inactive level.
- A set of multiple signals may be referred to as [m:n].
  Example: S[3:0] indicates four signals, S3, S2, S1 and S0, collectively.
- In the text, register names are enclosed in brackets *[ ]*.
  Example:*[ABCD]*
- A set of multiple registers, fields or bits of the same type may be described collectively using "n".
  Example: *[XYZ1]*, *[XYZ2]*, and *[XYZ3]* to *[XYZn]*
- A range of register bits are referred to as [m:n].
  Example: [3:0] indicates a range from bit 3 to bit 0.
- Values set in registers are indicated using either a hexadecimal or binary number.
- Example: *[ABCD]*.EFG = 0x01 (hexadecimal), *[XYZn]*.VW = 1 (binary)
- Words and bytes are defined as follows:
  Byte: 8 bits
  Halfword: 16 bits
  Word: 32 bits
  Doubleword: 64 bits
- Register bit attributes are defined as follows:
  R: Read-only
  W: Write-only
  W1C: Clear by write of 1 - A write of "1" clears the corresponding bit to 0.
  W1S: Set by write of 1 - A write of "1" sets the corresponding bit to 1.
  R/W: Read/Write
  R/W0C: Read/Clear by write of 0
  R/W1C: Read/Clear by write of 1
  R/W1S: Read/Set by write of 1
  RS/WC: Set by read/Clear by write - Set after a read and cleared after a data write.
- Registers only support word access unless otherwise specified.
- Any registers defined as Reserved in the text must not be rewritten. Also, any values read from such registers should not be used.
- Any bits for which default values are defined as "—" would return undefined values if read.
- When a data is written to a register containing both writable and read-only (R) bit fields, its default values should be written to read-only (R) bit fields. For any bit fields with default values defined as "—," refer to the definitions of the relevant register.
- Default values should be written to any reserved bit fields in a write-only register. For any bit fields with default values defined as "—," refer to the definitions of the relevant register.

Terms and Abbreviations

These specifications introduce a part of the terms and abbreviation which they used.

Table 1.1 Terms and abbreviations

Term	Description
PMU	Power Management Unit
DCG	Dynamic Clock Gating
BOR	Brown Out Reset
BGR	Band Gap Reference
LVD	Level Voltage Detector
ADPLL	All Digital Phase Locked Loop
SIOSC	Silicon Oscillator
PSW	Power Switch
MCU_SYS_RESET_N	HW Reset Pin
RetentionFF	Two powers of VDDB (regular ON) and VDDC are supplied to the FF which consists of a Set/Reset FF and a latch. Low power consumption is done by the VDDC shut-down at the Retention state.
SAVE	The signal for holding data to the latch in RetentionFF
RSTR	The signal for returning the data held in the latch in RetentionFF.
RetentionSRAM	Only memory data is held using the RET/WAIT signal. Two powers of VDDB/VDDC are supplied like RetentionFF, and low power consumption is done by the VDDC shut-down.
RET	The Retention signal used by RetentionSRAM or it may be used as an abbreviation of Retention.
WAIT	The Retention signal used by RetentionSRAM The difference from RET is no VDDC shut-down. The power supply of the Row decoder is shut down by PSW in the SRAM.
WFI (state)	It indicates that the WFI, WFE and SEV instruction are executed.

1. Overview

This document describes about the PMU (Power Management Unit) module. The function outlines are shown as follows.

- Clock control
  - Clock source control
  - Clock domain
    - Clock source selection
    - Prescaler (division) function
  - Clock gating control
    - Dynamic clock gating
    - Request for releasing clock gating
  - 32.768 kHz Clock out control
- Reset control
  - Software reset
  - Hardware reset
  - WDT reset
  - LOCKUP reset
  - SYSRESETREQ reset
- Power supply control
  - Power supply circuit
  - Power supply domain
  - Power domain control
    - Power supply shut-down control
    - Retention control
- Power mode
  - Power mode shift sequence
    - VoltageMode: Power supply and voltage change control (DVS control)
    - PowerMode: Power state control
- Boot sequence
  - Power supply sequence
  - Start-up sequence
- BrownOut control
  - Brown Out interrupt
  - Brown Out reset
- IO Control
  - IO Buffer control
    - IO Retention control
    - IO Output Buffer reset control
    - IO Input Buffer stand-by control
  - WakeUp interrupt control
- EFUSE load function
  - Override function

2. Block Diagram

The outline of the internal blocks of this module and a connection relation with each block are shown in Figure 2.1. PMU consists of three blocks, PMUHV, PMULV0, and PMULV1. The PMULV0 and PMULV1 are collectively called PMULV.

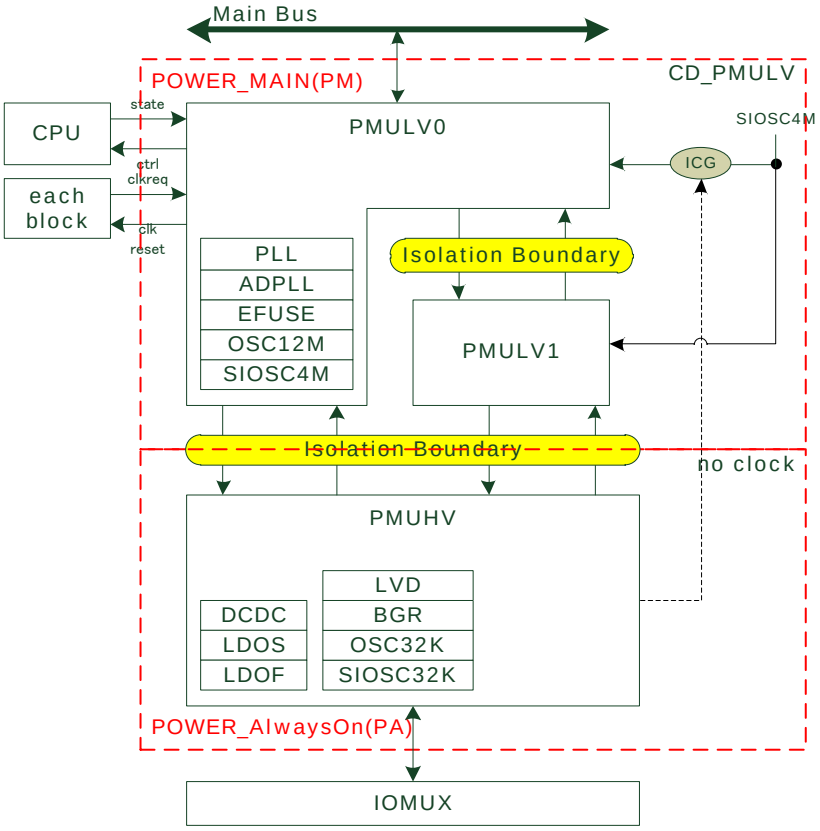

Figure 2.1 Block diagram

- PMUHV: It belongs to PA domain (refer to 4.2.2 Power Supply Domain), and there is no clock in this block. This block is always supplied with the power.
  * OSC32K and SIOSC32K are the clocks for RTC.
  - DCDC: Supplies from 1.0 to 1.2 V
  - LDOS: Supplies 0.9 V
  - LDOF: Supplies 1.8 V for SPI
  - LVD: The voltage detector for detecting 3.3 V
  - BGR: The block which generates the reference voltage to each LDO and LVD
- PMULV0: It belongs to PM domain (refer to 4.2.2 Power Supply Domain), and operates with PMULV_CLK which is driven by SIOSC4M.
  - Almost all the functions as PMULV are managed. It has connected with a main bus by APB3 protocol, and has an asynchronous relation.
- PMULV1: It belongs to PM domain (refer to 4.2.2 Power Supply Domain), and operates with PMULV_CLK which is driven by SIOSC4M.
  - The function of a part of PMULV is managed.

3. Address Map

Table 3.1 MCU Power Management Unit Register Map

Register Name	Type	Width	Reset Value	Address Offset
CG_ON_POWERDOMAIN	RW	32	0x0000 0F82	0x0000 0000
CG_OFF_POWERDOMAIN	RW	32	0x0000 003D	0x0000 0004
DCG_POWERDOMAIN	RW	32	0x0000 0000	0x0000 0010
SRST_ON_POWERDOMAIN	RW	32	0x0000 0F82	0x0000 0020
SRST_OFF_POWERDOMAIN	RW	32	0x0000 0021	0x0000 0024
CG_ON_PM_0	RW	32	0x0050 0000	0x0000 0100
CG_ON_PM_1	RW	32	0x3FA8 AAB7	0x0000 0104
CG_ON_PM_2	RW	32	0x0001 0FF1	0x0000 0108
CG_ON_PE	RW	32	0x0000 000F	0x0000 0110
CG_ON_PF	RW	32	0x0000 0000	0x0000 0120
CG_ON_PD	RW	32	0x0000 0001	0x0000 0128
CG_ON_PU	RW	32	0x0000 001D	0x0000 012C
CG_ON_PA12	RW	32	0x0000 0007	0x0000 0134
CG_ON_PA24	RW	32	0x0000 0007	0x0000 0138
CG_ON_PP1	RW	32	0x0000 FFF1	0x0000 013C
CG_ON_HARDMACRO	RW	32	0x0000 0000	0x0000 0140
CG_ON_REFCLK	RW	32	0x0001 0001	0x0000 0148
CG_OFF_PM_0	RW	32	0x0F80 0000	0x0000 0180
CG_OFF_PM_1	RW	32	0x0000 0000	0x0000 0184
CG_OFF_PM_2	RW	32	0x0000 0000	0x0000 0188
CG_OFF_PE	RW	32	0x0000 0000	0x0000 0190
CG_OFF_PF	RW	32	0x0000 0007	0x0000 01A0
CG_OFF_PD	RW	32	0x0000 0000	0x0000 01A8
CG_OFF_PU	RW	32	0x0000 0000	0x0000 01AC
CG_OFF_PA12	RW	32	0x0000 0000	0x0000 01B4
CG_OFF_PA24	RW	32	0x0000 0000	0x0000 01B8
CG_OFF_PP1	RW	32	0x0000 0000	0x0000 01BC
CG_OFF_HARDMACRO	RW	32	0x0001 0001	0x0000 01C0
CG_OFF_REFCLK	RW	32	0x0000 0000	0x0000 01C8
DCG_PM_0	RW	32	0x0000 0000	0x0000 0200
DCG_PM_1	RW	32	0x0000 0000	0x0000 0204
DCG_PM_2	RW	32	0x0000 0000	0x0000 0208
DCG_PE	RW	32	0x0000 0000	0x0000 0210
DCG_PF	RW	32	0x0000 0000	0x0000 0220
DCG_PD	RW	32	0x0000 0000	0x0000 0228
DCG_PU	RW	32	0x0000 0000	0x0000 022C
DCG_PA12	RW	32	0x0000 0000	0x0000 0234
DCG_PA24	RW	32	0x0000 0000	0x0000 0238
DCG_PP1	RW	32	0x0000 0000	0x0000 023C
CLKREQ_CONFIG_PE	RW	32	0x0002 0002	0x0000 0290
SRST_ON_PM_0	RW	32	0x0050 0000	0x0000 0300
SRST_ON_PM_1	RW	32	0x3F08 009F	0x0000 0304
SRST_ON_PM_2	RW	32	0x0001 0FF1	0x0000 0308
SRST_ON_PE	RW	32	0x0000 0005	0x0000 0310
SRST_ON_PF	RW	32	0x0000 0000	0x0000 0320
SRST_ON_PD	RW	32	0x0000 0001	0x0000 0328
SRST_ON_PU	RW	32	0x0000 001D	0x0000 032C
SRST_ON_PA12	RW	32	0x0000 0003	0x0000 0334
SRST_ON_PA24	RW	32	0x0000 0003	0x0000 0338
SRST_ON_PP1	RW	32	0x0000 FFF1	0x0000 033C
SRST_OFF_PM_0	RW	32	0x0900 0000	0x0000 0380
SRST_OFF_PM_1	RW	32	0x0000 0000	0x0000 0384
SRST_OFF_PM_2	RW	32	0x0000 0000	0x0000 0388
SRST_OFF_PE	RW	32	0x0000 0000	0x0000 0390

SRST_OFF_PF	RW	32	0x0000 000F	0x0000 03A0
SRST_OFF_PD	RW	32	0x0000 0000	0x0000 03A8
SRST_OFF_PU	RW	32	0x0000 0000	0x0000 03AC
SRST_OFF_PA12	RW	32	0x0000 0000	0x0000 03B4
SRST_OFF_PA24	RW	32	0x0000 0000	0x0000 03B8
SRST_OFF_PP1	RW	32	0x0000 0000	0x0000 03BC
CTRL_MODETRAN	RW	32	0x0000 0000	0x0000 0400
CSM_MAIN	RW	32	0x0000 0000	0x0000 0404
CSM_CPUTRC	RW	32	0x0000 0000	0x0000 0408
CSM_CPUST	RW	32	0x0000 0000	0x0000 040C
CSM_USBI	RW	32	0x0000 0000	0x0000 0410
CSM_UART0	RW	32	0x0000 0000	0x0000 0414
CSM_UART1	RW	32	0x0000 0000	0x0000 0418
CSM_UART2	RW	32	0x0000 0000	0x0000 041C
CSM_ADCC12A	RW	32	0x0000 0000	0x0000 0420
CSM_ADCC24A	RW	32	0x0000 0000	0x0000 0424
PRESCAL_MAIN	RW	32	0x0000 0011	0x0000 0484
PRESCAL_CPUST	RW	32	0x0000 0001	0x0000 048C
PRESCAL_USBI	RW	32	0x0000 0000	0x0000 0490
PRESCAL_UART0	RW	32	0x0000 0000	0x0000 0494
PRESCAL_UART1	RW	32	0x0000 0000	0x0000 0498
PRESCAL_UART2	RW	32	0x0000 0000	0x0000 049C
PRESCAL_ADCC12A	RW	32	0x0000 0000	0x0000 04A0
PRESCAL_ADCC24A	RW	32	0x0000 0000	0x0000 04A4
CONFIG_OSC12M	RW	32	0x0000 0000	0x0000 0500
CONFIG_PLL_0	RW	32	0x0000 0001	0x0000 0508
CONFIG_PLL_1	RW	32	0x0000 0093	0x0000 050C
CONFIG_ADPLL_0	RW	32	0x0000 7008	0x0000 0510
CONFIG_ADPLL_1	RW	32	0x0000 0000	0x0000 0514
CONFIG_DCDC_LVREG_1	RW	32	0x0000 0000	0x0000 0528
CONFIG_LDOF_0	RW	32	0x0000 0003	0x0000 0530
OVERRIDE_EFUSE_OSC12M	RW	32	0x0000 0007	0x0000 0580
SELECT_EFUSE	RW	32	0x0000 0000	0x0000 05C0
EFUSE_REVISIONID	RO	32	—	0x0000 05DC
EFUSE_BOOTSEQ	RO	32	—	0x0000 05E0
EFUSE_SiOSC4M	RO	32	—	0x0000 05E4
BROWNOUTRESET	RW	32	0x0000 0000	0x0000 0600
MOVE_VOLTAGE_START	RW	32	0x0000 0000	0x0000 0700
MOVE_POWER_VOLTAGE_MODE	RW	32	0x0000 0000	0x0000 0704
POWERDOMAIN_CTRL	RW	32	0x0000 0000	0x0000 0710
POWERDOMAIN_CTRL_MODE	RW	32	0x0014 4004	0x0000 0714
POWERDOMAIN_CTRL_STATUS	RO	32	0x0014 4004	0x0000 0718
POWERDOMAIN_CTRL_MODE_FOR_WAIT	RW	32	0x0000 03F0	0x0000 0720
POWERDOMAIN_CTRL_MODE_FOR_WRET	RW	32	0x00A8 ABF8	0x0000 0724
POWERDOMAIN_CTRL_MODE_FOR_RET	RW	32	0x00A8 AAA8	0x0000 0728
VOLTAGEMODE_SETTING	RW	32	0x0000 0000	0x0000 0730
WAITTIME_LDOF	RW	32	0x001E 001E	0x0000 0740
WAITTIME_PSW	RW	32	0x000F 000F	0x0000 0744
WAITTIME_DVSCTL	RW	32	0x00A0 1E1E	0x0000 0748
POWERMODE_SLEEP_CG_ON	RW	32	0x0000 0000	0x0000 0780
POWERMODE_SLEEP_PRESCAL	RW	32	0x0000 0000	0x0000 0790
CG_ON_PC_SCRT	RW	32	0x0000 0004	0x0000 1124
CG_OFF_PC_SCRT	RW	32	0x0000 000B	0x0000 11A4
CG_ON_PA	RW	32	0x0001 0101	0x0000 2000
CG_OFF_PA	RW	32	0x0000 0000	0x0000 2010
SRST_ON_PA	RW	32	0x0000 0001	0x0000 2020
SRST_OFF_PA	RW	32	0x0000 0000	0x0000 2030

CSM_RTC	RW	32	0x0000 0000	0x0000 2080
RTCLV_RSYNC_SETTING	RW	32	0x0000 0000	0x0000 20C0
CONFIG_OSC32K	RW	32	0x0000 0000	0x0000 2100
CONFIG_SiOSC32K	RW	32	0x0000 0000	0x0000 2104
CONFIG_SiOSC4M	RW	32	0x0000 0001	0x0000 2108
CONFIG_DCDC_HVREG	RW	32	0x0000 0013	0x0000 210C
CONFIG_LVD_0	RW	32	0x0000 0003	0x0000 2118
CONFIG_LDOM_0	RW	32	0x0000 0000	0x0000 2120
CONFIG_LDOM_1	RW	32	0x0000 0003	0x0000 2124
CONFIG_LDOS_0	RW	32	0x0000 0000	0x0000 2130
CONFIG_LDOS_1	RW	32	0x0000 0003	0x0000 2134
OVERRIDE_EFUSE_OSC32K	RW	32	0x0000 0000	0x0000 2180
OVERRIDE_EFUSE_SiOSC32K	RW	32	0x0000 0000	0x0000 2184
OVERRIDE_EFUSE_SiOSC4M	RW	32	0x0000 0000	0x0000 2188
OVERRIDE_EFUSE_BGR_0	RW	32	0x0000 0000	0x0000 2190
OVERRIDE_EFUSE_BGR_1	RW	32	0x0007 1F00	0x0000 2194
STATUS_LVPWR	RW	32	0x0000 0000	0x0000 2200
STATUS_LVRST	RW	32	—	0x0000 2204
BROWNOUTMODE	RW	32	0x0000 0000	0x0000 2210
CTRL_IO_AON_0	RW	32	0x0000 0001	0x0000 2300
CTRL_IO_AON_1	RW	32	0x0000 0000	0x0000 2304
CTRL_IO_AON_2	RW	32	0x0000 0000	0x0000 2308
CTRL_IO_AON_3	RW	32	0x0000 0000	0x0000 230C
CTRL_IO_AON_4	RW	32	0x0000 0001	0x0000 2310
CTRL_IO_AON_5	RW	32	0x0000 0000	0x0000 2314
CTRL_IO_AON_6	RW	32	0x0000 0000	0x0000 2318
PSW_PU	RW	32	0x0000 0000	0x0000 2420
PSW_EFUSE	RW	32	0x0000 0003	0x0000 2440
PSW_PLL	RW	32	0x0000 0000	0x0000 2444
PSW_ADPLL	RW	32	0x0000 0000	0x0000 2448
PSW_IO_USB	RW	32	0x0000 0000	0x0000 2450
PSW_HARDMACRO	RW	32	0x0000 0000	0x0000 2454
ISO_PU	RW	32	0x0000 0003	0x0000 2520
ISO_EFUSE	RW	32	0x0000 0000	0x0000 2540
ISO_PLL	RW	32	0x0000 0003	0x0000 2544
ISO_ADPLL	RW	32	0x0000 0003	0x0000 2548
IRQ_SETTING_0	RW	32	0x0000 0000	0x0000 2700
IRQ_SETTING_1	RW	32	0x0000 0000	0x0000 2704
IRQ_STATUS	RW	32	0x0000 0000	0x0000 2708
WAKEUP_EN	RW	32	0x0000 0000	0x0000 270C
WAKEUP_STATUS	RO	32	0x0000 0000	0x0000 2710
CTRL_CDBGPWRUPREQ	RW	32	0x0000 0001	0x0000 2808

4. Function

4.1. Clock and Reset

4.1.1. Clock Distribution Diagram

The following figure shows the clock distribution diagram. The clock domain (except for some domains) is constituted by a clock source select circuit and a prescaler. Each block belongs to a clock domain.

- Clock source is selected by the clock source change circuit.
- The selected clock is divided by the prescaler.

The clock source select circuit is common for six domains, CD_MPIER, CD_PPIER0, CD_PPIER1, CD_PPIER2, CD_SPIC, and CD_USB. The prescalers for 5 domains other than CD_MPIER are using the prescaler output for CD_MPIER as their clock sources.

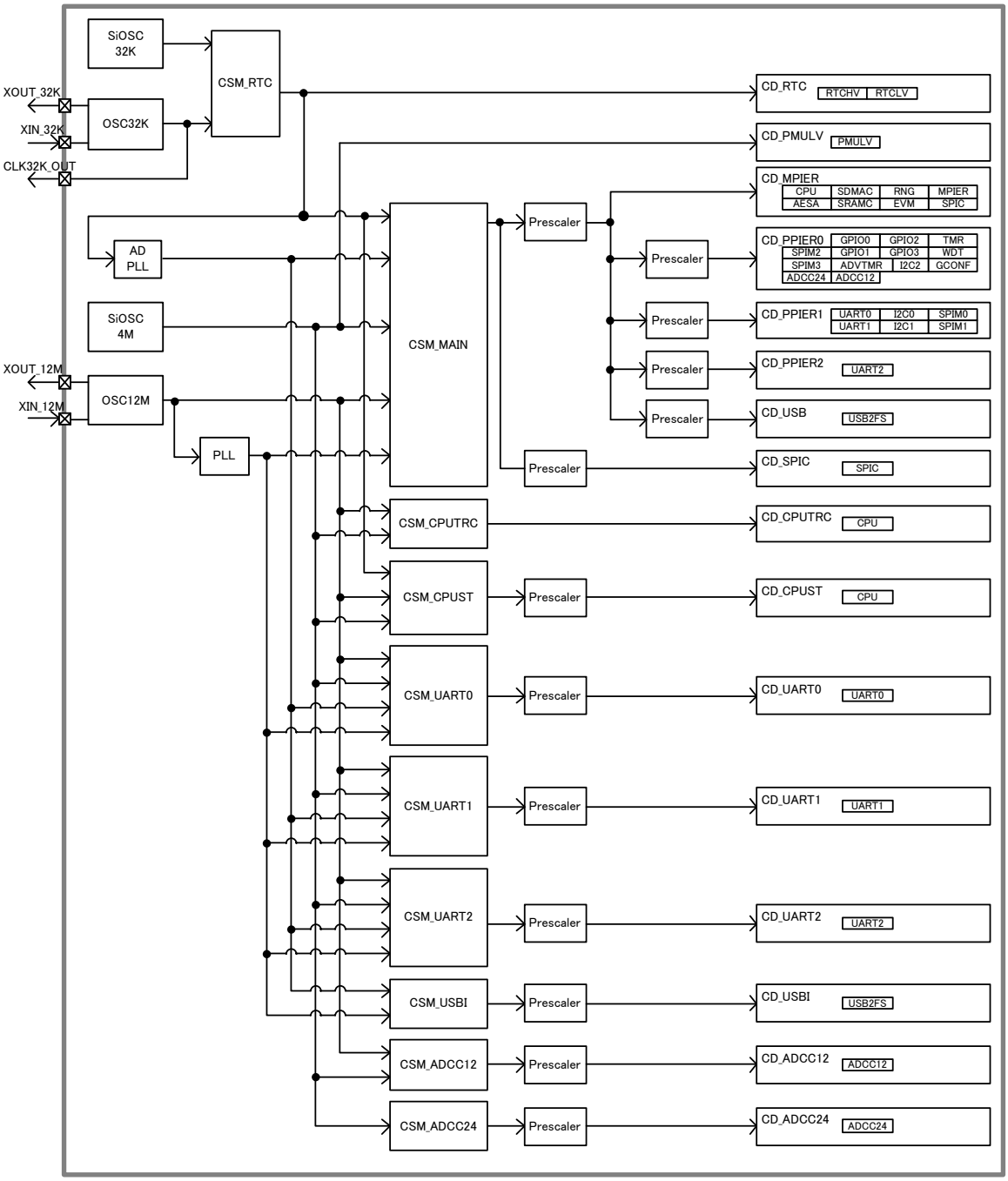

Figure 4.1 Clock distribution diagram

4.1.2. Clock Source

Six clock sources are included.

- OSC32K
  - Attach a crystal oscillator or an oscillation device outside.
  - Source oscillating frequency: 32.768 kHz
- SIOSC32K
  - A built-in self-oscillation oscillator. Since it is not so accurate compared with an external oscillator, optimization by trimming is required.
  - Source oscillating frequency: 32.768 kHz
- SIOSC4M
  - A built-in self-oscillation oscillator.
    Since it is not so accurate compared with an external oscillator, optimization by trimming is required.
  - Source oscillating frequency: 4 MHz
- ADPLL
  - It is All Digital PLL which uses OSC32K or SIOSC32K as the reference clock.
  - ADPLL cannot be used unless the reference clock is operating.
  - In the case to select SIOSC32K as the reference clock, the USB block is not able to comply with the standard.
  - Source oscillating frequency: 48 MHz
- OSC12M
  - Attach a crystal oscillator or an oscillation device outside.
  - Source oscillating frequency: 12 MHz
- PLL
  - It is PLL which uses OSC12M as the reference clock.
  - PLL cannot be used unless the reference clock is operating.
  - Source oscillating frequency: 12/24/36/48 MHz (Setting available)

4.1.3. Clock Domain

The two following tables summarize the clock source select circuit and the prescaler which constitute the circuits in each clock domain.

Table 4.1 Clock Source

Clock Domain	Clock Source Mux	Frequency (Max/Min)	Clock Source							
			OSC32K SIOSC32K	SIOSC4M	ADPLL	OSC12M	OSC12M3	PLL	PLL3	PLL9
CD_MPIER	CSM_MAIN	48 MHz/32.768 kHz	✓	✓	✓	✓	—	✓	—	—
CD_PPIER0		12 MHz/32.768 kHz								
CD_PPIER1		12 MHz/32.768 kHz								
CD_PPIER2		12 MHz/32.768 kHz								
CD_SPIC		48 MHz/32.768 kHz								
CD_USBB		48 MHz/24 MHz								
CD_RTC	CSM_RTC	32.768 kHz	✓	—	—	—	—	—	—	—
CD_CPUTRC	CSM_CPUTRC	12 MHz/4 MHz	—	✓	—	✓	—	—	—	—
CD_CPUST	CSM_CPUST	12 MHz/32.768 kHz	✓	✓	—	✓	—	—	—	—
CD_PMULV	CSM_PMULV	4 MHz	—	✓	—	—	—	—	—	—
CD_UART0	CSM_UART0	18 MHz/32.768 kHz (*1)	✓	✓	✓	✓	—	✓	—	—
CD_UART1	CSM_UART1	18 MHz/32.768 kHz (*1)	✓	✓	✓	✓	—	✓	—	—
CD_UART2	CSM_UART2	18 MHz/32.768 kHz (*2)	✓	✓	✓	✓	—	✓	—	—
CD_USBI	CSM_USB	48 MHz	—	—	✓	—	—	✓	—	—
CD_ADCC12	CSM_ADCC12	12 MHz/1 MHz	—	✓	✓	✓	✓	✓	✓	✓
CD_ADCC24	CSM_ADCC24	4 MHz	—	✓	✓	—	✓	✓	—	✓

Note: ✓ shows Selectable.

Note: ✓ shows a clock source which is selectable and is selected at the initial state.

Note: — shows Un-selectable.

Note: OSC12M3 indicates OSC12M divided by 3.

Note: PLL3 indicates PLL divided by 3. When using PLL = 24 MHz, it can use.

Note: PLL9 indicates PLL divided by 9. When using PLL = 36 MHz, it can use.

*1: When using CD_PPIER1 = 12 MHz, it is restrained with CD_UART0/1 ≤ 5/3 x CD_PPIER1.

*2: When using CD_PPIER2 = 12 MHz, it is restrained with CD_UART2 ≤ 5/3 x CD_PPIER2.

Table 4.2 Prescaler

Clock Domain	Feature		Default Value	
	Clock Gating	Dividing Ratio 1/n	Clock Gating	Dividing Ratio
CD_MPIER	✓	n = 1,2,3,4,5,6,7,8,9,10,12,18,24,36,48	Not Gated	1
CD_PPIER0	✓	n = 1,2,3,4,5,6,7,8,9,10,12,18,24,36,48	Gated	N/A
CD_PPIER1	✓	n = 1,2,3,4,5,6,7,8,9,10,12,18,24,36,48	Gated	N/A
CD_PPIER2	✓	n = 1,2,3,4,5,6,7,8,9,10,12,18,24,36,48	Gated	N/A
CD_SPIC	✓	n = 1,2,3,4,5,6,7,8,9,10,12,18,24,36,48	Not Gated	1
CD_USBB	✓	n = 1, 2	Gated	N/A
CD_RTC	N/A	N/A	N/A	N/A
CD_CPUTRC	N/A	N/A	N/A	N/A
CD_CPUST	✓	n = 1,2,3,4,5,6,7,8,9,10,12,18,24,36,48	Not Gated	1
CD_PMULV	N/A	N/A	N/A	N/A
CD_UART0	✓	n = 1,2,3,4,5,6,7,8,9,10,12,18,24,36,48	Gated	N/A
CD_UART1	✓	n = 1,2,3,4,5,6,7,8,9,10,12,18,24,36,48	Gated	N/A
CD_UART2	✓	n = 1,2,3,4,5,6,7,8,9,10,12,18,24,36,48	Gated	N/A
CD_USBI	✓	n = 1	Gated	N/A

Clock Domain	Feature		Default Value	
	Clock Gating	Dividing Ratio 1/n	Clock Gating	Dividing Ratio
CD_ADCC12	✓	SIOSC4M: n = 1,2,4 OSC12M: n = 1,2,4,6,12 OSC12M3: n = 1 PLL: n = 2,4,6,8,12,18,24,36,48 PLL3: n = 1 PLL9: n = 1 ADPLL: n = 4,6,8,12,24,48	Gated	N/A
CD_ADCC24	✓	SIOSC4M: n = 1 OSC12M3: n = 1 PLL/ADPLL: n = 6,12 PLL9: n = 1	Gated	N/A

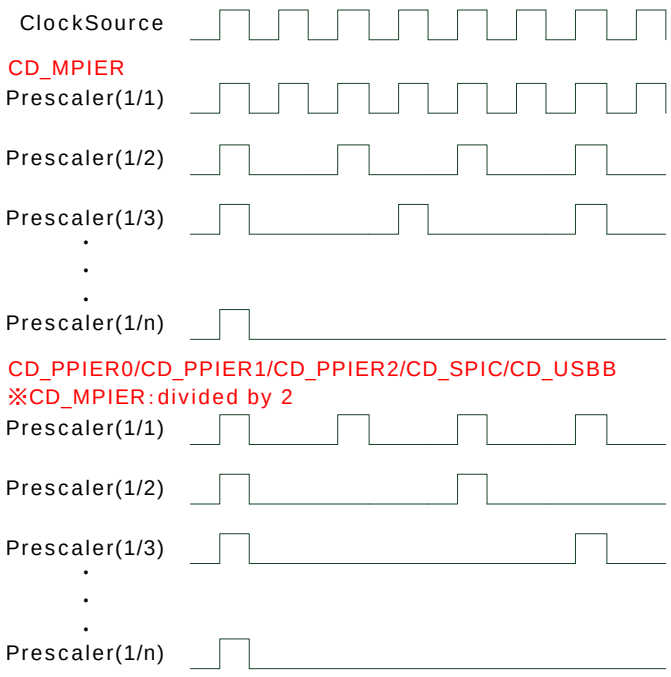

Figure 4.2 Prescaler output (CD_MPIER/CD_PPIER0･1･2/CD_SPIC/CD_USBB)

CD_MPIER : $CLKOUT_{CD\_MPIER} = f_{CSMSEL}/P_{PRESCAL}$

CD_PPIER0･1･2/CD_SPIC/CD_USBB: $CLKOUT = CLKOUT_{CD\_MPIER}/P_{PRESCAL}$

*f_{CSMSEL}: The clock source frequency supplied by CSM_MAIN

*$P_{PRESCAL}$: "n" value determined by PRESCAL which can be specified by the domain

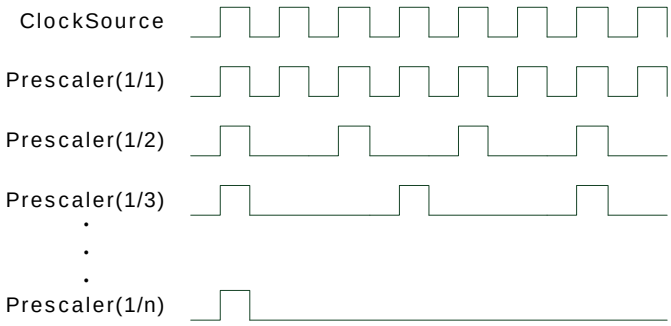

Figure 4.3 Prescaler output (CD_UART0·1·2/CD_CPUST/CD_USBI/CD_ADCC12·24)

$$CLKOUT = f_{CSMSEL}/P_{PRESCAL}$$

*f_{CSMSEL}: The clock source frequency supplied by CSM_MAIN
*$P_{PRESCAL}$: "n" value determined by PRESCAL which can be specified by the domain

4.1.3.1. Maximum operating frequency of each clock domain

Maximum operating frequency of each clock domain is different in each mode of VoltageMode (refer to 4.3.2. VoltageMode),which will be described later. The table below is the maximum operating frequency of each clock domain.

In addition, please check the individual document of each block about the clock constraints of each block.

Table 4.3 Maximum operating frequency of each clock domain

Clock Domain	VoltageMode			
	ModeA	ModeB	ModeC	ModeD
CD_MPIER	48 MHz	36 MHz	12 MHz	4 MHz
CD_PPIER0	12 MHz	9 MHz	4 MHz	4 MHz
CD_PPIER1	12 MHz	9 MHz	4 MHz	4 MHz
CD_PPIER2	12 MHz	9 MHz	4 MHz	4 MHz
CD_SPIC	48 MHz	36 MHz	12 MHz	4 MHz
CD_USBB	48 MHz	—	—	—
CD_RTC	32.768 kHz	32.768 kHz	32.768 kHz	32.768 kHz
CD_CPUTRC	12 MHz	9 MHz	4 MHz	4 MHz
CD_CPUST	12 MHz	12 MHz	4 MHz	1 MHz
CD_PMULV	4 MHz	4 MHz	4 MHz	4 MHz
CD_UART0	16 MHz	12 MHz	4 MHz	4 MHz
CD_UART1	16 MHz	12 MHz	4 MHz	4 MHz
CD_UART2	16 MHz	12 MHz	4 MHz	4 MHz
CD_USBI	48 MHz	—	—	—
CD_ADCC12	12 MHz	9 MHz	4 MHz	4 MHz
CD_ADCC24	4 MHz	4 MHz	4 MHz	4 MHz

* —: inoperable

4.1.4. Clock Source Control

Clock source can starts and stops by software. Each chapter indicates start-up and stop procedures.

4.1.4.1. OSC12M

(Clock start-up procedure)

(1) The start-up signal is asserted.
   – 1 is written to ***[CONFIG_OSC12M]***.
(2) Wait tSTART until the clock is stabilized - Refer to "Technical Data Sheet Hardware Specification 7.5.1 XOSC12M" about tSTART.
(3) The clock start-up completes.

(Clock stop procedure)

(1) The start-up signal is deasserted.
   – 0 is written to ***[CONFIG_OSC12M]***.OSC12M_EN.
(2) The clock stop completes.

4.1.4.2. OSC32K

(Clock start-up procedure)

(1) The start-up signal is asserted.
   – 1 is written to ***[CONFIG_OSC32K]***.OSC32K_EN.
(2) Wait tSTART until the clock is stabilized - Refer to "Technical Data Sheet Hardware Specification 7.5.2 XOSC32K" about tSTART.
(3) The boost signal is disabled for low power consumption.
   – 1 is written to ***[CONFIG_OSC32K]***. OSC32K_BOOST_DISABLE.
(4) Wait tSTBL until the clock is stabilized - Refer to "Technical Data Sheet Hardware Specification 7.5.2 XOSC32K" about tSTBL.
(5) The clock start-up completes.

(Clock stop procedure)

(1) The boost signal is enabled.
   – 0 is written to ***[CONFIG_OSC32K]***. OSC32K_BOOST_DISABLE
(2) The start-up signal is deasserted.
   – 0 is written to ***[CONFIG_OSC32K]***.OSC32K_EN
(3) The clock stop completes.

(Trimming value change procedure)

The trimming value should be changed in the stop state of the clock and the reset state of the used block.

The trimming value can be set up to the EFUSE value or an arbitrary value in the OVERRIDE register. The data indicated to EFUSE is usually used.

*Refer to 4.7. EFUSE Function, for the EFUSE and OVERRIDE registers.

[In the case of using EFUSE data]

(1) The clock stop procedure should be performed if the clock is in the state of operating.
(2) The trimming value indicated to EFUSE is selected.
   – 0 is written to ***[SELECT_EFUSE]***.SEL_EFUSE_OSC32K.
(3) The data of (2) is set.
   – ***[OVERRIDE_EFUSE_OSC32K]*** is written.
   – The preset value of EFUSE selected by (2) is used as the write data.
(4) Changing the trimming value is completed.

[In the case of using an arbitrary value in the OVERRIDE register]

(1) The clock stop procedure should be performed if the clock is in the state of operating.
(2) The OVERRIDE register is selected.
   – 1 is written to ***[SELECT_EFUSE]***.SEL_EFUSE_OSC32K.
(3) OVERRIDE register is set.
   – 0b0000 is written to ***[OVERRIDE_EFUSE_OSC32K]***.OVERRIDE_EFUSE_OSC32K_RSV.
   – An arbitrary value is written to ***[OVERRIDE_EFUSE_OSC32K]***.OVERRIDE_EFUSE_OSC32K_TRIMIN_VREF_GMBIAS.
   – An arbitrary value is written to ***[OVERRIDE_EFUSE_OSC32K]***.OVERRIDE_EFUSE_OSC32K_TRIMIN.
(4) Changing the trimming value is completed.

4.1.4.3. SIOSC4M

Starting or stopping control of SIOSC4M cannot be done by software.

(Trimming value change procedure)

The setting of a trimming value should be performed by software after the Start-up Sequence.

Moreover, after returning from the RTC/STOP state in the power mode mentioned later (refer to 4.3.3.5. RTC/STOP Mode for details), the trimming value needs to be set up again, since it is initialized.

The trimming value can be set up to the EFUSE value or an arbitrary value in the OVERRIDE register. The data indicated to EFUSE is usually used.

*Refer to 4.7. EFUSE Function, for the EFUSE and OVERRIDE registers.

(1) OVERRIDE register is selected.
- 1 is written to ***[SELECT_EFUSE]***.SEL_EFUSE_SiOSC4M.

(2) The trimming value is loaded.
- 1 is written to ***[CONFIG_SiOSC4M]***.SiOSC4M_CTRIM_LAT.

(3) When you set the EFUSE data, read the ***[EFUSE_SiOSC4M]*** register. The setting value changes by the state of VoltageMode (4.3.2. VoltageMode)
The case of ModeA**:** uses ***[EFUSE_SiOSC4M]***.EFUSE_SiOSC4M_CTRIM_MODEA.
The case of ModeB**:** uses ***[EFUSE_SiOSC4M]***.EFUSE_SiOSC4M_CTRIM_MODEB.
The case of ModeC**:** uses ***[EFUSE_SiOSC4M]***.EFUSE_SiOSC4M_CTRIM_MODEC.
The case of ModeD**:** uses ***[EFUSE_SiOSC4M]***.EFUSE_SiOSC4M_CTRIM_MODED.

(4) OVERRIDE register is set.
- The value of (3) or an arbitrary value is written to ***[OVERRIDE_EFUSE_SiOSC4M]***.OVERRIDE_EFUSE_SiOSC4M_CTRIM
- The setting value of the register is used as the write data.

(5) The loading signal of the trimming value is deasserted.
- 0 is written to ***[CONFIG_SiOSC4M]***.SiOSC4M_CTRIM_LAT.

4.1.4.4. SIOSC32K

(Clock start-up procedure)

(1) The start-up signal is asserted.
   – 1 is written to ***[CONFIG_SIOSC32K]***.SIOSC32K_EN.
(2) Wait tSTASO32Kμs until the clock is stabilized - Refer to "Technical Data Sheet Hardware Specification 7.5.2 XOSC32K" about tSTASO32K.
(3) The clock start-up completes.

(Clock stop procedure)

(1) The start-up signal is deasserted.
   – 0 is written to ***[CONFIG_SIOSC32K]***.SIOSC32K_EN.
(2) The clock stop completes.

(Trimming value change procedure)

The trimming value should be changed in the stop state of the clock and the reset state of the used block.

The trimming value can be set up to the EFUSE value or an arbitrary value in the OVERRIDE register. The data indicated to EFUSE is usually used.

* Refer to 4.7. EFUSE Function, for the EFUSE and OVERRIDE registers.

[In the case of using EFUSE data]

(1) The clock stop procedure should be performed if the clock is in the state of operating.
(2) The trimming value indicated to EFUSE is selected.
   – 0 is written to ***[SELECT_EFUSE]***.SEL_EFUSE_SIOSC32K.
(3) The data of (2) is set.
   – ***[OVERRIDE_EFUSE_SIOSC32K]*** is written.
   – The preset value of EFUSE selected by (2) is used as the write data.
(4) Changing the trimming value is completed.

[In the case of using an arbitrary value in the OVERRIDE register]

(1) The clock stop procedure should be performed if the clock is in the state of operating.
(2) The OVERRIDE register is selected.
   – 1 is written to ***[SELECT_EFUSE]***.SEL_EFUSE_SIOSC32K.
(3) OVERRIDE register is set.
   – An arbitrary value is written to ***[OVERRIDE_EFUSE_SIOSC32K]***.OVERRIDE_EFUSE_SIOSC32K_TRIMIN_FREQ.
(4) Changing the trimming value is completed.

4.1.4.5. PLL

(Clock start-up procedure)

(1) OSC12M used as a reference clock should be started up. Refer to 4.1.4.1. OSC12M for details.
(2) If the PLL power supply is in the OFF state, the PLL should be supplied with the power according to the power supply procedure before the clock start-up (4.2.3.7. PPLL Domain control).
(3) The starting signal is changed to the bypass mode.
   – 1 is written to ***[CONFIG_PLL_0]***.PLL_BP.
(4) Wait 100 µs.
(5) The starting signal is changed to the normal mode.
   – 0 is written to ***[CONFIG_PLL_0]***.PLL_BP.
(6) Wait 100 µs until lock-up.
(7) The clock start-up is completed.

(Clock stop procedure)

(1) The starting signal is changed to the bypass mode.
   – 1 is written to ***[CONFIG_PLL_0]***.PLL_BP.
(2) When changing the PPLL domain into the power supply OFF state after the clock stop, the power supply shut-down procedure (4.2.3.7. PPLL Domain control) should be performed.
(3) The reference clock is stopped.
   – 0 is written to ***[CONFIG_OSC12M]***.OSC12M_EN.

* The procedure of (3) should not be followed when OSC12M as a reference clock is used as clock source of the clock domain.

(Change procedure of the multiplied ratio)

Change of the multiplied ratio should be performed in the state of the clock stop.

(1) allow the changes made by the software
   – 1 is written to ***[CONFIG_PLL_0]***.PLL_SWEN.
(2) The starting signal is changed to the bypass mode.
   – 1 is written to ***[CONFIG_PLL_0]***.PLL_BP.
(3) The multiplied ratio is changed.
   – The setting value is written to ***[CONFIG_PLL_1]***.ND.
(4) Perform (3) of the PLL clock start-up procedure and the subsequent ones.
(5) don't allow the changes made by the software
   – 0 is written to ***[CONFIG_PLL_0]***.PLL_SWEN.

4.1.4.6. ADPLL

(Clock start-up procedure)

(1) The reference clock is either SIOSC32K or OSC32K. The clock source of SIOSC32K or OSC32K should be started up. Refer to 4.1.4. Clock Source Control.
(2) If the PADPLL domain is in a power supply OFF state, the PADPLL domain is supplied with the power according to a power supply procedure before the clock start-up (4.2.3.8. PADPLL Domain control).
(3) Set to 32.768 kHz clock for ADPLL - refer to 4.1.7. Setting 32.768 kHz clock.
(4) The starting signal is asserted.
   – 1 is written to ***[CONFIG_ADPLL_0]***.ENPLL.
(5) Wait 8 ms until lock-up.
(6) The clock start-up is completed.

(Clock stop procedure)

(1) The starting signal is deasserted.
   – 0 is written to ***[CONFIG_ADPLL_0]***.ENPLL.
(2) When changing the PADPLL domain into a power supply OFF state after the clock stop, the power supply shut-down procedure (4.2.3.8. PADPLL Domain control) should be performed.
(3) The reference clock is stopped.
   – If the reference clock is OSC32K, please refer to 4.1.4.2 OSC32K.
   – If the reference clock is SISOC32K, please refer to 4.1.4.4 SIOSC32K.

* The procedure of (3) should not be followed when 32.768 kHz as a reference clock is used in the RTC block.

(High-speed lock-up procedure)

When ADPLL is started, the lock-up time can be shortened. When using this mode, it is necessary to fetch the data (NTWDATA) required for a high-speed lock-up before the stop of ADPLL. ADPLL is always updating and outputting NTWDATA with synchronizing the reference clock (= 32.768 kHz).

The data issued by ADPLL is fetched by writing 1 to ***[CONFIG_ADPLL_1]***.ADPLL_NTWOUT_LATEN.

The value is updated with synchronizing the reference clock when the bit is1. Note that the data used for a high-speed lock-up needs to be one after a lock-up.

Since data fetching is performed with synchronizing the reference clock (= 32.768 kHz) of ADPLL, at least 2 clocks @ 32.768 kHz or more are needed to fetch the data.

* The stop refers to such as the clock stop and the power supply OFF.

(1) The starting signal is asserted.
   – 1 is written to ***[CONFIG_ADPLL_0]***.ENPLL.
(2) Wait 100 ns.
(3) The fetch signal is asserted.
   – 1 is written to ***[CONFIG_ADPLL_1]***.NTWMODE.
(4) Wait 100 µs.
(5) The fetch signal is deasserted.
   – 0 is written to ***[CONFIG_ADPLL_1]***.NTWMODE.
(6) Wait 2 ms.

(NTW data fetch)

(1) The fetch signal is asserted after the start-up procedure (4).
   – 1 is written to ***[CONFIG_ADPLL_1]***. ADPLL_NTWOUT_LATEN.
(2) Wait 2 clocks of the reference clock of the ADPLL.

4.1.5. DFS Control

DFS control is performed by the combination of a clock source change and a prescaler setting.

The changing clock source must be done in the state that two clock sources before and after changing are started. When changing clock source, it is necessary that the target clock source is started up and the clock becomes stable in advance. Refer to 4.1.4 Clock Source Control, for the start-up of the clock source.

Depending on the oscillating frequency of the clock source, the setting order of a clock source change and the prescaler setting is changed. The Source oscillating frequency can be checked via a register. Moreover, note that the PLL source oscillating frequency may change according to the set value.

The change of the clock source can be omitted to make only the change of prescaler.

The change of the prescaler can be omitted to make only the change of the clock source.

Control Register	Control	
*[CSM_****]*	Write	The target clock source is specified. For detail, refer to Register specification.
	Read	The setting value which is written can be read.
*[PRESCAL_****]*	Write	The setting value of the dividing ration of the frequency is specified. Refer to Register specification for details.
	Read	The setting value which is written can be read.

Refer to the Reference Manual of each block about some constraints and necessary procedures of it by the change of frequency. It means that there is no constraints about the block described below.

- Refer to the Chapter 5 of the latest TZ1000 Series Reference Manual MCU Processor and core peripherals.
- Refer to the Chapter 4.11 of the latest TZ1000 Series Reference Manual MCU SPI Flash Controller.
- Refer to the Chapter 4.2.3 of the latest TZ1000 Series Reference Manual MCU SRAM Controller.
- Refer to the Chapter 4.3.1 of the latest TZ1000 Series Reference Manual MCU 12-bit Analog to Digital Converter.
- Refer to the Chapter 4.3.1 of the latest TZ1000 Series Reference Manual MCU 24-bit Analog to Digital Converter.
- Refer to the Chapter 5.2.1 of the latest TZ1000 Series Reference Manual MCU USB Device controller.
- Refer to the Chapter 4.5 of the latest TZ1000 Series Reference Manual MCU AES Accelerator.
- Refer to the Chapter 4.4 of the latest TZ1000 Series Reference Manual MCU Random Number Generator.
- Refer to the Chapter 5.14.1 of the latest TZ1000 Series Reference Manual MCU I^2C Master/Slave Interface.
- Refer to the Chapter 5.7.1 of the latest TZ1000 Series Reference Manual MCU Universal asynchronous receiver/transmitter.
- Refer to the Chapter 5.5.1 of the latest TZ1000 Series Reference Manual MCU Timer/Counter.
- Refer to the Chapter 5.11.1 of the latest TZ1000 Series Reference Manual MCU Advanced Timer/Counter.
- Refer to the Chapter 5.4.1 of the latest TZ1000 Series Reference Manual MCU Watchdog Timer.
- Refer to the Chapter 4.9.3 of the latest TZ1000 Series Reference Manual MCU Real Time Clock Counter.
- Refer to the Chapter 6.3 of the latest TZ1000 Series Reference Manual MCU Event Control Block.

(When changed to a low clock source from a high clock source oscillating frequency)

(1) The clock source is changed.
  – ***[CSM_****]***.CSMSEL_**** is written.
(2) The prescaler is changed.
  – ***[PRESCAL_****]***.PRESEL_**** is written.

(When changed to a high clock source from a low clock source oscillating frequency)

(1) The prescaler is changed.
  – ***[PRESCAL_****]***.PRESEL_**** is written.
(2) The clock source is changed.
  – ***[CSM_****]***.CSMSEL_**** is written.

4.1.6. Clock Source Change for CPU TraceClock

The following procedure is needed for changing the CSM_CPUTRC. Although the SIOSC4M is always operating, the OSC12M may stop. When the change target is the OSC12M, perform starting it up in advance.

(The change to the OSC12M from the SIOSC4M)

(1) The CPU TraceClock supply is stopped.
  – 1 is written to ***[CG_ON_PC_SCRT]***. CG_cputrcclk_cpu_traceclk.
(2) The clock source is changed to the OSC12M.
  – 1 is written to ***[CSM_CPUTRC]***.CSMSEL_CPUTRC.
(3) The CPU TraceClock supply is resumed.
  – 1 is written to ***[CG_OFF_PC_SCRT]***. CG_cputrcclk_cpu_traceclk.

(The change to the SIOSC4M from OSC12M)

(1) The CPU TraceClock supply is stopped.
  – 1 is written to ***[CG_ON_PC_SCRT]***. CG_cputrcclk_cpu_traceclk.
(2) The clock source is changed to the SIOSC4M.
  – 0 is written to ***[CSM_CPUTRC]***.CSMSEL_CPUTRC.
(3) The CPU TraceClock supply is resumed.
  – 1 is written to ***[CG_OFF_PC_SCRT]***. CG_cputrcclk_cpu_traceclk.
(4) The OSC12M is stopped if it is not used in other blocks.
  – Refer to 4.1.4. Clock Source Control, for the clock stop procedure.

4.1.7. Setting 32.768 kHz clock

Refer to 4.1.4. Clock Source Control, for the start-up procedure of the clock source.

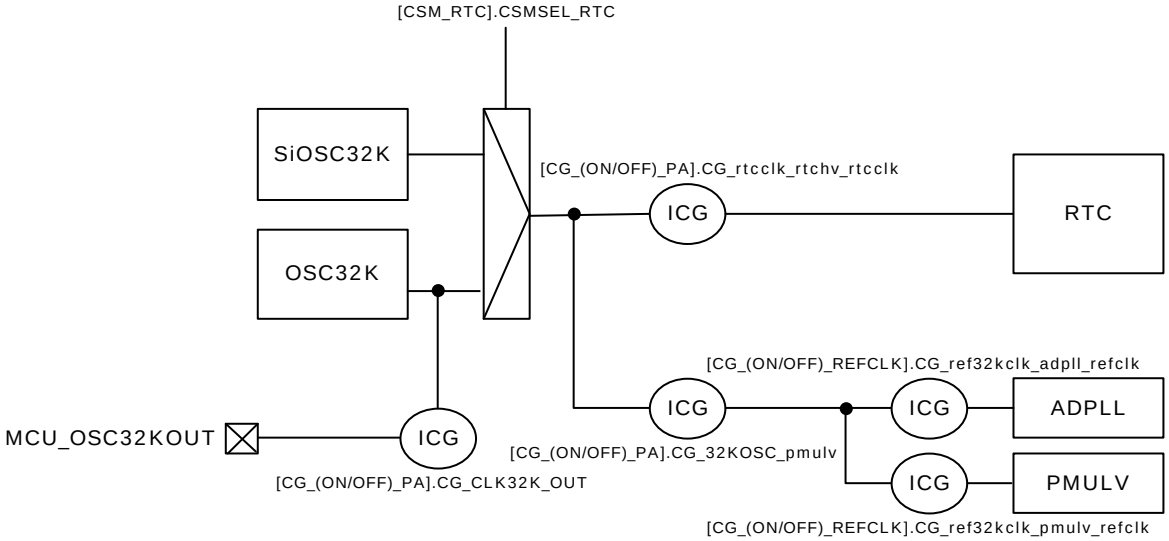

Figure 4.4 Peripheral circuit structure of the CSM_RTC

Before changing, the reset or clock gating should be performed to the modules which are operating with the 32.768 kHz clock. Start-up of the target clock source should be also performed in advance.

(The change to the SIOSC32K from OSC32K)

(1) The clock supply after selection of the OSC32K and the SIOSC32K is stopped before the change.
   – 1 is written to ***[CG_ON_PA]***.CG_rtcclk_rtchv_rtcclk.
   – 1 is written to ***[CG_ON_PA]***.CG_32KOSC_pmulv.
(2) The clock source is changed to the SIOSC32K.
   – 1 is written to ***[CSM_RTC]***.CSMSEL_RTC.
(3) The OSC32K is stopped. Refer to 4.1.4 Clock Source Control, for the clock stop procedure.

(The change to the OSC32K from SIOSC32K)

(1) 32.768 kHz clock supply after selection of the OSC32K or the SIOSC32K is stopped before the change.
   – 1 is written to ***[CG_ON_PA]***.CG_rtcclk_rtchv_rtcclk.
   – 1 is written to ***[CG_ON_PA]***.CG_32KOSC_pmulv.
(2) The clock source is changed to the OSC32K.
   – 0 is written to ***[CSM_RTC]***.CSMSEL_RTC.
(3) The SIOSC32K is stopped. Refer to 4.1.4. Clock Source Control, for the clock stop procedure.

(32.768 kHz Clock for RTC supply procedure)

(1) When the changing the clock source is required in advance, perform (The change to the SIOSC32K from OSC32K) or (The change to the OSC32K from SIOSC32K).
(2) Start the clock supply.
   – 1 is written to ***[CG_OFF_PA]***.CG_rtcclk_rtchv_rtcclk.
(3) Perform the RTC start-up procedure - refer to RTC document.

(32.768 kHz Clock for ADPLL supply procedure)

(1) When the changing the clock source is required in advance, perform (The change to the SIOSC32K from OSC32K) or (The change to the OSC32K from SIOSC32K).

(2) Start the clock supply.
   - 1 is written to ***[CG_OFF_PA]***.CG_32KOSC_pmulv.
   - 1 is written to ***[CG_OFF_REFCLK]***.CG_ref32kclk_adpll_refclk.

(3) Perform the ADPLL start-up procedure - refer to 4.1.4.6. ADPLL.

(32.768 kHz Clock for PMULV supply procedure)

It is possible to operate at 32.768 kHz in the clock domain other than CSM_RTC.

(1) When the changing the clock source is required in advance, perform (The change to the SIOSC32K from OSC32K) or (The change to the OSC32K from SIOSC32K).

(2) Start the clock supply.
   - 1 is written to ***[CG_OFF_PA]***.CG_32KOSC_pmulv.
   - 1 is written to ***[CG_OFF_REFCLK]***.CG_ref32kclk_pmulv_refclk.

(3) Perform the DFS control - refer to4.1.5 DFS Control.

When the blocks other than RTC use 32.768 kHz clock or transit RETENTION mode, must be changed to the clock source other than 32.768 kHz clock source and stop 32.768 kHz clock. When it use 32.768 kHz clock at the RETENTION mode, it cannot return from the RETENTION state correctly.

4.1.8. MCU_OSC32KOUT Control

The 32.768 kHz clock generated by the OSC32K can be supplied to the external via a pin. The clock supply is stopped as default.

(Clock supply procedure)

1 is written to ***[CG_OFF_PA]***.CG_CLK32K_OUT.

(Clock stop procedure)

1 is written to ***[CG_ON_PA]***.CG_CLK32K_OUT.

4.1.9. Reset Control

4.1.9.1. Software Reset

The reset of each block can be controlled by software. After reset deasserted, it takes time until reset state is reflected. It can access to the block after 4 cycles in the operating frequency of it, if set and read the *[SRST_OFF_AA_BB]* register.

Control Register	Control		
[SRST_ON_AA_BB]	Write	1: Reset asserted	0: Ignored
	Read	1: Reset asserting	0: Reset deasserting
[SRST_OFF_AA_BB]	Write	1: Reset deasserted	0: Ignored
	Read	1: Reset deasserting	0: Reset asserting

* The initial value is not the same in all power supply domains.
* AA: The name of the power supply domain, BB: Number

Control Register	Control		
[SRST_ON_POWERDOMAIN]	Write	1: Reset asserted	0: Ignored
	Read	1: Reset asserting	0: Reset deasserting
[SRST_OFF_POWERDOMAIN]	Write	1: Reset deasserted	0: Ignored
	Read	1: Reset deasserting	0: Reset asserting

* The initial value is not the same in all power supply domains.

4.1.9.2. Hardware reset

The whole chip is reset by asserting the MCU_SYS_RESET_N which is an external pin. If it is deasserted, the Power Supply Sequence and the Start-up Sequence are performed in the order, and the boot starts.

4.1.9.3. WDT reset

If the reset from the WDT block is asserted, the PMULV will return to the power supply sequence and the reboot starts.

Since the *[STATUS_LVRST]* register is not initialized, the reboot cause can be known by referring to this register after the reboot.

4.1.9.4. LOCKUP reset

If the LOCKUP signal is asserted from the CPU block, it will return to the power supply sequence like the WDT reset.

4.1.9.5. SYSRESETREQ reset

If the SYSRESETREQ signal is asserted from the CPU block, it will return to the power supply sequence like the WDT reset.

4.1.9.6. BrownOut reset

Refer to 4.5. BrownOut Control for details. If the BrownOut reset is asserted, it will return to the power supply sequence. However, note that it does not carry out the reboot, unlike the WDT/LOCKUP/SYSRESETREQ reset.

The hardware reset is required for the reboot. The cause can be known by referring to ***[STATUS_LVRST]*** after the hardware reset.

4.1.9.7. WDT/LOCKUP/SYSRESETREQ reset in the debugger connection

When it is connected to the debugger and set ***[CTRL_CDBGPWRUPREQ]***.CDBGPWRUPREQ_EN to 1,

- WDT reset: The CPU core and WDT is only reset without reboot.
- LOCKUP reset: The CPU core is only reset without reboot.
- SYSRESETREQ reset: The CPU core is only reset without reboot.

4.1.9.8. Reset Cause Summary

The following table shows the classification of each blocks and the registers in the PMULV/PMUHV initialized by each reset cause.

* The PMULV/PMUHV does not have registers reset by software unlike the other blocks.

	HW Reset	WDT Reset	LOCKUP Reset	SYSRESETREQ Reset	BrownOut Reset
The Debugger is not connected or is connected and ***[CTRL_CDBGPWRUPREQ]***.CDBGPWRUPREQ_EN = 0					
the blocks except for PMU	✓	✓	✓	✓	✓
PMULV	✓	✓	✓	✓	✓
the control in the PMUHV	✓	✓	✓	✓	✓
the register in the PMUHV	For the registers in the PMUHV, refer to the following.				
RTC registers related ***[CG_(ON/OFF)_PA]*** ***[SRST_(ON/OFF)_PA]*** ***[CSM_RTC]*** ***[RTCLV_RSYNC_SETTING]*** ***[CONFIG_OSC32K]*** ***[CONFIG_SiOSC32K]*** ***[OVERRIDE_EFUSE_OSC32K]*** ***[OVERRIDE_EFUSE_SiOSC32K]*** ***[STATUS_LVRST]***. STATUS_LVRST_cpu_SYSRESETREQ ***[STATUS_LVRST]***. STATUS_LVRST_cpu_LOCKUP ***[STATUS_LVRST]***. STATUS_LVRST_wdt_wdtResetout ***[IRQ_SETTING_1]***. IRQ_RTCHVWAKEUP_setting ***[IRQ_STATUS]***. IRQ_RTCHVWAKEUP_setting ***[WAKEUP_EN]***. WAKEUP_RTCHVWAKEUP_enable ***[WAKEUP_STATUS]***. WAKEUP_RTCHVWAKEUP_status	✓	—	—	—	✓

IO control related ***[CTRL_IO_AON_number]***	✓	✓	✓	✓	✓
PowerDomain control ***[PSW_AA]*** (*1) ***[PSW_BB]*** (*2)	✓	✓	✓	✓	✓
HardMacro control related ***[CONFIG_SiOSC4M]*** ***[CONFIG_DCDC_HVREG]*** ***[CONFIG_LVD_0]*** ***[CONFIG_LDOM_number]*** ***[CONFIG_LDOS_number]*** ***[OVERRIDE_EFUSE_SiOSC4M]*** ***[OVERRIDE_EFUSE_BGR_number]***	✓	✓	✓	✓	✓
BrownOut related ***[IRQ_SETTING_1]***. IRQ_BROWNOUT_setting ***[IRQ_STATUS]***. IRQ_BROWNOUT ***[WAKEUP_EN]***. WAKEUP_BROWNOUT_enable ***[WAKEUP_STATUS]***. WAKEUP_BROWNOUT_status	✓	—	—	—	✓
[BROWNOUTMODE]	✓	—	—	—	—
[STATUS_LVPWR]	✓	✓	✓	✓	✓
[STATUS_LVRST].STATUS_LVRST_BOR	—	—	—	—	—
[STATUS_LVRST]. STATUS_LVRST_IO_SYS_RESET_N	✓	—	—	—	—
[STATUS_LVRST].STATUS_LVRST_RTC ***[STATUS_LVRST]***.STATUS_LVRST_STOP	✓	✓	✓	✓	✓
Interrupt control related ***[IRQ_SETTING_0]***. IRQ_GPIOCC_setting (*3) ***[IRQ_SETTING_1]***. IRQ_GPIOCC_setting (*3) ***[IRQ_SETTING_1]***. IRQ_CPU_DEBUGIN ***[IRQ_STATUS]*** .IRQ_GPIOCC (*3) ***[IRQ_STATUS]***. IRQ_CPU_DEBUGIN ***[WAKEUP_EN]***. WAKEUP_GPIOCC_enable (*3) ***[WAKEUP_EN]***. WAKEUP_CPU_DEBUGIN_enable ***[WAKEUP_STATUS]***. WAKEUP_GPIOCC_status (*3) ***[WAKEUP_STATUS]***. WAKEUP_CPU_DEBUGIN_status	✓	✓	✓	✓	✓
The Debugger is connected and ***[CTRL_CDBGPWRUPREQ]***.CDBGPWRUPREQ_EN=1					
CPU(core)	✓	✓	✓	✓	✓
CPU(other)	✓	—	—	—	✓
WDT	✓	✓	—	—	✓
The other block	✓	—	—	—	✓

✓: initialized —: not initialized

*1: "AA" indicates PU, EFUSE, PLL, ADPLL, IO_USB and HARDMACRO

*2: "BB" indicates PU, EFUSE, PLL and ADPLL.

*3: "CC" indicates the number of GPIO.

4.1.10. Clock Gating Control

It is possible to change the clock gating by register access. The clock gating is required at the power supply control and the low power consumption.

The clock gating mechanism is prepared also per power supply domain, and when carrying out clock gating at the power supply control, all clocks in a domain can be controlled collectively.

After clock-gating deasserted, it takes time until clock-gating state is reflected. It can access to the block after 2cycles in the operating frequency of it, if set and read the *[CG_OFF_AA_BB]* register.

Control Register	Control		
[CG_ON_AA_BB]	Write	1: Clock stopped	0: Ignored
	Read	1: Clock stopping	0: Clock supplying
[CG_OFF_AA_BB]	Write	1: Clock supplied	0: Ignored
	Read	1: Clock supplying	0: Clock stopping

* The initial value is not the same in all power supply domains.

* AA: The name of the power supply domain, BB: Number

Control Register	Control		
[CG_ON_POWERDOMAIN]	Write	1: Clock stopped	0: Ignored
	Read	1: Clock stopping	0: Clock supplying
[CG_OFF_POWERDOMAIN]	Write	1: Clock supplied	0: Ignored
	Read	1: Clock supplying	0: Clock stopping

* The initial value is not the same in all power supply domains.

4.1.10.1. Dynamic Clock Gating

Dynamic clock gating is a hardware mechanism which performs clock supply only during operation. There are two kinds of dynamic clock gating.

- Bus transaction detection
  - Issue of the transaction from the master performs clock supply for the target slave block and the bus. It is stopped by the end of the transaction.
- Clock supply request from the master/slave block
  - Clock supply is required by the master/slave block when a setting to the start-up register and an interrupt occurs. The clock supply is continued while the request is issued.

The dynamic clock gating function can be controlled by the following register. The function ON is set by software if needed. It should be noted that the register for ON/OFF is not separated unlike the clock gating or the software reset registers.

Control Register	Control		
[DCG_AA]	Write	1: Function ON	0: Function OFF
	Read	1: Function ON	0: Function OFF

* The initial value is the function OFF.
* AA: The name of the power supply domain

Control Register	Control		
[DCG_POWERDOMAIN]	Write	1: Function ON	0: Function OFF
	Read	1: Function ON	0: Function OFF

* The initial value is the function OFF.

4.1.11. Clock Gating Control Linked to Reset Control

When a reset is asserted, the target clock also stops. It is required to supply the clock for enabling this function. If the clock is supplied, the reset enables controlling the clock stop.

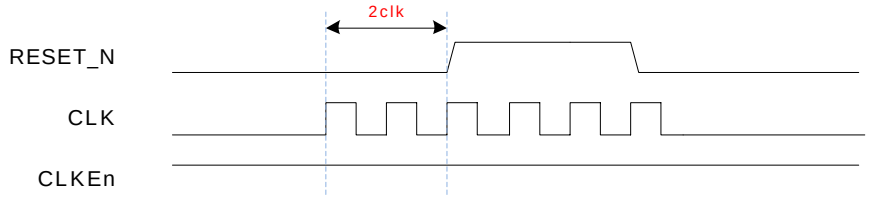

Figure 4.5 Clock Gating Control linked to Reset Control

The following table shows the clock and reset state by the SRST, the CG, and the DCG registers.

Table 4.4 Clock and Reset state

SRST	CG	DCG	Clock	Reset
Reset	—	—	Gating	Reset
Release	Gating	—	Gating	Release
	Release	Valid	Release	Release
		Invalid	Release	Release

* The SRST/CG/DCG are the setting registers.

4.2. Power Control

4.2.1. Power Circuit

The PMU includes 3 power circuits.

- DC-DC
  - Voltage range: 1.0/1.1/1.2 V
- LDOM
  - Voltage: 0.9/1.0/1.1 V
- LDOS
  - Voltage: 0.9 V
- LDOF
  - Voltage: 1.7 V
  - The LDOF is the dedicated IO power supply in the PF domain - refer to 4.2.2. Power Supply Domain.

4.2.2. Power Supply Domain

16 power domains and 4 power stats are supported.

(Power state)

- ON: Power supply ON.
- OFF: Power supply OFF.
- RET: Retention state.
  - 2 power supplies are used for the retention state. A power for Flip-flop circuits or SRAM memory cells is always supplied (a retention power supply) and the normal power supply for the other circuits. In the retention state, the normal power supply is shut down to reduce the power consumption. The return time is longer because of the power shut-down.
- WAIT: Wait state.
  - This state is only for the SRAM. The operation in this state is the same as that in the retention state. Both powers are supplied, so the power consumption is bigger but the return time is shorter.

When the PEFUSE, PPLL, or PADPLL is not used, it should be OFF by software.

Table 4.5 Power domain

Domain	Abbreviation	Voltage	Source	State	Description
POWER_CPU	PC	0.9 V 1.0 V 1.1 V 1.2 V	LDOS DCDC	ON/OFF/RET	CPU power domain
POWER_USB	PU			ON/OFF	USB power domain
POWER_FLASH	PF			ON/OFF/RET	Flash power domain
POWER_SRAM0	PS0			ON/OFF/RET/WAIT	SRAM0 power domain
POWER_SRAM1	PS1			ON/OFF/RET/WAIT	SRAM1 power domain
POWER_SRAM2	PS2			ON/OFF/RET/WAIT	SRAM2 power domain
POWER_DMAC	PD			ON/OFF/RET	DMAC power domain
POWER_ENCRYPT	PE			ON/OFF/RET	ENCRYPT power domain
POWER_PPEIR1	PP1			ON/OFF/RET	PPIER1 power domain
POWER_ADCC12	PA12			ON/OFF/RET	ADCC12 power domain
POWER_ADCC24	PA24			ON/OFF/RET	ADCC24 power domain
POWER_MAIN	PM			ON/OFF/RET	Main power domain
POWER_EFUSE	PEFUSE			ON/OFF	EFUSE power domain
POWER_PLL	PPLL			ON/OFF	PLL power domain
POWER_ADPLL	PADPLL			ON/OFF	ADPLL power domain
POWER_AlwaysON	PA	3.3 V	Battery	ON/OFF	AlwaysOn power domain

* State: The states available.
  ON: Power supply ON, OFF: Power supply OFF, RET: Retention state, WAIT: Wait state.
* The power supply of the PU is 1.2 V only.

4.2.3. Power Domain Control

2 power controls are supported.

- Power shut-down and return control
- Retention transition and return control

The power domain controls are not the same for all domains. Refer to Table 4.5.

All power domains except the PM domain can be controlled separately by software.

4.2.3.1. Power Shut-down and Return Control

The power shut-down control executes the transition from the Power supply ON state to the Power supply OFF state of an power domain. And the return control executes the transition from the Power supply OFF state to the Power supply ON state.

After the transition from the power OFF to ON, the domain is in the reset state and the re-setting in the domain is necessary.

4.2.3.2. Retention Transition and Return Control

The transition to the retention state or the return from the state maintains the data because of the retention power supply ON. After the return, no re-setting is necessary.

4.2.3.3. PM Domain Control

Software cannot control the power supply of the PM domain, hardware only.

4.2.3.4. PU Domain Control

The power of the PU domain is controlled by software. The control is the power shut-down and its return only. The procedure is shown as follows. It is noted that the PU domain operates at only 1.2 V power supply.

(Power supply procedure)

(1) The PU domain is supplied with 1.2 V power.
   (a) ***[PSW_PU]***.PSW_PU_VDDCW should be written to 1.
   (b) ***[PSW_PU]***.PSW_PU_VDDCS should be written to 1.
   * These fields should not be written at the same time.
   * ***[PSW_PU]***.PSW_PU_VDDCW should be done first.

(2) The PU domain is supplied with 3.3 V power.
   (a) ***[PSW_IO_USB]***.PSW_IO_USB_VDDCW should be written to 1.
   (b) ***[PSW_IO_USB]***.PSW_IO_USB_VDDCS should be written to 1.
   * These fields are not written at the same time.
   * ***[PSW_IO_USB]***.PSW_IO_USB_VDDCW should be done first.

(3) The isolation signals are released for the PU domain.
   – ***[ISO_PU]***.INISOEN_PU should be written to 0.
   – ***[ISO_PU]***.OUTISOEN_PU should be written to 0.
   – These fields can be written without any restrictions for the order of the writes.

(4) If the USB2FS starts up next, its own start-up procedure should be done. For detail, refer to the USB2FS specification.

(Power shut-down procedure)

(1) The stop procedure of the USB2FS should be executed to stop the clock and to assert the reset.

(2) The isolation for the PU domain is done.
- ***[ISO_PU]***.INISOEN_PU should be written to 1.
- ***[ISO_PU]***.OUTISOEN_PU should be written to 1.
- These fields can be written without any restrictions for the order of the writes.

(3) 3.3 V power supply for the PU domain is shut down.
(a) ***[PSW_IO_USB]***.PSW_IO_USB_VDDCS should be written to 0.
(b) ***[PSW_IO_USB]***.PSW_IO_USB_VDDCW should be written to 0.
* These fields should not be written at the same time.
* ***[PSW_IO_USB]***.PSW_IO_USB_VDDCS should be done first.

(4) 1.2 V power supply for the PU domain is shut down.
(a) ***[PSW_PU]***.PSW_PU_VDDCS should be written to 0.
(b) ***[PSW_PU]***.PSW_PU_VDDCW should be written to 0.
* These fields should not be written at the same time.
* ***[PSW_PU]***.PSW_PU_VDDCS should be done first.

(5) The power shut-down completes.

4.2.3.5. PF/PC/PD/PS0/PS1/PS2/PE/PP1/PA12/PA24 Domain Control

These domains can be controlled separately by software. The procedure is as follows.

(1) Confirm that the VoltageMode is not in operation.
- Read the ***[MOVE_VOLTAGE_START]***.START and confirm the value is 0.

(2) Confirm the completion of the power domain control.
- ***[POWERDOMAIN_CTRL]***.START_[Power domain] is read and the value is confirmed to be 0.

(3) Set the transition mode for a power domain.
- Set ***[POWERDOMAIN_CTRL_MODE]***.PDMODE_[Power domain].

(4) In the case of the PP1 domain, if is not set to pull-up or pull-down about the input terminal, set to the standby state in order to prevent flow-through current. For the IO Control, refer to Section 4.6.
- When the InputBuffer is transited to the standby state, ***[CTRL_IO_AON_6]***.CTRL_IO_[Block]_STBX should be set to 0.

(5) The power domain control starts up.
- ***[POWERDOMAIN_CTRL]***.START_[Power domain] should be written to 1.

(6) Confirm the completion of the power domain control (only when transited to the power ON state).
- ***[POWERDOMAIN_CTRL]***.START_[Power domain] is read and the value is confirmed to be 0.
- Wait for time depending on the capacitance of the capacitor put to MCU_VDD18_SPIF_OUT (only when MCU_BOOTMODE3 is 0 and the state of the PF domain is ON).
  - When put the 5 µF (current recommended value) including the 1 µF inside PKG, wait for time obtained by substracting the time set to the ***[WAITTIME_LDOF]***.WAITTIME_LDOF_PWON register from 1.5 ms.

(7) The power domain control completes.

Multiple domain controls can be started up simultaneously with the two following restrictions.
- The PS0, PS1, and PS2 should not be started up simultaneously.
- More than 3 power domains should not be started up simultaneously.

If the PF domain control will be done during the SPIC operation, the stop procedure of the SPIC should be executed before it.

The power transition time about the PS0, PS1 and PS2 power domain can control by the ***[WAITTIME_PSW]*** register.

4.2.3.6. PEFUSE Domain Control

The control for the PEFUSE domain is the power shut-down and its return only. The power should be shut down by software after the Start-up Sequence, the power mode transition control described later, and the return from the RTC/STOP mode to reduce power consumption.

The information in the PEFUSE domain is stored in a shift register in the PM domain by the Start-up Sequence. It is forbidden that the PEFUSE domain is in the power supply ON state again.

(Power shut-down procedure)

(1) Signal isolation is done.
- ***[ISO_EFUSE]***.INISOEN_EFUSE should be written to 1.
- ***[ISO_EFUSE]***.OUTISOEN_EFUSE should be written to 1.
- These fields can be written without any restrictions for the order of the writes.

(2) The power supply of the PEFUSE domain is shut down.
   (a) ***[PSW_EFUSE]***.PSW_EFUSE_VDDCS should be written to 0.
   (b) ***[PSW_EFUSE]***.PSW_EFUSE_VDDCW should be written to 0.
   * These fields should not be written at the same time.
   * ***[PSW_EFUSE]***.PSW_EFUSE_VDDCS should be done first.

4.2.3.7. PPLL Domain control

The control for the PPLL domain is the power shut-down and its return only.

When the power mode transit to the WAIT/WAIT-RETENTION/RETENTION state (described later: Power Mode Transition Control), the power supply is shut down by hardware. At the return from the state, the power is not supplied automatically, so this domain should be in the power supply ON state by software.

(Power supply procedure)

(1) The PPLL domain is supplied with the power.
   (a) ***[PSW_PLL]***.PSW_PLL_VDDCW should be written to 1.
   (b) ***[PSW_PLL]***.PSW_PLL_VDDCS should be written to 1.
   * These fields should not be written at the same time.
   * ***[PSW_PLL]***.PSW_PLL_VDDCW should be done first.

(2) Isolation is released.
- ***[ISO_PLL]***.INISOEN_PLL should be written to 0.
- ***[ISO_PLL]***.OUTISOEN_PLL should be written to 0.
- These fields can be written without any restrictions for the order of the writes.

(3) When the PLL is used after the return, the OSC12M start-up (4.1.4.1. OSC12M) and the PLL start-up (4.1.4.5. PLL) should be done in the order.

(Power shut-down procedure)

(1) The clock stop procedure is executed. For detail, refer to 4.1.4.5. PLL.

(2) Signal isolation is done.
- ***[ISO_PLL]***.INISOEN_PLL should be written to 1.
- ***[ISO_PLL]***.OUTISOEN_PLL should be written to 1.
- These fields can be written without any restrictions for the order of the writes.

(3) The power supply of the PPLL domain is shut down.
   (a) ***[PSW_PLL]***.PSW_PLL_VDDCS should be 0.
   (b) ***[PSW_PLL]***.PSW_PLL_VDDCW should be 0.
   * These fields should not be written at the same time.
   * ***[PSW_PLL]***.PSW_PLL_VDDCS should be done first.

4.2.3.8. PADPLL Domain control

The control for the PADPLL domain is the power shut-down and its return only.

When the power mode transit to the WAIT/WAIT-RETENTION/RETENTION state (described later), the power supply is shut down by hardware. At the return from the state, the power is not supplied automatically, so this domain should be in the power supply ON state by software.

(Power supply procedure)

(1) The PADPLL domain is supplied with the power.
   (a) ***[PSW_ADPLL]***.PSW_ADPLL_VDDCW should be written to 1.
   (b) ***[PSW_ADPLL]***.PSW_ADPLL_VDDCS should be written to 1.
   * These fields should not be written at the same time.
   * ***[PSW_ADPLL]***.PSW_ADPLL_VDDCW should be done first.
(2) Wait for 150 μs
(3) Isolation is released.
   – ***[ISO_ADPLL]***.INISOEN_ADPLL should be written to 0.
   – ***[ISO_ADPLL]***.OUTISOEN_ADPLL should be written to 0.
   – These fields can be written without any restrictions for the order of the writes.
(4) When the ADPLL is used after the return, the power supply to the PADPLL domain, 32.768 kHz clock supply, and the ADPLL start-up (4.1.4.6. ADPLL) should be done in the order.

(Power shut-down procedure)

(1) The clock stop procedure is executed. For detail, refer to 4.1.4.6 ADPLL.
(2) Signal isolation is done.
   – ***[ISO_ADPLL]***.INISOEN_ADPLL should be written to 1.
   – ***[ISO_ADPLL]***.OUTISOEN_ADPLL should be written to 1.
   – These fields can be written without any restrictions for the order of the writes.
(3) The power supply of the ADPPLL domain is shut down.
   (a) ***[PSW_ADPLL]***.PSW_ADPLL_VDDCS should be written to 0.
   (b) ***[PSW_ADPLL]***.PSW_ADPLL_VDDCW should be written to 0.
   * These fields should not be written at the same time.
(4) ***[PSW_ADPLL]***.PSW_ADPLL_VDDCS should be done first.

4.2.4. Sensor Power Supply Pin Control

The sensor power is supplied by the MCU. The power supply ON or OFF can be controlled by software.

The power mode transition control maintains the power state in the ACTIVE mode - for example, a transiting to the STOP mode from the ACTIVE mode in the power supply ON state maintains the power supply ON state.

4.2.4.1. Gyroscope Power Supply Pin Control (MCU_VDD33_GYRO_OUT)

(Power supply control)

(1) The power is supplied.
   (a) ***[PSW_HARDMACRO]***.PSW_GYRO_VDDCW should be written to 1.
   (b) 70 µs wait time is necessary for the power to become stable.
   (c) ***[PSW_HARDMACRO]***.PSW_GYRO_VD DCS should be written to 1.
   * These fields should not be written at the same time.
   * ***[PSW_HARDMACRO]***.PSW_GYRO_VDDCW should be done first.
(2) The Gyroscope start-up procedure is executed.

(Power shut-down procedure)

(1) The Gyroscope stop procedure is executed.
(2) The power supply is shut down.
   (a) ***[PSW_HARDMACRO]***.PSW_GYRO_VDDCS should be written to 0.
   (b) ***[PSW_HARDMACRO]***.PSW_GYRO_VD DCW should be written to 0.
   * These fields should not be written at the same time.
   * ***[PSW_HARDMACRO]***.PSW_GYRO_VDDCS should be done first.

4.2.4.2. Magnetometer Power Supply Pin Control (MCU_VDD33_MAG_OUT)

(Power supply control)

(1) The power is supplied.
   (a) ***[PSW_HARDMACRO]***.PSW_MAG_VDDCW should be written to 1.
   (b) 70 µs wait time is necessary for the power to become stable.
   (c) ***[PSW_HARDMACRO]***.PSW_MAG_VD DCS should be written to 1.
   * These fields should not be written at the same time.
   * ***[PSW_HARDMACRO]***.PSW_MAG_VDDCW should be done first.
(2) The Magnetometer start-up procedure is executed.

(Power shut-down procedure)

(1) The Magnetometer stop procedure is executed.
(2) The power supply is shut down.
   (a) ***[PSW_HARDMACRO]***.PSW_MAG_VDDCS should be written to 0.
   (b) ***[PSW_HARDMACRO]***.PSW_MAG_VD DCW should be written to 0.
   * These fields should not be written at the same time.
   * ***[PSW_HARDMACRO]***.PSW_MAG_VDDCS should be done first.

4.2.4.3. Accelerometer Power Supply Pin Control (MCU_VDD33_ACC_OUT)

(Power supply control)

(1) The power is supplied.
   (a) ***[PSW_HARDMACRO]***.PSW_ACC_VDDCW should be written to 1.
   (b) 110 µs wait time is necessary for the power to become stable.
   (c) ***[PSW_HARDMACRO]***.PSW_ACC_VD DCS should be written to 1.
   * These fields should not be written at the same time.
   * ***[PSW_HARDMACRO]***.PSW_ACC_VDDCW should be done first.
(2) The Accelerometer start-up procedure is executed.

(Power shut-down procedure)

(1) The Accelerometer stop procedure is executed.
(2) The power supply is shut down.
   (a) ***[PSW_HARDMACRO]***.PSW_ACC_VDDCS should be written to 0.
   (b) ***[PSW_HARDMACRO]***.PSW_ACC_VD DCW should be written to 0.
   * These fields should not be written at the same time.
   * ***[PSW_HARDMACRO]***.PSW_ACC_VDDCS should be done first.

4.2.4.4. SPI Flash Memory Power Supply Pin Control

SPI Flash Memory can be powered-on/off in the PF power domain control.

4.3. Power Mode Transition Control

Two power modes are supported. It is not possible to start up these mode at the same time.

- VoltageMode
  - 4 modes are defined with the power and the voltage. The transition among these modes is possible.
    - ModeA: The DCDC is used, and the voltage is 1.2 V. The maximum frequency is 48 MHz.
    - ModeB: The DCDC is used, and the voltage is 1.1 V. The maximum frequency is 36 MHz.
    - ModeC: The DCDC is used, and the voltage is 1.0 V. The maximum frequency is 12 MHz.
    - ModeD: The LDOS is used, and the voltage is 0.9 V. The maximum frequency is 4 MHz.
  - ***[VOLTAGEMODE_SETTING]*** register control the voltage circuit about ModeB, ModeC, and ModeD.
  - The write 1 to ***[MOVE_VOLTAGE_START]***.START by software starts up these modes.
  - The maximum frequency is determined in each mode. The DFS control should be done to prevent the operation frequency from exceeding the maximum frequency.

- PowerMode
  - 9 modes are supported.
  - The transition to all modes is through the ACTIVE mode.
  - The return destination is always the ACTIVE mode. The other modes cannot be the destination.
  - The transition in the PowerMode is triggered when the CPU becomes the WFI state. The transition is controlled by ***[MOVE_VOLTAGE_MO DE]***.POWER_MODE.
  - The return in the PowerMode is triggered by an interrupt request to the CPU. The destination mode of the return is the ACTIVE mode.

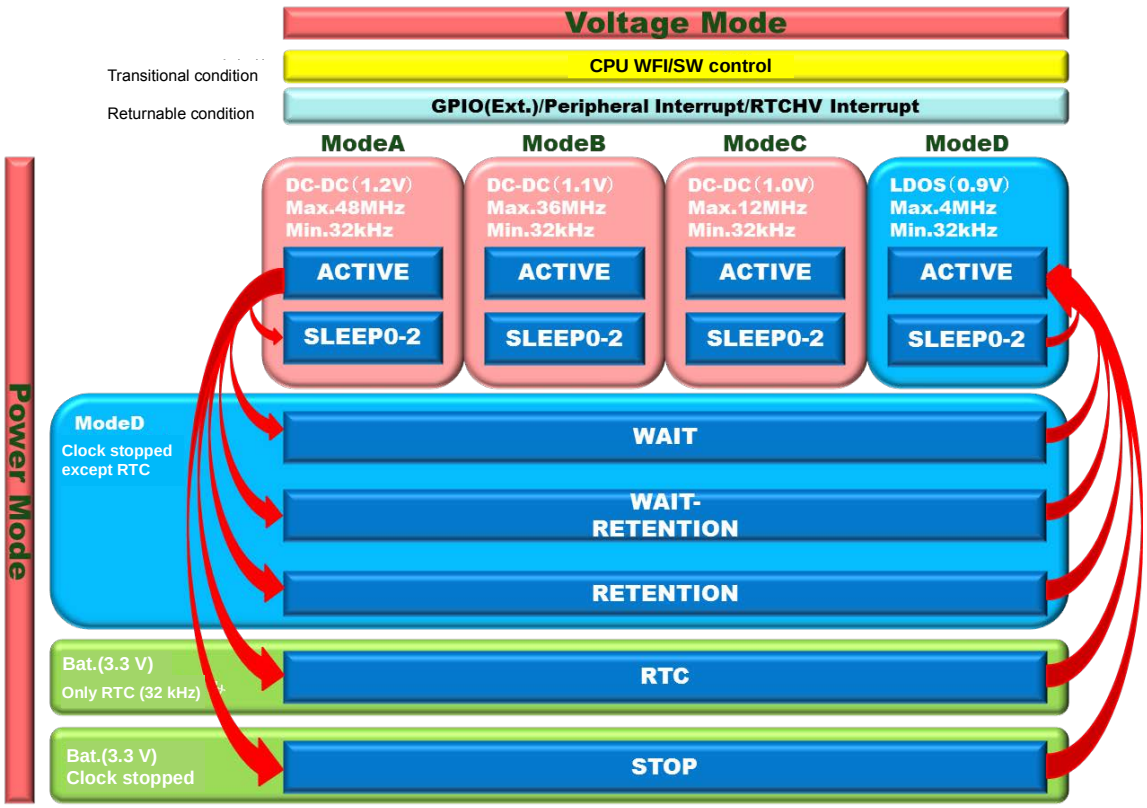

Figure 4.6 Power mode

Table 4.6 Power mode

PowerMode	Description	Voltage Mode	CPU Clock	AHB Clock	APB Clock	RTC Clock	Power Domain
ACTIVE	Active mode. Normal operation.	ModeA-D	ON	ON	ON	ON	Whole ON (*1)
SLEEP0	Low power mode 1. CPU WFI state clock stop. Fast return triggered by an interrupt.	ModeA-D	OFF	ON (*1)	ON (*1)	ON	Whole ON (*1)
SLEEP1	Low power mode 2. CPU WFI state clock stop. AHB clock stop. Fast return triggered by an interrupt	ModeA-D	OFF	OFF	ON (*1)	ON	Whole ON (*1)
SLEEP2	Low power mode 3. CPU WFI state clock stop. AHB/APB clock stop. Fast return triggered by an interrupt.	ModeA-D	OFF	OFF	OFF (*1)	ON	Whole ON (*1)
WAIT	Ultra low power mode 1. CPU WFI state clock stop. All clocks stop except RTC. Slower return than SLEEP0-2.	ModeD	OFF	OFF	OFF	ON	Whole ON (*1) PS0: WAIT PS1: WAIT (*2) PS2: WAIT (*2)
WAIT-RETENTION	Ultra low power mode 2. CPU WFI state clock stop. All clocks stop except RTC. Slower return than SLEEP0-2.	ModeD	OFF	OFF	OFF	ON	PM: ON PS0: WAIT PS1: WAIT (*2) PS2: WAIT (*2) Others: RET
RETENTION	Retention mode. Whole retention. All clocks stop except RTC. Power supply of some power domains can be shut down.	ModeD	OFF	OFF	OFF	ON	Whole RET (*3)
RTC	RTC mode. Only 3.3 V power supply. RTC is operating. CPU reboot is necessary at return.	—	OFF	OFF	OFF	ON	PA: ON Others: OFF
STOP	STOP mode. Only 3.3 V power supply. All clocks stop. CPU reboot is necessary at return.	—	OFF	OFF	OFF	OFF	PA: ON Others: OFF

*1: Some can be OFF.

*2: It can be OFF.

*3: All can be OFF except the PM domain.

Note: RET denotes RETENTION.

4.3.1. Power Mode Transition Diagram

The power mode transition diagram is shown in the following figure. There are 9 power modes and 4 other modes.

- POWEROFF
  - The state before the power is supplied.
- POWERON
  - The power ON state. The power supply sequence is the transition sequence to the STARTUP state. (For detail, refer to 4.4.1. Power Supply Sequence.)
- STARTUP
  - The PMUHV start-up state. The start-up sequence it the transition sequence to the ACTIVE state. (For detail, 4.4.2. Start-up Sequence.)
- BROWNOUT
  - The BROWNOUT state. For detail, refer to 4.5. BrownOut Control.

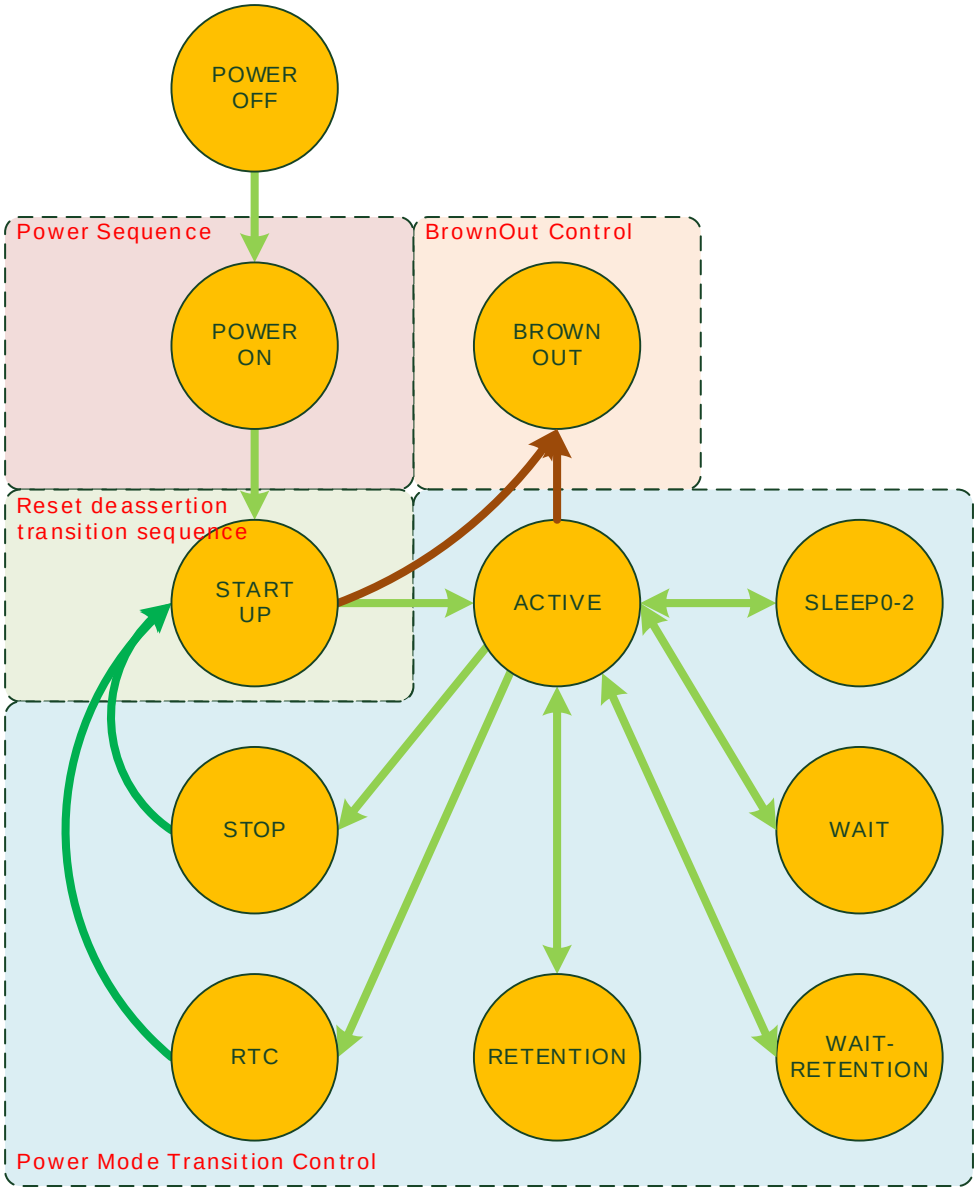

Figure 4.7 Power mode transition diagram

4.3.2. VoltageMode

The VoltageMode transition can be done only at the ACTIVE state in the PowerMode.

4.3.2.1. VoltageMode Transition Specification

- The VoltageMode transition is triggered by the ***[MOVE_VOLTAGE_START]***.START, not by the WFI transition.
- The each mode have the constraints on the available clock source - refer to 4.3.2.4. The available clock source in VoltageMode.
- There is the necessary procedure before and after voltagemode transition according to 4.3.2.5. The necessary procedure to VoltageMode transition.
- The DFS control mult conform to the constraints described in the 4.1.3.1. Maximum operating frequency of each clock domain.
- This specification does not include the Clock/Reset/Power domain control of each block.
- The VoltageMode setting register should be changed only when this mode starts up.
- It is no possible to transit during running the power domain control. Make sure that ***[POWERDOMAIN_CTRL]*** register is 0.

4.3.2.2. Voltage Circuit Switch procedure

(1) Confirm that the VoltageMode is not in operation.
  – Read the ***[MOVE_VOLTAGE_START]***.START and confirm the value is 0.
(2) Set the necessary setting for the VoltageMode.
  – Set the power source per mode and the transition interval to the ***[WAITTIME_DVSCTL]*** register in advance.
  – ***[MOVE_VOLTAGE_MODE]***.POWER_MODE is set to the ACTIVE.
  The mode after the transition is set to ***[MOVE_POWER_VOLTAGE_MODE]***.VOLTAGE_MODE.
(3) Start up the VoltageMode.
  – Write 1 to ***[MOVE_VOLTAGE_START]***.START.

It is possible to check the current status by reading the ***[MOVE_VOLTAGE_START]***.VMSTATUS register. This register is valid when the ***[MOVE_VOLTAGE_START]***.START is 0. If it is 1,it will show the state before the transition.

4.3.2.3. VoltageMode Transition procedure

(1) Confirm that the VoltageMode is not in operation.
  – Read the ***[MOVE_VOLTAGE_START]***.START and confirm the value is 0.
(2) Set the necessary setting for the VoltageMode.
  – Set the power source per mode and the transition interval to the ***[WAITTIME_DVSCTL]*** register in advance.
  – ***[MOVE_VOLTAGE_MODE]***.POWER_MODE is set to the ACTIVE.
  The mode after the transition is set to ***[MOVE_POWER_VOLTAGE_MODE]***.VOLTAGE_MODE.
(3) Start up the VoltageMode.
  – Write 1 to ***[MOVE_VOLTAGE_START]***.START.

4.3.2.4. The available clock source in VoltageMode

There are the constraints on the clock source used in each mode. Refer to the table below.

Table 4.7 The available clock source in VoltageMode

ClockSource/ VoltageMode	ModeA	ModeB	ModeC	ModeD
PLL (48 MHz)	✓	—	—	—
PLL9 (36 MHz)	—	✓	—	—
PLL3 (24 MHz)	—	✓	—	—
ADPLL	✓	—	—	—
OSC12M/OSC12M3	✓	✓	✓	—
SIOSC4M	✓	✓	✓	✓
OSC32K	✓	✓	✓	✓
SIOSC32K	✓	✓	✓	✓

Note: ✓ shows Selectable.

Note: — shows Un-selectable.

4.3.2.5. The necessary procedure to VoltageMode transition

Refer to the table below about the necessary procedures to VoltageMode Transition. However, if they are the state of start or stop and are not used, they are not necessarily executed.

from/to	Procedure Timing	ModeA	ModeB	ModeC	ModeD
ModeA	Pre-procedure	—	DFS Control The stop of ADPLL The stop of PLL The trimming value change of SIOSC4M	DFS Control The stop of ADPLL The stop of PLL The trimming value change of SIOSC4M	DFS Control The stop of ADPLL The stop of PLL The stop of OSC12M The trimming value change of SIOSC4M
	Post-procedure	—	The change of the multiplied ratio of PLL The start of PLL DFS Control	—	—
ModeB	Pre-procedure	DFS Control The stop of PLL The trimming value change of SIOSC4M	—	DFS Control The stop of PLL The trimming value change of SIOSC4M	DFS Control The stop of PLL The stop of OSC12M The trimming value change of SIOSC4M
	Post-procedure	The start of ADPLL The change of the multiplied ratio of PLL The start of PLL DFS Control	—	—	—
ModeC	Pre-procedure	The trimming value change of SIOSC4M	The trimming value change of SIOSC4M	—	DFS Control The stop of OSC12M The trimming value change of SIOSC4M
	Post-procedure	The start of ADPLL The start of PLL DFS Control	The start of PLL DFS Control	—	—
ModeD	Pre-procedure	The trimming value change of SIOSC4M	The trimming value change of SIOSC4M	The trimming value change of SIOSC4M	—
	Post-procedure	The start of ADPLL The start of PLL The start of OSC12M DFS Control	The start of PLL The start of OSC12M DFS Control	The start of OSC12M DFS Control	—

Note: The vertical axis is the state of the voltagemode before the transition.
Note: The horizontal axis is the state of the voltagemode after the transition.
Note: refer to 4.1.4.6. ADPLL about the start and stop of ADPLL.
Note: refer to 4.1.4.5. PLL about the start and stop of PLL.
Note: refer to 4.1.4.1. OSC12M about the start and stop of OSC12M.
Note: refer to 4.1.4.3. SIOSC4M about the trimming value change of SIOSC4M.
Note: — indicates that no procedure is to be performed.

4.3.3. PowerMode

It is transited from the ACTIVE state to the other power state triggered by the CPU WFI state. It returns to the Active state with the WAKEUP interrupt.

The PowerMode consists of the subsequences such as the VoltageMode control, the power control, the reset control, clock control, and IO control. It is controlled by the PMU hardware sequencer.

The PowerMode specification is described for each power mode. Refer to each specification.

4.3.3.1. ACTIVE-WFI Mode

In the ACTIVE-WFI mode, only CPU core clock gating is executed.

(Outlines)

- In this mode, the reset and power states remain the states before transiting the WFI state.
- The clock state returns the state before transiting the WFI state.

4.3.3.1.1. ACTIVE-WFI Transition and Return

4.3.3.1.1.1. ACTIVE-WFI Transition Control

(1) The followings are set;
[MOVE_POWER_VOLTAGE_MODE]. POWER_MODE = 0b0000

(2) Wait 3cycle at the CPU Clock and 250 ns. The ACTIVE-WFI are controlled by the CPU clock. This is because it takes times to reflect the change of ***[MOVE_POWER_VOLTAGE_MODE]***.POWER_MODE from the PMU clock to the CPU Clock.

(3) The CPU transits to the WFI state

(4) The PMULV hardware sequencer starts and the target blocks transit to their specified modes.

4.3.3.1.1.2. ACTIVE-WFI Return Control

(1) The CPU receives the interrupt from each block.

(2) The CPU changes its mode from the WFI mode by the interrupt because the CPU is supplied with the FCLK in the ACTIVE-WFI mode.

(3) The PMULV is surveying the CPU is out of the WFI state. The PMULV hardware sequencer starts and releases the clock stop of the target block.

(4) Return from the ACTIVE-WFI mode to the ACTIVE state.

4.3.3.2. SLEEP0/1/2 Mode

In the SLEEP0/1/2 mode, only clock gating is executed. The transition and return time is short because of no power domain controls.

(Outlines)

- In this mode, the reset and power states remain the states before transiting the WFI state.
- The clock state returns the state before transiting the WFI state.
- In the SLEEP0/1/2 mode, the target block clocks are forced to be gated. The other clocks remain the state before transiting to the WFI state.
- The USB2FS is not the target. It remains the same as the state before the WFI state.
- When the CPU is set to the SLEEPING, the CPU returns by all interrupts which the CPU receives.
- When the CPU is set to the SLEEPDEEP, the CPU returns by only the wake up interrupt (GPIO/RTC/CPU Hot Plug/BrownOut).

- According to the state of [CG_ON_AA_BB] register, it stop automatically the internal circuit of PMU.
- By using the ***[POWERMODE_SLEEP_PRESCAL]*** register, the CPU FCLK is divided in the SLEEP0/1/2 mode (SLEEPING) state, and can reduce the power consumption. However the transition time will be longer.
- By using the ***[POWERMODE_SLEEP_CG_ON]*** register, a clock gating target block can be added in the SLEEP0/1/2 mode.
  For example, the SLEEP0 mode is the mode where only the CPU is the target. The clock gating of the SRAMC, however, can also be done by the register.

Table 4.8 Clock gating target block

PowerMode	Clock Gating Target Block
SLEEP0	CPU
SLEEP1	CPU/MPIER/SDMAC/AESA/RNG/SRAMC/SPIC
SLEEP2	CPU/MPIER/SDMAC/AESA/RNG/SRAMC/SPIC UART0/UART1/UART2/I2C0/I2C1/I2C2/SPIM0/SPIM1 SPIM2/SPIM3/TMR/ADVTMR/WDT/EVM

4.3.3.2.1. SLEEP0/1/2 Transition and Return

4.3.3.2.1.1. SLEEP0/1/2 Transition Control

(1) The followings are set;
SLEEP0**: *[MOVE_POWER_VOLTAGE_MODE]***. POWER_MODE = 0b0001
SLEEP1**: *[MOVE_POWER_VOLTAGE_MODE]***.POWER_MODE = 0b0010
SLEEP2**: *[MOVE_POWER_VOLTAGE_MODE]***.POWER_MODE = 0b0011

(2) Wait 3cycle at the CPU Clock and 250 ns. The SLEEP0/1/2 Mode are controlled by the CPU clock. This is because it takes times to reflect the change of ***[MOVE_POWER_VOLTAGE_MODE]***.POWER_MODE from the PMU clock to the CPU Clock.

(3) Check in advance that each block is in the idle state.

- Refer to the Chapter 4.6.1 and 4.6.2 of the latest TZ1000 Series Reference Manual MCU SPI Flash Controller.
- Refer to the Chapter 4.1.1 and 4.1.2 of the latest TZ1000 Series Reference Manual MCU SRAM Controller.
- Refer to the Chapter 4.2 of the latest TZ1000 Series Reference Manual MCU 12-bit Analog to Digital Converter.
- Refer to the Chapter 4.2 of the latest TZ1000 Series Reference Manual MCU 24-bit Analog to Digital Converter.
- Refer to the Chapter 5.3 of the latest TZ1000 Series Reference Manual MCU USB Device controller.
- Refer to the Chapter 4.3 of the latest TZ1000 Series Reference Manual MCU Global Configuration Block.
- Refer to the Chapter 4.3 and 4.4 of the latest TZ1000 Series Reference Manual MCU AES Accelerator.
- Refer to the Chapter 4.2 and 4.3 of the latest TZ1000 Series Reference Manual MCU Random Number Generator.
- Refer to the Chapter 5.2 of the latest TZ1000 Series Reference Manual MCU General-Purpose Input/Output Controller.
- Refer to the Chapter 6.13 of the latest TZ1000 Series Reference Manual MCU I^2C Master/Slave Interface.
- Refer to the Chapter 5.6 of the latest TZ1000 Series Reference Manual MCU Universal asynchronous receiver/transmitter.
- Refer to the Chapter 5.7 of the latest TZ1000 Series Reference Manual MCU Serial Peripheral Interface.
- Refer to the Chapter 5.4 and 5.5 of the latest TZ1000 Series Reference Manual MCU Timer/Counter.
- Refer to the Chapter 5.10 and 5.11 of the latest TZ1000 Series Reference Manual MCU Advanced Timer/Counter.
- Refer to the Chapter 5.3 and 5.4 of the latest TZ1000 Series Reference Manual MCU Watchdog Timer.
- Refer to the Chapter 5.6 of the latest TZ1000 Series Reference Manual MCU System DMA Controller.
- Refer to the Chapter 5.2 of the latest TZ1000 Series Reference Manual MCU Real Time Clock Counter.
- Refer to the Chapter 4.3 of the latest TZ1000 Series Reference Manual MCU Event Control Block.
- Refer to the Chapter 4.4 of the latest TZ1000 Series Reference Manual MCU IO.

(4) Read the bus.***[BUS_BUSY]*** register and make sure that the value is 0 except for the SLEEP0 mode.

(5) The CPU transits to the WFI state

(6) The PMULV hardware sequencer starts and the target blocks transit to their specified modes.

* There is no the order constraints in (3).

4.3.3.2.1.2. SLEEP0/1/2 Return Control (when the CPU SLEEPING is set)

(1) The CPU receives the interrupt from each block.
(2) The CPU changes its mode from the WFI mode by the interrupt because the CPU is supplied with the FCLK in the SLEEP0/1/2 mode.
(3) The PMULV is surveying the CPU is out of the WFI state. The PMULV hardware sequencer starts and releases the clock stop of the target block.
(4) Return from the SLEEP0/1/2 mode to the ACTIVE state.

4.3.3.2.1.3. SLEEP0/1/2 Return Control (When the CPU SLEEPDEEP is set)

(1) The PMUHV receives the interrupt from the GPIO or the RTC. This interrupt is also transferred to the PMULV and the CPU.
(2) The PMULV releases the clock stop of the target block. The CPU is supplied with the FCLK.
(3) The CPU changes its mode from the WFI state.
(4) The PMULV is surveying the CPU is out of the WFI state. The block returns from the SLEEP0/1/2 mode to the ACTIVE state.

4.3.3.3. WAIT/WAIT-RETENTION Mode

In the WAIT/WAIT-RETENTION mode, the power domains are in the WAIT mode or the RETENTION mode. It reduces the power consumption. The retention is not applied to the whole domain, which is different from the RETENTION mode. So the return from this mode is faster. The difference between the WAIT mode and the WAIT-RETENTION mode is that the power domains other than the PS0/1/2 are applied with the retention, or not.

(Outlines)

- The clock gating, reset, and power states are returned to the states before the transition to the WFI.
  - The clock gating state returns to the state which is set in ***[CG_ON(OFF)_[Power domain]_[Number]***.
  - The reset state returns to the state which is set in ***[SRST_ON(OFF)_[Power domain]_[Number]***.
  - The power domain state returns to the state which is set in ***[POWERDOMAIN_CTRL_MODE]***.
- If the power of the domain is OFF, the transition is done with the power OFF even though the *[POWERDOM AIN_CTRL_MODE_FOR_WAIT]* register and the *[POWERDOMAIN_CTRL_MODE_FOR_WRET]* register are set to the WAIT and the RET, respectively.
- The sensor power transits in the state before changing to the WFI state.
- In the case of WAIT-RETENTION mode, the IO retention control is performed on PP1 block area by the hardware sequencer (transition: from ON to RET/OFF return: from RET/OFF to ON).
- Hardware sequencer operates as follows.
  - Stop all clocks except the clocks in the CD_RTC domain.
  - All clocks except the clocks in the CD_RTC domain are changed to 4 MHz clock (divided by one) whose source is the SIOSC4M.
  - The power of the PADPLL/PPLL is shut down.
  - Stop the OSC12M clock.
  - VoltageMode: Transit to the ModeD.

  All settings except the VoltageMode should be re-setting by software when returning from this mode.
- *[MOVE_POWER_VOLTAGE_MODE]*.FAST_MODE can select the VoltageMode state after the return.
  - If the setting value is 0, the normal return mode is selected and the destination is the VoltageMode before changing to the WFI state

  If the setting value is 1, the high speed return mode is selected and VoltageMode remains ModeD.

Return to ACTIVE by the RTC interrupt, the GPIO interrupt, the CPU Hot Plug interrupt, or the BrownOut interrupt.

4.3.3.3.1. WAIT/WAIT-RETENTION Transition and Return

4.3.3.3.1.1. WAIT/WAIT-RETENTION Transition Control

(1) The followings are set.
WAIT**:** ***[MOVE_POWER_VOLTAGE_MODE]***. POWER_MODE = 0b0100
[POWERDOMAIN_CTRL_MODE_FOR_WAIT]
WAIT-RETENTION**:** ***[MOVE_POWER_VOLTAGE_MODE]***. POWER_MODE = 0b0101
[POWERDOMAIN_CTRL_MODE_FOR_WRET]
[MOVE_POWER_VOLTAGE_MODE].FAST_MODE is set to select the Voltage Mode after returning from this mode.

(2) The power domain control in the WAIT mode is done only to PS0, PS1, and PS2. The control is done by the setting in the ***[POWERDOMAIN_CTRL_MODE_FOR_WAIT]*** register. The setting of the register is necessary. And, in the WAIT-RETENTION mode, the power domains except the PM and the PU are controlled by the ***[POWERDOMAIN_CTRL_MODE_FOR_WRET]*** register. The setting of the register is necessary.

(3) CPU SCR.SLEEPDEEP register should be set to 1.

(4) Check that the power domain control and VoltageMode are not running.
- Check that ***[POWERDOMAIN_CTRL]*** is all 0.
- Check that ***[MOVE_VOLTAGE_START]***.START is 0.

(5) Each power domain is returned according to the value of ***[POWERDOMAIN_CTRL_MODE]*** register. When PowerMode is transited, must be set the same as the value of the ***[POWER DOMAIN_CTRL_STATUS]***.

(6) Check in advance that each block is in the idle state.
- Refer to the Chapter 4.6.2, 4.6.3 and 6.2.3 of the latest TZ1000 Series Reference Manual MCU SPI Flash Controller.
- Refer to the Chapter 4.1.3 and 4.1.4 of the latest TZ1000 Series Reference Manual MCU SRAM Controller.
- Refer to the Chapter 4.2 of the latest TZ1000 Series Reference Manual MCU 12-bit Analog to Digital Converter.
- Refer to the Chapter 4.2 of the latest TZ1000 Series Reference Manual MCU 24-bit Analog to Digital Converter.
- Refer to the Chapter 5.3 of the latest TZ1000 Series Reference Manual MCU USB Device controller.
- Refer to the Chapter 4.3 of the latest TZ1000 Series Reference Manual MCU Global Configuration Block.
- Refer to the Chapter 4.3 and 4.4 of the latest TZ1000 Series Reference Manual MCU AES Accelerator.
- Refer to the Chapter 4.2 and 4.3 of the latest TZ1000 Series Reference Manual MCU Random Number Generator.
- Refer to the Chapter 5.2 of the latest TZ1000 Series Reference Manual MCU General-Purpose Input/Output Controller.
- Refer to the Chapter 5.13 of the latest TZ1000 Series Reference Manual MCU I^2C Master/Slave Interface.
- Refer to the Chapter 5.6 of the latest TZ1000 Series Reference Manual MCU Universal asynchronous receiver/transmitter.
- Refer to the Chapter 5.7 of the latest TZ1000 Series Reference Manual MCU Serial Peripheral Interface.
- Refer to the Chapter 5.4 and 5.5 of the latest TZ1000 Series Reference Manual MCU Timer/Counter.
- Refer to the Chapter 5.10 and 5.11 of the latest TZ1000 Series Reference Manual MCU Advanced Timer/Counter.
- Refer to the Chapter 5.3 and 5.4 of the latest TZ1000 Series Reference Manual MCU Watchdog Timer.
- Refer to the Chapter 5.6 of the latest TZ1000 Series Reference Manual MCU System DMA Controller.
- Refer to the Chapter 5.2 of the latest TZ1000 Series Reference Manual MCU Real Time Clock Counter.
- Refer to the Chapter 4.3 of the latest TZ1000 Series Reference Manual MCU Event Control Block.
- Refer to the Chapter 4.4 and 4.5 of the latest TZ1000 Series Reference Manual MCU IO.

(7) Read the bus.***[BUS_BUSY]*** register and make sure that the value is 0. Refer to the Chapter 5.1 of the latest TZ1000 Series Reference Manual MCU Bus Interconnect.

(8) The CPU transits to the WFI state.

* There is no the order constraints from (1) to (3).

* There is no the order constraints in (6).

* When MCU_BOOTMODE3 is 0 and the state of the PF domain is ON, CPU must ensure that it fetch the instruction and data from SRAM before the transition of PowerMode (only WAIT-RETENT ION). The correct data might not be read from SPI, if is accessed to it immediately after the return of PowerMode.

4.3.3.3.1.2. WAIT/WAIT-RETENTION Return Control

(1) An interrupt is generated in one of the RTC, GPIO, CPU HotPlug, and BrownOut modes.
(2) The PMU starts the return operation when it receives the interrupt request.
(3) The CPU receives the interrupt and returns to the ACTIVE state.
(4) Wait for time depending on the capacitance of the capacitor put to MCU_VDD18_SPIF_OUT (only when MCU_BOOTMODE3 is 0 and the state of the PF domain is ON).
   – When put the 5 μF (current recommended value) including the 1 μF inside PKG, wait for time obtained by substracting the time set to the ***[WAITTIME_LDOF]***.WAITTIME_LDOF_PWON register from 1.5 ms.
(5) When the WAIT-RETENTION mode is returned to the ACTIVE mode, the clock gating control, reset control, DFS control, power domain control, and VoltageMode control should be done after confirming the ***[STATUS_LVPWR]*** register is All 0 (that is, in ACTIVE mode). The clock source control (the power control and start-up control), however, can be done without the confirmation of the register value.

After returning, all clock domains except the CD_RTC operate with 4 MHz clock (divided by one) whose source is the SIOSC4M. If the clock source is changed to the PLL, the sequence of the power ON of the PPLL domain (4.2.3.7 PPLL Domain control), OSC12M start-up (4.1.4.1 OSC12M), and then, PLL start-up should be done in the order.

When ***[MOVE_POWER_VOLTAGE_MODE]***.FAST_MODE = high speed return mode is set, the return is done in the mode of VoltageMode = ModeD. If VoltageMode is changed to the original mode before the WFI state, the transition should follow the VoltageMode transition specification.

4.3.3.4. RETENTION Mode

All power domains except the PA can be in the RETENTION mode.

(Outlines)

- The clock gating, reset, and power states are returned to the states before the transition to the WFI.
  - The clock gating state returns to the state which is set in ***[CG_ON(OFF)_[Power domain]_[Number]***.
  - The reset state returns to the state which is set in ***[SRST_ON(OFF)_[Power domain]_[Number]***.
  - The power domain state returns to the state which is set in ***[POWERDOMAIN_CTRL_MODE]***.

  The powers of the power domains except the PM can be shut down. The mode after the transition is selected by the ***[POWERDOMAIN_CTRL_M ODE_FOR_RET]*** register.
- If the power of the domain is OFF, the transition is done with the power OFF even though the ***[POWERDOMAIN_CTRL_MODE_FOR_RET]*** register is set to the RET.
- The sensor power transits in the state before changing to the WFI state.
- In the case of RETENTION mode, the IO retention control is performed on the PP1 and PM block area by hardware sequencer (transition: from ON to RET/OFF return: from RET/OFF to ON)
- Hardware sequencer operates as follows.
  - Stop all clocks except the clocks in the CD_RTC domain.
  - All clocks except the clocks in the CD_RTC domain are changed to 4 MHz clock (divided by one) whose source is the SIOSC4M.
  - The power of the PADPLL/PPLL is shut down.
  - Stop the OSC12M clock.
  - VoltageMode: Transit to the ModeD.

  All settings except the VoltageMode should be re-setting by software when returning from this mode.
- ***[MOVE_POWER_VOLTAGE_MODE]***.FAST_MODE can select the VoltageMode state after the return.
  - If the setting value is 0, the normal return mode is selected and the destination is the VoltageMode before changing to the WFI state
  - If the setting value is 1, the high speed return mode is selected and VoltageMode remains ModeD.
- Return to ACTIVE by the RTC interrupt, the GPIO WAKEUP interrupt, the CPU Hot Plug interrupt, or the BrownOut interrupt.

4.3.3.4.1. RETENTION Transition and Return

4.3.3.4.1.1. RETENTION Transition Control

(1) RETENTION**:** ***[Move_Power_Voltage_Mode]***. MODE_power_mode = 0b0111
[POWERDOMAIN_CTRL_MODE_FOR_RET] is set.
[MOVE_POWER_VOLTAGE_MODE].FAST_MODE is set to select the Voltage Mode after returning from this mode.

(2) Regardless of the setting value of the prescaler, when the clock domain other than CD_RTC has selected the 32.768 kHz clock source, it is necessary to change to another clock source - refer to 4.1.5. DFS Control). And then, stop the 32.768 kHz clock other than RTC block.

- The ***[CG_ON_PA]***.CG_32KOSC_pmulv register should be set to 1.

(3) In the RETENTION mode, the power domain is controlled by the ***[POWERDOMAIN_CTRL_MODE_FOR_RET]*** register. The setting of the register is necessary.

(4) The power of the PU domain should be shut down - refer to 4.2.3.4. PU Domain Control.

(5) CPU SCR.SLEEPDEEP register should be set to 1.

(6) Check that the power domain control and VoltageMode are not running.

- Check that ***[POWERDOMAIN_CTRL]*** is all 0.
- Check that ***[MOVE_VOLTAGE_START]***.START is 0.

(7) Each power domain is returned according to the value of ***[POWERDOMAIN_CTRL_MODE]*** register. When PowerMode is transited, must be set the same as the value of the ***[POWER DOMAIN_CTRL_STATUS]***.

(8) Check in advance that each block is in the idle state.

- Refer to the Chapter 4.6.3 and 6.2.3 of the latest TZ1000 Series Reference Manual MCU SPI Flash Controller.
- Refer to the Chapter 4.1.5 of the latest TZ1000 Series Reference Manual MCU SRAM Controller.
- Refer to the Chapter 4.2 of the latest TZ1000 Series Reference Manual MCU 12-bit Analog to Digital Converter.
- Refer to the Chapter 4.2 of the latest TZ1000 Series Reference Manual MCU 24-bit Analog to Digital Converter.
- Refer to the Chapter 5.3 of the latest TZ1000 Series Reference Manual MCU USB Device controller.
- Refer to the Chapter 4.3 of the latest TZ1000 Series Reference Manual MCU Global Configuration Block.
- Refer to the Chapter 4.3 and 4.4 of the latest TZ1000 Series Reference Manual MCU AES Accelerator.
- Refer to the Chapter 4.2 and 4.3 of the latest TZ1000 Series Reference Manual MCU Random Number Generator.
- Refer to the Chapter 5.2 of the latest TZ1000 Series Reference Manual MCU General-Purpose Input/Output Controller.
- Refer to the Chapter 5.13 of the latest TZ1000 Series Reference Manual MCU I^2C Master/Slave Interface.
- Refer to the Chapter 5.6 of the latest TZ1000 Series Reference Manual MCU Universal asynchronous receiver/transmitter.
- Refer to the Chapter 5.7 of the latest TZ1000 Series Reference Manual MCU Serial Peripheral Interface.
- Refer to the Chapter 5.4 and 5.5 of the latest TZ1000 Series Reference Manual MCU Timer/Counter.
- Refer to the Chapter 5.10 and 5.11 of the latest TZ1000 Series Reference Manual MCU Advanced Timer/Counter.
- Refer to the Chapter 5.3 and 5.4 of the latest TZ1000 Series Reference Manual MCU Watchdog Timer.
- Refer to the Chapter 5.6 of the latest TZ1000 Series Reference Manual MCU System DMA Controller.
- Refer to the Chapter 5.2 of the latest TZ1000 Series Reference Manual MCU Real Time Clock Counter.
- Refer to the Chapter 4.3 of the latest TZ1000 Series Reference Manual MCU Event Control Block.
- Refer to the Chapter 4.3 of the latest TZ1000 Series Reference Manual MCU IO.

(9) Read the bus. ***[BUS_BUSY]*** register and make sure that the value is 0. Refer to the Chapter 5.1 of the latest TZ1000 Series Reference Manual MCU Bus Interconnect.

(10) The CPU transits to the WFI state.

* There is no the order constraints from (1) to (5).

* There is no the order constraints in (8).

* When MCU_BOOTMODE3 is 0 and the state of the PF domain is ON, CPU must ensure that it fetch the instruction and data from SRAM before the transition of PowerMode (only WAIT-RETENT ION). The correct data might not be read from SPI, if is accessed to it immediately after the return of PowerMode.

4.3.3.4.1.2. RETENTION Return Control

(1) An interrupt is generated in one of the RTC, GPIO, CPU HotPlug, and BrownOut modes.
(2) The PMU starts the return operation when it receives the interrupt request.
(3) The CPU receives the interrupt and returns to the ACTIVE state.
(4) Wait for time depending on the capacitance of the capacitor put to MCU_VDD18_SPIF_OUT - only when MCU_BOOTMODE3 is 0 and the state of the PF domain is ON.
   – When put the 5 μF (current recommended value) including the 1 μF inside PKG, wait for time obtained by substracting the time set to the ***[WAITTIME_LDOF]***.WAITTIME_LDOF_PWON register from 1.5 ms.
(5) When the RETENTION mode is returned to the ACTIVE mode, the clock gating control, reset control, DFS control, power domain control, and VoltageMode control should be done after confirming the ***[STATUS_LVPWR]*** register is All 0 (that is, in ACTIVE mode). The clock source control (the power control and start-up control), however, can be done without the confirmation of the register value.

After returning, all clock domains except the CD_RTC operate with 4 MHz clock(divided by one) whose source is the SIOSC4M. If the clock source is changed to the PLL, After the start of PLL - refer to 4.1.4.5. PLL, change the clock source.

After returning, it takes some time until it can write access to the RTC block. There is no constraints to read access. If the CPU has write access to before it is ready, the reflected time of write access to the rtc.***[RTC_CTRL]*** register is delayed. The delay time is determined by the ***[RTCLV_RSYNC_SETTING]*** register.

Accessible time is determined by the setting of ***[RTCLV_RSYNC_SETTING]*** register except for 0b00 in the only case of return from RETENTION mode.

- The setting value is 0b00: about 5 μs
- The setting value is 0b01: about 70 μs
- The setting value is 0b10: about 100 μs

When ***[MOVE_POWER_VOLTAGE_MODE]***.FAST_MODE = high speed return mode is set, the return is done in the mode of VoltageMode = ModeD. If VoltageMode is changed to the original mode before the WFI state, the transition should follow the VoltageMode Transition procedure.

4.3.3.5. RTC/STOP Mode

In the RTC/STOP mode, all powers except the PA power are shut down. The clock for the RTC block is disabled in the STOP mode, and the clock is enabled in the RTC mode. When returning from the RTC/STOP mode, the start-up sequence is executed.

(Outlines)

- The state after returning from the RTC/STOP mode is almost the same state after the start-up sequence.
  - Power supply voltage: 1.2 V
  - Power: DC-DC power supply
  - Frequency: 48 MHz (By the EFUSE setting it may be OSC12M - 12 MHz or SIOSC4M- 4 MHz)
  - The CPU, PMULV, SPIC, SRAMC, and Main Bus are in the state of the clock gating and reset deassertion.
- The sensor power transits in the state before changing to the WFI state.
- Return to ACTIVE by the RTC interrupt, the GPIO WAKEUP interrupt, the CPU Hot Plug interrupt, or the BrownOut interrupt.
- In the case of RTC/STOP mode, the IO retention control is performed by hardware sequencer (transition: from all state to OFF return: not performed)
  - Because the powers of all domains except PA are shut down, the IO setting such as the drivability and the pull-up or pull-down resistor are initialized.

It should be set again after returning from the RTC and STOP mode, because PA in the register is partially initialized. Please refer to the following table for the registers initialized or not initialized by RTC/STOP mode

Table 4.9 The initialized or not initialized register by RTC and STOP mode

	Initialized register	Not Initialized register
All block except for PMUHV	All register	—
PMUHV	***[CONFIG_SIOSC4M]*** ***[CONFIG_DCDC_HVREG]*** ***[CONFIG_LVD_0]*** ***[CONFIG_LDOM_number]*** ***[CONFIG_LDOS_number]*** ***[OVERRIDE_EFUSE_SIOSC4M]*** ***[OVERRIDE_EFUSE_BGR_0]*** ***[CG_ON/OFF_PA]***.CG_32KOSC_pmulv	***[CONFIG_OSC32K]*** ***[CONFIG_SIOSC32K]*** ***[OVERRIDE_EFUSE_OSC32K]*** ***[OVERRIDE_EFUSE_SIOSC32K]*** ***[OVERRIDE_EFUSE_BGR_1]*** ***[CTRL_IO_AON_number]*** ***[IRQ_SETTING_number]*** ***[WAKEUP_EN]*** ***[IRQ_STATUS]*** ***[STATUS_LVPWR]*** ***[STATUS_LVRST]*** ***[CG_ON/OFF_PA]***.CG_CLK32K_OUT ***[CG_ON/OFF_PA]***.CG_rtcclk_rtchv_rtcclk ***[SRST_ON/OFF_PA]*** ***[CSM_RTC]*** ***[CPU_DBGEN]*** ***[BROWNOUTMODE]*** ***[RTCLV_RSYNC_SETTING]***

4.3.3.5.1. RTC/STOP Transition and Return

4.3.3.5.1.1. RTC/STOP Transition Control

(1) The followings are set;
- RTC**:** ***[MOVE_POWER_VOLTAGE_MODE]***.MODE_power_mode = 0b1000
- STOP**:** ***[MOVE_POWER_VOLTAGE_MODE]***.MODE_power_mode = 0b1001

(2) When transiting to the STOP mode, the clock source of the CD_RTC and its output to the external should be stopped.
- ***[CG_ON_PA]***.CG_CLK32K_OUT should be written to 1.
- ***[CG_ON_PA]***.CG_32KOSC_pmulv should be written to 1.
- ***[CG_ON_PA]***. CG_rtcclk_rtchv_rtcclk should be written to 1.
- The selected clock source should be stopped - refer to 4.1.4.2. OSC32K or 4.1.4.4. SIOSC32K.

(3) The power of the PU domain should be shut down by software - refer to 4.2.3.4. PU Domain Control.

(4) CPU SCR.SLEEPDEEP register should be set to 1.

(5) Check that the power domain control and VoltageMode are not running.
- Check that ***[POWERDOMAIN_CTRL]*** is all 0.
- Check that ***[MOVE_VOLTAGE_START]***.START is 0.

(6) Check in advance that each block is in the idle state.
- Refer to the Chapter 4.6.4 of the latest TZ1000 Series Reference Manual MCU SPI Flash Controller.
- Refer to the Chapter 4.1.6 of the latest TZ1000 Series Reference Manual MCU SRAM Controller.
- Refer to the Chapter 4.2 of the latest TZ1000 Series Reference Manual MCU 12-bit Analog to Digital Converter.
- Refer to the Chapter 4.2 of the latest TZ1000 Series Reference Manual MCU 24-bit Analog to Digital Converter.
- Refer to the Chapter 5.3 of the latest TZ1000 Series Reference Manual MCU USB Device controller.
- Refer to the Chapter 4.3 of the latest TZ1000 Series Reference Manual MCU Global Configuration Block.
- Refer to the Chapter 4.3 and 4.4 of the latest TZ1000 Series Reference Manual MCU AES Accelerator.
- Refer to the Chapter 4.2 and 4.3 of the latest TZ1000 Series Reference Manual MCU Random Number Generator.
- Refer to the Chapter 5.2 of the latest TZ1000 Series Reference Manual MCU General-Purpose Input/Output Controller.
- Refer to the Chapter 5.13 of the latest TZ1000 Series Reference Manual MCU I^2C Master/Slave Interface.
- Refer to the Chapter 5.6 of the latest TZ1000 Series Reference Manual MCU Universal asynchronous receiver/transmitter.
- Refer to the Chapter 5.7 of the latest TZ1000 Series Reference Manual MCU Serial Peripheral Interface.
- Refer to the Chapter 5.4 and 5.5 of the latest TZ1000 Series Reference Manual MCU Timer/Counter.
- Refer to the Chapter 5.10 and 5.11 of the latest TZ1000 Series Reference Manual MCU Advanced Timer/Counter.
- Refer to the Chapter 5.3 and 5.4 of the latest TZ1000 Series Reference Manual MCU Watchdog Timer.
- Refer to the Chapter 5.6 of the latest TZ1000 Series Reference Manual MCU System DMA Controller.
- Refer to the Chapter 4.8 and 5.2 of the latest TZ1000 Series Reference Manual MCU Real Time Clock Counter.
- Refer to the Chapter 4.3 of the latest TZ1000 Series Reference Manual MCU Event Control Block.
- Refer to the Chapter 4.2 of the latest TZ1000 Series Reference Manual MCU IO.

(7) Read the bus. ***[BUS_BUSY]*** register and make sure that the value is 0. Refer to the Chapter 5.1 of the latest TZ1000 Series Reference Manual MCU Bus Interconnect.

(8) The CPU transits to the WFI state.

* There is no the order constraints from (1) to (4).

* There is no the order constraints in (6).

4.3.3.5.1.2. RTC/STOP return control

(1) An interrupt request is generated in one of the RTC (except the STOP mode), GPIO, CPU HotPlug, and BrownOut modes.

(2) The PMU starts the return operation when it receives the interrupt request.

(3) The CPU reset is deasserted and the rerun is done.

(4) The IO retention state should be released after the settings of the drivability and the pull-up or pull-down resistor are done. For the setting, refer to the latest Reference Manual TZ1000 Series Reference Manual MCU Global Configuration Block.

4.3.3.6. Relationship of PowerMode, VoltageMode, Power Domain Control, Clock Source and Clock Domain

This shows the detailed relationship of PowerMode, VoltageMode, Power Domain Control, Clock Source and Clock Domain.

(The view of table)

- Returnable Condition
  - described the returnable wakeup interrupt
  - ✓ shows that it is returnable.
  - — show that it is not returnable.
- Clock Source
  - described the available clock source - refer to 4.3.2.4. The available clock source in VoltageMode
  - ✓ shows that it is available.
  - — show that it is not available.
  - → OFF show that it stop by hardware sequencer.
  - Other → OFF show that it change the another clock source and then stop by hardware sequencer.
- Power Domain
  - described the state of power domain that can be in the PowerMode, and is managed by software. For example, ON/OFF means that it can be either state. It is recommended to the state of OFF for power reduction, if is not used.
  - If → is attached, it show that it is translated by hardware sequencer.
  - If → is not attached, it show that the state change before and after the transition of PowerMode.
  - If some states has been described, it means that it is selectable by register.
- Clock Domain
  - described the state of clock domain that can be in the PowerMode, and is managed by software. For example, ON/OFF means that it can be either state. It is recommended to the state of OFF for power reduction, if is not used.
  - If → is attached, it show that it is translated by hardware sequencer.
  - If → is not attached, it show that the state change before and after the transition of PowerMode.
  - cpu fclk show that it is free run clock of CPU.
  - cpu hclk show that it is core clock of CPU.
  - other fclk show that it is clock other than CPU.

4.3.3.7. PowerMode transition when a Debugger is connected

When a debugger is connected, the PowerMode set by *[MOVE_POWER_VOLTAGE_MODE]*. POWER_MODE is not transited. In this case, ACTIVE status is kept and CPU becomes WFI mode. And the clock is supplied to CPU different from ACTIVE WFI mode.

Table 4.10 ACTIVE/SLEEP0 Mode

			ACTIVE				SLEEP0			
			ModeA	ModeB	ModeC	ModeD	ModeA	ModeB	ModeC	ModeD
Returnable Condition	Interrupt from each Peripheral		—				✓			
	Wakeup Interrupt by RTC		—				✓			
	Wakeup Interrupt by GPIO		—				✓			
	Wakeup Interrupt by BrownOut		—				✓			
	Wakeup Interrupt by CPU Debug		—				✓			
Clock Source	OSC12M/OSC12M3		✓	✓	✓	—	✓	✓	✓	—
	PLL		✓	✓	—	—	✓	✓	—	—
	PLL9 (at 36 MHz)		—	✓	—	—	—	✓	—	—
	PLL3 (at 24 MHz)		—	✓	—	—	—	✓	—	—
	ADPLL		✓	—	—	—	✓	—	—	—
	OSC32K		✓	✓	✓	✓	✓	✓	✓	✓
	SIOSC4M		✓	✓	✓	✓	✓	✓	✓	✓
	SIOSC32K		✓	✓	✓	✓	✓	✓	✓	✓
Power Domain	POWER_CPU	PC	ON				ON			
	POWER_MAIN	PM	ON				ON			
	POWER_DMAC	PD	ON/OFF/RET				ON/OFF/RET			
	POWER_FLASH	PF	ON/OFF/RET				ON/OFF/RET			
	POWER_SRAM0	PS0	ON/OFF/RET/WAIT				ON/OFF/RET/WAIT			
	POWER_SRAM1	PS1	ON/OFF/RET/WAIT				ON/OFF/RET/WAIT			
	POWER_SRAM2	PS2	ON/OFF/RET/WAIT				ON/OFF/RET/WAIT			
	POWER_USB	PU	ON OFF	ON OFF	ON OFF	ON OFF	ON OFF	ON OFF	ON OFF	ON OFF
	POWER_CRYPT	PE	ON/OFF/RET				ON/OFF/RET			
	POWER_ADPLL	PADPLL	ON OFF	ON OFF	ON OFF	ON OFF	ON OFF	ON OFF	ON OFF	ON OFF
	POWER_EFUSE	PEFUSE	OFF				OFF			
	POWER_PLL	PPLL	ON OFF	ON OFF	ON OFF	ON OFF	ON OFF	ON OFF	ON OFF	ON OFF
	POWER_AON	PA	ON				ON			
	POWER_PPIER1	PPIER1	ON/OFF/RET				ON/OFF/RET			
	POWER_ADCC12	PADCC12	ON/OFF/RET				ON/OFF/RET			
	POWER_ADCC24	PADCC24	ON/OFF/RET				ON/OFF/RET			
Clock Domain	CD_MPIER	cpu fclk	ON				ON (SLEEPING) ON → OFF (SLEEPDEEP)			
		cpu hclk	ON				ON → OFF			
		other clk	ON/OFF				ON/OFF			
	CD_PPIER0	-	ON/OFF				ON/OFF			
	CD_PPIER1	-	ON/OFF				ON/OFF			
	CD_PPIER2	-	ON/OFF				ON/OFF			
	CD_UART0	-	ON/OFF				ON/OFF			
	CD_UART1	-	ON/OFF				ON/OFF			
	CD_UART2	-	ON/OFF				ON/OFF			
	CD_ADCC12	-	ON/OFF				ON/OFF			
	CD_ADCC24	-	ON/OFF				ON/OFF			
	CD_SPIC	-	ON/OFF				ON/OFF			
	CD_USBB	-	ON OFF	OFF			ON OFF	OFF		
	CD_USBI	-	ON OFF	OFF			ON OFF	OFF		
	CD_PMULV	-	ON				ON			
	CD_RTC	-	ON/OFF				ON/OFF			

Table 4.11 SLEEP1/SLEEP2 Mode

			SLEEP1				SLEEP2			
			ModeA	ModeB	ModeC	ModeD	ModeA	ModeB	ModeC	ModeD
Returnable Condition	Interrupt from each Peripheral		✓				—			
	Wakeup Interrupt by RTC		✓				✓			
	Wakeup Interrupt by GPIO		✓				✓			
	Wakeup Interrupt by BrownOut		✓				✓			
	Wakeup Interrupt by CPU Debug		✓				✓			
Clock Source	OSC12M/OSC12M3		✓	✓	✓	—	✓	✓	✓	—
	PLL		✓	✓	—	—	✓	✓	—	—
	PLL9 (at 36 MHz)		—	✓	—	—	—	✓	—	—
	PLL3 (at 24 MHz)		—	✓	—	—	—	✓	—	—
	ADPLL		✓	—	—	—	✓	—	—	—
	OSC32K		✓	✓	✓	✓	✓	✓	✓	✓
	SIOSC4M		✓	✓	✓	✓	✓	✓	✓	✓
	SIOSC32K		✓	✓	✓	✓	✓	✓	✓	✓
Power Domain	POWER_CPU	PC	ON				ON			
	POWER_MAIN	PM	ON				ON			
	POWER_DMAC	PD	ON/OFF/RET				ON/OFF/RET			
	POWER_FLASH	PF	ON/OFF/RET				ON/OFF/RET			
	POWER_SRAM0	PS0	ON/OFF/RET/WAIT				ON/OFF/RET/WAIT			
	POWER_SRAM1	PS1	ON/OFF/RET/WAIT				ON/OFF/RET/WAIT			
	POWER_SRAM2	PS2	ON/OFF/RET/WAIT				ON/OFF/RET/WAIT			
	POWER_USB	PU	ON OFF	ON OFF	ON OFF	ON OFF	ON OFF	ON OFF	ON OFF	ON OFF
	POWER_CRYPT	PE	ON/OFF/RET				ON/OFF/RET			
	POWER_ADPLL	PADPLL	ON OFF	ON OFF	ON OFF	ON OFF	ON OFF	ON OFF	ON OFF	ON OFF
	POWER_EFUSE	PEFUSE	OFF				OFF			
	POWER_PLL	PPLL	ON OFF	ON OFF	ON OFF	ON OFF	ON OFF	ON OFF	ON OFF	ON OFF
	POWER_AON	PA	ON				ON			
	POWER_PPIER1	PPIER1	ON/OFF/RET				ON/OFF/RET			
	POWER_ADCC12	PADCC12	ON/OFF/RET				ON/OFF/RET			
	POWER_ADCC24	PADCC24	ON/OFF/RET				ON/OFF/RET			
Clock Domain	CD_MPIER	cpu fclk	ON (SLEEPING) ON → OFF (SLEEPDEEP)				ON (SLEEPING) ON → OFF (SLEEPDEEP)			
		cpu hclk	ON → OFF				ON → OFF			
		other clk	ON → OFF				ON → OFF			
	CD_PPIER0	-	ON/OFF				ON → OFF			
	CD_PPIER1	-	ON/OFF				ON → OFF			
	CD_PPIER2	-	ON/OFF				ON → OFF			
	CD_UART0	-	ON/OFF				ON → OFF			
	CD_UART1	-	ON/OFF				ON → OFF			
	CD_UART2	-	ON/OFF				ON → OFF			
	CD_ADCC12	-	ON/OFF				ON → OFF			
	CD_ADCC24	-	ON/OFF				ON → OFF			
	CD_SPIC	-	ON → OFF				ON → OFF			
	CD_USBB	-	ON/OFF				ON/OFF			
	CD_USBI	-	ON/OFF				ON/OFF			
	CD_PMULV	-	ON				ON			
	CD_RTC	-	ON/OFF				ON/OFF			

Table 4.12 WAIT/WAIT-RETENTION/RETENTION Mode

			WAIT	WAIT-RETENTION	RETENTION
			ModeD	ModeD	ModeD
Returnable Condition	Interrupt from each Peripheral		—	—	—
	Wakeup Interrupt by RTC		✓	✓	✓
	Wakeup Interrupt by GPIO		✓	✓	✓
	Wakeup Interrupt by BrownOut		✓	✓	✓
	Wakeup Interrupt by CPU Debug		✓	✓	✓
Clock Source	OSC12M/OSC12M3		→ OFF	→ OFF	→ OFF
	PLL (48 MHz)		→ OFF	→ OFF	→ OFF
	PLL9 (36 MHz)		→ OFF	→ OFF	→ OFF
	PLL3 (24 MHz)		→ OFF	→ OFF	→ OFF
	ADPLL		→ OFF	→ OFF	→ OFF
	OSC32K		✓	✓	✓
	SIOSC4M		Other → OFF	Other → OFF	Other → OFF
	SIOSC32K		✓	✓	✓
Power Domain	POWER_CPU	PC	ON	ON ON → RET	ON → RET
	POWER_MAIN	PM	ON	ON	ON → RET
	POWER_DMAC	PD	ON OFF RET	ON ON → RET OFF RET	ON → RET OFF RET
	POWER_FLASH	PF			
	POWER_CRYPT	PE			
	POWER_PPIER1	PPIER1			
	POWER_ADCC12	PADCC12			
	POWER_ADCC24	PADCC24			
	POWER_SRAM0	PS0	ON ON → WAIT OFF WAIT	ON ON → WAIT OFF WAIT	ON → RET OFF RET
	POWER_SRAM1	PS1			
	POWER_SRAM2	PS2			
	POWER_USB	PU	ON OFF	ON OFF	OFF
	POWER_ADPLL	PADPLL	OFF ON → OFF	OFF ON → OFF	OFF ON → OFF
	POWER_PLL	PPLL			
	POWER_EFUSE	PEFUSE	OFF	OFF	OFF
	POWER_AON	PA	ON	ON	ON
Clock Domain	CD_MPIER	cpu fclk	ON → OFF	ON → OFF	ON → OFF
		cpu hclk	ON → OFF	ON → OFF	ON → OFF
		other clk	ON → OFF	ON → OFF	ON → OFF
	CD_PPIER0	-	ON → OFF	ON → OFF	ON → OFF
	CD_PPIER1	-	ON → OFF	ON → OFF	ON → OFF
	CD_PPIER2	-	ON → OFF	ON → OFF	ON → OFF
	CD_UART0	-	ON → OFF	ON → OFF	ON → OFF
	CD_UART1	-	ON → OFF	ON → OFF	ON → OFF
	CD_UART2	-	ON → OFF	ON → OFF	ON → OFF
	CD_ADCC12	-	ON → OFF	ON → OFF	ON → OFF
	CD_ADCC24	-	ON → OFF	ON → OFF	ON → OFF
	CD_SPIC	-	ON → OFF	ON → OFF	ON → OFF
	CD_USBB	-	OFF	OFF	OFF
	CD_USBi	-	OFF	OFF	OFF
	CD_PMULV	-	ON → OFF	ON → OFF	ON → OFF
	CD_RTC	-	ON/OFF	ON/OFF	ON/OFF

Table 4.13 RTC/STOP Mode

			RTC	STOP
			MCU_VDD33	MCU_VDD33—
Returnable Condition	Interrupt from each Peripheral		—	—
	Wakeup Interrupt by RTC		✓	—
	Wakeup Interrupt by GPIO		✓	✓
	Wakeup Interrupt by BrownOut		✓	✓
	Wakeup Interrupt by CPU Debug		✓	✓
Clock Source	OSC12M/OSC12M3		→ OFF	→ OFF
	PLL (48 MHz)		→ OFF	→ OFF
	PLL9 (36 MHz)		→ OFF	→ OFF
	PLL3 (24 MHz)		→ OFF	→ OFF
	ADPLL		→ OFF	→ OFF
	OSC32K		✓	OFF
	SIOSC4M		Other → OFF	Other → OFF
	SIOSC32K		✓	OFF
Power Domain	POWER_CPU	PC	ON → OFF	ON → OFF
	POWER_MAIN	PM	ON → OFF	ON → OFF
	POWER_DMAC	PD	ON → OFF OFF RET → OFF	ON → OFF OFF RET → OFF
	POWER_FLASH	PF		
	POWER_CRYPT	PE		
	POWER_PPIER1	PPIER1		
	POWER_ADCC12	PADCC12		
	POWER_ADCC24	PADCC24		
	POWER_SRAM0	PS0	ON → OFF OFF RET → OFF WAIT → OFF	ON → OFF OFF RET → OFF WAIT → OFF
	POWER_SRAM1	PS1		
	POWER_SRAM2	PS2		
	POWER_USB	PU	OFF	OFF
	POWER_EFUSE	PEFUSE	OFF	OFF
	POWER_ADPLL	PADPLL	ON → OFF OFF	ON → OFF OFF
	POWER_PLL	PPLL	ON → OFF OFF	ON → OFF OFF
	POWER_AON	PA	ON	ON
Clock Domain	CD_MPIER	cpu fclk	ON → OFF	ON → OFF
		cpu hclk	ON → OFF	ON → OFF
		other clk	ON → OFF	ON → OFF
	CD_PPIER0	-	ON → OFF	ON → OFF
	CD_PPIER1	-	ON → OFF	ON → OFF
	CD_PPIER2	-	ON → OFF	ON → OFF
	CD_UART0	-	ON → OFF	ON → OFF
	CD_UART1	-	ON → OFF	ON → OFF
	CD_UART2	-	ON → OFF	ON → OFF
	CD_ADCC12	-	ON → OFF	ON → OFF
	CD_ADCC24	-	ON → OFF	ON → OFF
	CD_SPIC	-	ON → OFF	ON → OFF
	CD_USBB	-	OFF	OFF
	CD_USBi	-	OFF	OFF
	CD_PMULV	-	ON → OFF	ON → OFF
	CD_RTC	-	ON/OFF	OFF

4.4. Boot Sequence

4.4.1. Power Supply Sequence

The power supply sequence starts when the MCU_SYS_RESET_N pin signal is set to High after the MCU_VDD33/MCU_VDD33_DCDC powers are supplied. The power supply sequence controls until the PMUHV deasserts the reset to the PMULV.

4.4.1.1. SPI Power internal supply mode (BOOTMODE3 = 0)

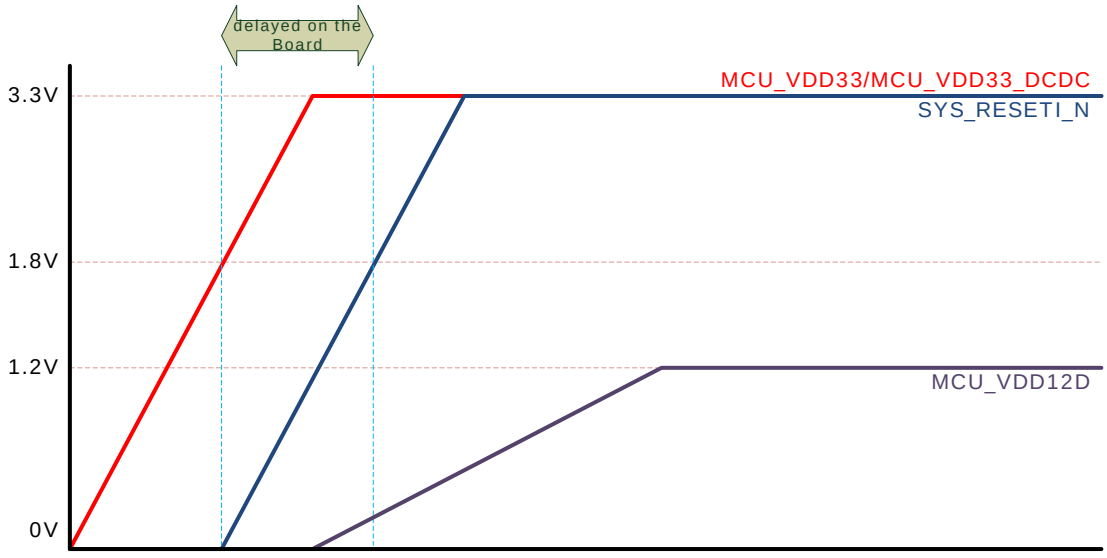

Figure 4.8 Power supply sequence (BOOTMODE3 = 0)

The MCU_SYS_RESET_N pin should be High when the MCU_VDD33 becomes 1.8 V or more.

4.4.1.2. SPI Power External Supply Mode (BOOTMODE3 = 1)

The SPI power is supplied by MCU_VDD33.

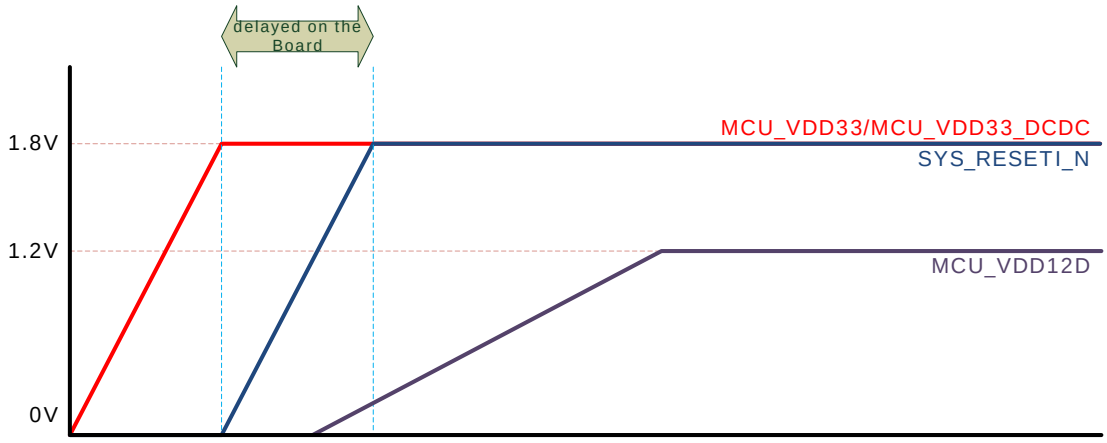

Figure 4.9 Power supply sequence (BOOTMODE3 = 1)

The MCU_SYS_RESET_N pin should be High when the MCU_VDD33 becomes 1.8 V or more.

4.4.2. Start-up Sequence

The start-up sequence is defined as the sequence between the reset deassertion to the PMULV and the reset deassertion to the CPU. It is controlled by the PMULV.

After the start-up sequence, PM,PC,PF,PS0,PS1,PS2,and PP1 domain is supplied with the power.

After the start-up sequence, software should set the followings.

- Set the SIOSC4M trimming valuesx - Refer to 4.1.4.3 SIOSC4M.
- Shut down the power of the PEFUSE - Refer to 4.2.3.6 PEFUSE Domain Control.
- Disable the DCDC Software Start (Enable at the power-up).
  - ***[CONFIG_DCDC_LVREG_1]***.DCDC_SSFAST should be written to 1.
- Change to DCDC External Clock Mode (Default: FreeRunMode)
  - ***[CONFIG_DCDC_LVREG_1]***.DCDC_EXTCLKMODE should be written to 1.
- Change the wait time at the voltage circuit switch.
  - ***[WAITTIME_DVSCTL]***.WAITTIME_CHGTIME should be written to 0.
- Change the wait time at the power domain control for PS0, PS1 and PS2.
  - ***[WAITTIME_PSW]***.WAITTIME_PSW_OFF and ***[WAITTIME_PSW]***.WAITTIME_PSW_ON should be written to 0x9.
- Set the OSC32K trimming values - Refer to 4.1.4.2 OSC32K.
  - When the SIOSC32K is used, this is not necessary.
- Set the SIOSC32K trimming values - Refer to 4.1.4.4 SIOSC32K.
  - When the OSC32K is used, this is not necessary.
- 32.768 kHz oscillation starts.
  - When the 32.768 kHz clock is not used, this is not necessary.

4.5. BrownOut Control

The BrownOut control is the control which shuts down the system in safety when the MCU_VDD33 is decreasing. It is disabled as the default. The write 1 to ***[BROWNOUTMODE].***BROWNOUT_EN enables it.

One of two detection ways of the BrownOut is selected by the ***[BROWNOUTMODE]*** register.

- BrownOut interrupt request
  - The LVD detects the decrease of the MCU_VDD33 voltage and the BrownOut interrupt is asserted.
  - It will return to the ACTIVE state when the interrupt is asserted in PowerMode transition state.
  - In the case of RTC/STOP mode, it depends on the value of ***[BROWNOUTMODE]***.BOMODE_INT_FOR_RTC_STOP. If it is 0, it return to the ACTIVE state. IF it is 1, the brownout reset is forced to be asserted by hardware.
  - After the return, the BrownOut reset is asserted by writing 1 to ***[BROWNOUTRESET]***.BOR.
- BrownOut hardware reset
  - After detecting the BrownOut, the BrownOut reset is forced to be asserted by hardware.

After BrownOut reset, should be rebooted by HW reset. After reboot, check the cause of reset. ***[STATUS_LVRST]***.STATUS_LVRST_BOR is special register. It is not initialized by the all reset. After boot, it must be initialized by setting 1. It must prepare an identification flag in the FLASH in order to distinguish the boot and reboot.

4.5.1. Precaution

Before the setting is changed, the ***[BROWNOUTMODE].***BROWNOUT_EN should be written to 0.

4.6. IO Control

4.6.1. IO Buffer Control

There are the three IO control functions

In the Start-up Sequence and Power Mode Transition Control, the IO controls are done by hardware. Software can also control the IOs.

(1) IO Output Buffer reset function
- Each power domain can be controlled separately.
- When the reset is asserted, the OutputBuffer becomes Input. And one of PullDown, PullUp, and Hi-Z is selected depending on the IO type.
- The reset and the retention are exclusive, each other. The reset is prioritized.
- This function is used when an external device power is ON and the MCU core power is OFF.

(2) IO Output Buffer retention function
- Each power domain can be controlled separately.
- In the retention state, the OutputBuffer saves the status before the retention (the information about the signal, the drivability, and PullUp or PullDown resistor).
- This function is used when an external device power is ON and the MCU core power is OFF.

(3) IO Input Buffer standby function
- This control can be done per function.
- In the standby state, the input buffer is disabled and the input signals in this product are fixed to Low.
- This function is used when an external device power is OFF and the MCU core power is ON.
- Before the transition to the standby state, the clock of the target block should be stopped and the reset should be asserted to the block.
- After the transition from the standby state, the target block should be supplied with the clock and the reset should be deasserted.

The list of the IO controls are shown in the following table.

Table 4.14 IO buffer function

Function	Target Block	Initial Value (at Power ON)
IO Output Buffer Reset Function	IO_AON (PM domain)	Reset (*1)
	IO_AON (PP1 domain)	Reset (*1)
IO Output Buffer Retention Function	IO_AON (PM domain)	— (*2)
	IO_AON (PP1 domain)	— (*2)
IO Input Buffer Standby Function	UART0 (RXD/TXD)	Standby
	UART1 (RXD/TXD)	Standby
	UART1 (RTS_N/CTS_N)	Standby
	UART2 (RXD/TXD)	Standby
	UART2 (RTS_N/CTS_N)	Standby
	I2C0	Standby
	I2C1	Standby
	I2C2	Standby
	SPIM0	Standby
	SPIM1	Standby
	SPIM2	Standby
	SPIM3	Standby
	ADCC24_SYNC	Standby
	GPIO0-15, 24-31 * GPIO is in the units of bits.	Standby

*1: The start-up sequence make it to the normal operation state.

*2: The reset state is prioritized. After the reset sequence, it becomes the normal operation state.

Table 4.15 IO control register

Control Register	Control	
[CTRL_IO_AON_Number]	Write	Refer to 5 Details of Registers
	Read	Read the setting value.

4.6.2. IO Buffer Control and PowerMode

The IO retention control is performed at the PowerMode (=WAIT-RETENTION/RETENTION/RTC/STOP mode) by the hardware sequencer. When the IO state is the IO retention state or the IO reset state before PowerMode transition, it will maintain the state.

PowerMode	Power Domain	Transition				Return			
		Current Power Domain State	Current IO State	Next Power Domain State	Next IO State	Current Power Domain State	Current IO State	Next Power Domain State	Next IO State
WAIT-RETENTION	PP1	ON	normal	RET OFF	retention	RET OFF	retention	ON	normal
			retention		retention		retention		retention
			reset		reset		reset		reset
			normal	ON	normal	ON	normal		normal
			retention		retention		retention		retention
			reset		reset		reset		reset
		RET OFF	retention	RET OFF	retention	RET OFF	retention	RET OFF	retention
			reset		reset		reset		reset
	PM	ON	normal	ON	normal	ON	normal	ON	normal
			retention		retention		retention		retention
			reset		reset		reset		reset
RETENTION	PP1	ON	normal	RET OFF	retention	RET OFF	retention	ON	normal
			retention		retention		retention		retention
			reset		reset		reset		reset
		RET OFF	retention	RET OFF	retention	RET OFF	retention	RET OFF	retention
			reset		reset		reset		reset
	PM	ON	normal	RET	retention	RET	retention	ON	normal
			retention		retention		retention		retention
			reset		reset		reset		reset
RTC STOP	PP1	ON	normal	OFF	retention	OFF	retention	ON	retention
			retention		retention		retention		retention
			reset		reset		reset		reset
		RET OFF	retention	OFF	retention	OFF	retention	ON	retention
			reset		reset		reset		reset
	PM	ON	normal	OFF	retention	OFF	retention	ON	retention
			retention		retention		retention		retention
			reset		reset		reset		reset

4.6.3. Wakeup Interrupt Detection

4 wakeup interrupts are supported.

- External input signals from GPIO pins (GPIO30/27/26/25/24/7/6/5/4/3/2/1/0).
- RTC interrupt
- CPU HotPlug control
- BrownOut interrupt

The condition of wakeup interrupt detection can be set in ***[IRQ_SETTING_number]*** register. The initial value is disabled.

It will need to be set according to specifications of the external device about GPIO. For the RTC interrupt ,the CPU HotPlug control and the brownout interrupt, the rising edge detection should be set. In addition, set the ***[IRQ_SETTING_number]*** register before setting the ***[BROWNOUTMODE]***.BROWNOUT_EN register to 1 about the brownout interrupt.

The wakeup interrupt can use by setting to one in the ***[WAKEUP_EN]*** register. The wakeup interrupt will be the starting point of PowerMode return, it notifies the cpu as the wakeup interrupt. When the ***[WAKEUP_EN]*** register is disabled, the wakeup interrupt is not the starting point of PowerMode return, it will not be notified to the CPU. Therefore, must be enabled 1bit or more ***[WAKEUP_EN]*** register.

The field that is enabled in ***[WAKEUP_EN]*** register can be confirmed by referring to the ***[WAKEUP_STATUS]*** register as a cause of wakeup interrupt. All cause of wakeup can be confirmed by referring to the ***[IRQ_STATUS]*** register. In addition, It is possible to clear the wakeup interrupt by writing 1 to it.

The external signals from GPIO pins are also used by the GPIO block. It is noted that the interrupts in both the GPIO block and the PMU block may be asserted.

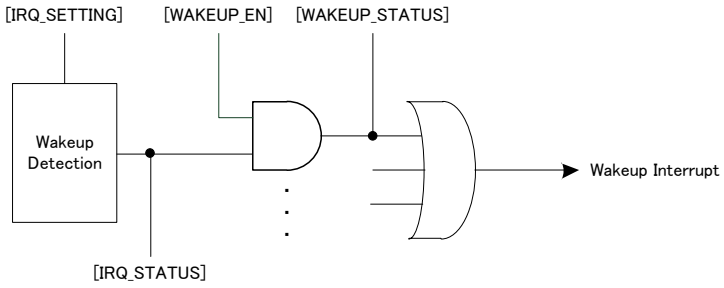

Figure 4.10 wakeup detection circuit

Table 4.16 Wakeup interrupt register

Control Register	Control	
[WAKEUP_EN]	Write	0: interrupt for wakeup disable 1: interrupt for wakeup enable
	Read	It is possible to refer the setting value.
[WAKEUP_STATUS]	Read	0: interrupt for wakeup is not output. 1: interrupt for wakeup is output.
[IRQ_SETTING_Number]	Write	bit0: rising edge bit1: falling edge bit2: low level bit3: high level * 0:disable 1:enable * In the case to use the both edge detection, write bit2 and bit3 to 1. * All 0 indicate the mask status.
	Read	Read the setting value.
[IRQ_STATUS]	Write	1: clear 0: ignored
	Read	[0]: GPIO0 Pin [1]: GPIO1 Pin [2]: GPIO2 Pin [3]: GPIO3 Pin [4]: GPIO4 Pin [5]: GPIO5 Pin [6]: GPIO6 Pin [7]: GPIO7 Pin [8]: GPIO24 Pin [9]: GPIO25 Pin [10]: GPIO26 Pin [11]: GPIO27 Pin [12]: GPIO30 Pin [15]: BrownOut [16]: RTC [17]: CPU HotPlug 1: interrupt asserted 0: interrupt deasserted

(wakeup detection setting and changing procedure)

(1) Mask the target fields of ***[IRQ_SETTING_number]*** register.
(2) Read ***[IRQ_STATUS]*** and check the interrupt state.
(3) If there is the cause of wakeup interrupt, write 1 to the target field and clear it. If there is not, this step can be skipped.
    * Even if set to the mask status in the step (1), the cause of wakeup is not cleared.
(4) Change the target field of ***[IRQ_SETTING_number]*** register.

(wakeup interrupt setting procedure)

It will be the procedure to be enabled as the wakeup interrupt.

(1) Set the cause of wakeup that is enabled by ***[WAKEUP_EN]*** according to (wakeup detection setting and changing procedure).
(2) Enable ***[WAKEUP_EN]*** register.

It will be the procedure to be disabled as the wakeup interrupt.

(1) Disable ***[WAKEUP_EN]*** register.
    * The cause of wakeup is not cleared, and it is possible to detect it.
    * If the ***[WAKEUP_EN]*** register is enabled to the cause that set 1 to the ***[IRQ_STATUS]*** register, the wakeup interrupt will be generated immediately.
    * Even if the ***[WAKEUP_EN]*** is disabled, it is possible to clear the cause that set 1 to the ***[IRQ_STATUS]*** register. In that case, it is possible to omit the control of the ***[WAKEUP_STATUS]*** and ***[WAKEUP_EN]*** from the clear procedure.

The procedure of clear is different for level detection and edge detection.

(wakeup interrupt clear procedure of edge detection)

(1) Read ***[WAKEUP_STATUS]*** register and check the cause of wakeup interrupt.
(2) Set the target field of ***[IRQ_SETTING_number]*** register to the mask state.
(3) Write 1 to the target field of ***[IRQ_STATUS]*** register and clear the cause of wakeup. By clearing the cause of wakeup in ***[IRQ_STATUS]*** register, ***[WAKEUP_STATUS]*** register is also cleared.
(4) Return form the mask state which is set in step (3) to the original state.
(5) If read the ***[WAKEUP_STATUS]*** register and it is 0, the clear procedure will be done. If is 1, return to the step (2).

(wakeup interrupt clear procedure of level detection)

(1) Read ***[WAKEUP_STATUS]*** register and check the cause of wakeup interrupt.
(2) Set the target field of ***[IRQ_SETTING_number]*** register to the mask state.
(3) Write 1 to the target field of ***[IRQ_STATUS]*** register and clear the cause of wakeup.
(4) Write 0 to the target field of ***[WAKEUP_EN]*** register and disable the detection of wakeup.
(5) Change the target field of ***[IRQ_SETTING_number]*** register to edge detection.
(6) Clear the source of wakeup interrupt.
(7) Read ***[IRQ_STATUS]*** register and make the polling until it detects the cause of wakeup interrupt.
(8) Set the target field of ***[IRQ_SETTING_number]*** register to the mask state.
(9) Write 1 to the target field of ***[IRQ_STATUS]*** register and clear the cause of wakeup.
(10) Write 1 to the target field of ***[WAKEUP_EN]*** register and enable the detection of wakeup.
(11) Return the target field of ***[IRQ_SETTING_number]*** register to the level detection.
(12) If read the ***[WAKEUP_STATUS]*** register and it is 0, the clear procedure will be done. If is 1, return to the step (2).

4.7. EFUSE Function

The EFUSE data is loaded in the shift register in the PM domain during the start-up sequence. The EFUSE Macro store the trimming values for the source clocks and the power supply circuits. The EFUSE values are loaded from the shift register to the register in the PA domain during the start-up sequence except the SIOSC4M and the SIOSC32K values.

Any data can be overwritten in the register in the PA domain, and it is possible to re-load the EFUSE value form the shift register.

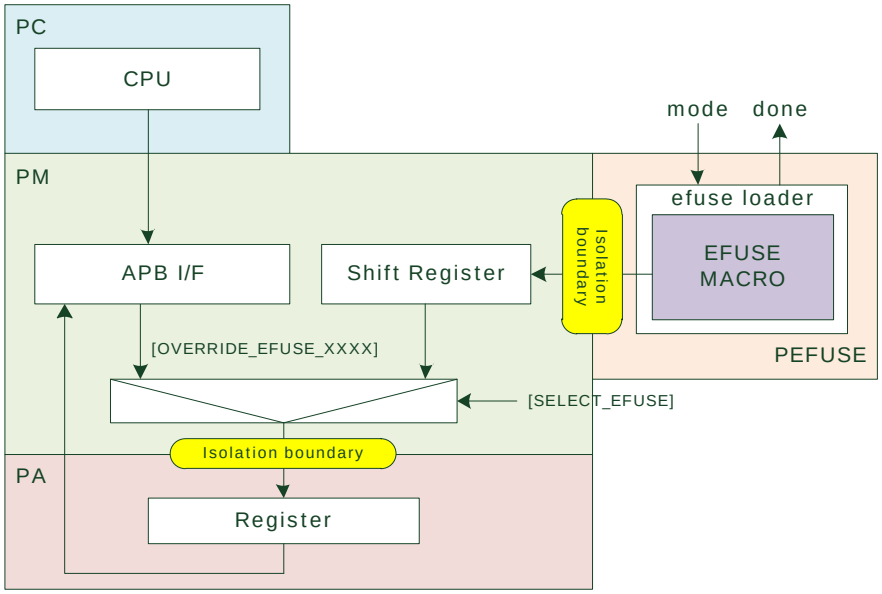

Figure 4.11 EFUSE load

(EFUSE shift register re-load)

(1) The shift register is selected by the ***[SELECT_EFUSE]*** register.

(2) A write operation is done to ***[OVERRIDE_EUFSE_[Macro name]]***. The EFUSE shift register value is set to the register.

(Override register load)

(1) The override register is selected by the ***[SELECT_EFUSE]*** register.

(2) A write operation is done to ***[OVERRIDE_EUFSE_[Macro name]]***. The override register value is set to the register.

5. Details of Registers

5.1. CG_ON_POWERDOMAIN

CG_ON_POWERDOMAIN			
Description	Clock gating ON (for each power supply domain) [Write]1: Clock stops. 0: Ignored [Read]1: Clock is stopped. 0: Clock is being supplied. * Writing also changes the values of associated individual CG registers. (Example) If writing is done to the CG_PD field, the values of the ***[CG_ON_PD]*** and ***[CG_OFF_PD]*** registers are also changed.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0000		
Physical address View0	0x4000 0000		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:12	Reserved	—	—	—
11	CG_PP1	Batch control of clocks belonging to PP1	RW oneToSet	1
10	CG_PA24	Batch control of clocks belonging to PA24	RW oneToSet	1
9	CG_PA12	Batch control of clocks belonging to PA12	RW oneToSet	1
8	CG_PU	Batch control of clocks belonging to PU	RW oneToSet	1
7	CG_PD	Batch control of clocks belonging to PD	RW oneToSet	1
6	Reserved	—	—	—
5	CG_PF	Batch control of clocks belonging to PF	RW oneToSet	0
4	CG_PS2	Batch control of clocks belonging to PS2	RW oneToSet	0
3	CG_PS1	Batch control of clocks belonging to PS1	RW oneToSet	0
2	CG_PS0	Batch control of clocks belonging to PS0	RW oneToSet	0
1	CG_PE	Batch control of clocks belonging to PE	RW oneToSet	1
0	CG_PM	Batch control of clocks belonging to PM	RW oneToSet	0

5.2. CG_OFF_POWERDOMAIN

CG_OFF_POWERDOMAIN			
Description	Clock gating OFF (for each power supply domain) [Write]1: Clock is supplied. 0: Ignored [Read]1: Clock is being supplied. 0: Clock is stopped. * Writing also changes the values of associated individual CG registers. (Example) If writing is done to the CG_PD field, the values of the ***[CG_ON_PD]*** and ***[CG_OFF_PD]*** registers are also changed.		
Address Region	pulls	**Type:**	RW
Offset	0x0000 0004		
Physical address View0	0x4000 0004		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:12	Reserved	—	—	—
11	CG_PP1	Batch control of clocks belonging to PP1	RW oneToSet	0
10	CG_PA24	Batch control of clocks belonging to PA24	RW oneToSet	0
9	CG_PA12	Batch control of clocks belonging to PA12	RW oneToSet	0
8	CG_PU	Batch control of clocks belonging to PU	RW oneToSet	0
7	CG_PD	Batch control of clocks belonging to PD	RW oneToSet	0
6	Reserved	—	—	—
5	CG_PF	Batch control of clocks belonging to PF	RW oneToSet	1
4	CG_PS2	Batch control of clocks belonging to PS2	RW oneToSet	1
3	CG_PS1	Batch control of clocks belonging to PS1	RW oneToSet	1
2	CG_PS0	Batch control of clocks belonging to PS0	RW oneToSet	1
1	CG_PE	Batch control of clocks belonging to PE	RW oneToSet	0
0	CG_PM	Batch control of clocks belonging to PM	RW oneToSet	1

5.3. DCG_POWERDOMAIN

DCG_POWERDOMAIN			
Description	Dynamic clock gating (for each power supply domain) [Write]1: Dynamic clock gating enable. 0: Dynamic clock gating disable. [Read] A configured value can be checked. * Writing also changes values of associated individual DCG registers. (Example) If writing is done to the DCG_PD field, the ***[DCG_PD]*** register value is also changed.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0010		
Physical address View0	0x4000 0010		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:12	Reserved	—	—	—
11	DCG_PP1	Batch control of clocks belonging to PP1	RW modify	0
10	DCG_PA24	Batch control of clocks belonging to PA24	RW modify	0
9	DCG_PA12	Batch control of clocks belonging to PA12	RW modify	0
8	DCG_PU	Batch control of clocks belonging to PU	RW modify	0
7	DCG_PD	Batch control of clocks belonging to PD	RW modify	0
6	Reserved	—	—	—
5	DCG_PF	Batch control of clocks belonging to PF	RW modify	0
4	DCG_PS2	Batch control of clocks belonging to PS2	RW modify	0
3	DCG_PS1	Batch control of clocks belonging to PS1	RW modify	0
2	DCG_PS0	Batch control of clocks belonging to PS0	RW modify	0
1	DCG_PE	Batch control of clocks belonging to PE	RW modify	0
0	DCG_PM	Batch control of clocks belonging to PM	RW modify	0

5.4. SRST_ON_POWERDOMAIN

SRST_ON_POWERDOMAIN			
Description	Soft reset ON (for each power supply domain) [Write]1: Reset assert. 0: Ignored. [Read]1: Reset assert in progress. 0: Reset deassert in progress * Writing also changes values of associated individual SRST registers. (Example) If writing is done to the SRST_PD field, the values of the ***[SRST_ON_PD]*** and ***[SRST_OFF_PD]*** registers are also changed.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0020		
Physical address View0	0x4000 0020		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:12	Reserved	—	—	—
11	SRST_PP1	Batch control of resets belonging to PP1	RW oneToSet	1
10	SRST_PA24	Batch control of resets belonging to PA24	RW oneToSet	1
9	SRST_PA12	Batch control of resets belonging to PA12	RW oneToSet	1
8	Reserved	—	—	—
7	SRST_PD	Batch control of resets belonging to PD	RW oneToSet	1
6	Reserved	—	—	—
5	SRST_PF	Batch control of resets belonging to PF	RW oneToSet	0
4:2	Reserved	—	—	—
1	SRST_PE	Batch control of resets belonging to PE	RW oneToSet	1
0	SRST_PM	Batch control of resets belonging to PM	RW oneToSet	0

5.5. SRST_OFF_POWERDOMAIN

SRST_OFF_POWERDOMAIN			
Description	Soft reset OFF (for each power supply domain) [Write]1: Reset deassert. 0: Ignored. [Read]1: Reset deassert in progress. 0: Reset assert in progress * Writing also changes values of associated individual SRST registers. (Example) If writing is done to the SRST_PD field, the values of the ***[SRST_ON_PD]*** and ***[SRST_OFF_PD]*** registers are also changed.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0024		
Physical address View0	0x4000 0024		
Physical address View1	—		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:12	Reserved	—	—	—
11	SRST_PP1	Batch control of resets belonging to PP1	RW oneToSet	0
10	SRST_PA24	Batch control of resets belonging to PA24	RW oneToSet	0
9	SRST_PA12	Batch control of resets belonging to PA12	RW oneToSet	0
8	Reserved	—	—	—
7	SRST_PD	Batch control of resets belonging to PD	RW oneToSet	0
6	Reserved	—	—	—
5	SRST_PF	Batch control of resets belonging to PF	RW oneToSet	1
4:2	Reserved	—	—	—
1	SRST_PE	Batch control of resets belonging to PE	RW oneToSet	0
0	SRST_PM	Batch control of resets belonging to PM	RW oneToSet	1

5.6. CG_ON_PM_0

CG_ON_PM_0			
Description	Clock gating ON (PM/PS0/PS1/PS2) [Write]1: Clock stops. 0: Ignored. [Read]1: Clock is stopped. 0: Clock is being supplied.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0100		
Physical address View0	0x4000 0100		
Physical address View1	—		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:28	Reserved	—	—	—
27	CG_mpierclk_sramc_pclk	SRAMC APB I/F clock * Also changed by writing to ***[CG_ON_POWERDOMAIN]***.CG_PM and ***[CG_OFF_POWERDOMAIN]***.CG_PM.	RW oneToSet	0
26	CG_mpierclk_sramc_s2hclk	SRAMC PS2 clock * Also changed by writing to	RW oneToSet	0

		[CG_ON_POWERDOMAIN].CG_PS2 and ***[CG_OFF_POWERDOMAIN]***.CG_PS2.		
25	CG_mpierclk_sramc_s1hclk	SRAMC PS1 clock * Also changed by writing to ***[CG_ON_POWERDOMAIN]***.CG_PS1 and ***[CG_OFF_POWERDOMAIN]***.CG_PS1.	RW oneToSet	0
24	CG_mpierclk_sramc_s0hclk	SRAMC PS0 clock * Also changed by writing to ***[CG_ON_POWERDOMAIN]***.CG_PS0 and ***[CG_OFF_POWERDOMAIN]***.CG_PS0.	RW oneToSet	0
23	CG_mpierclk_sramc_hclk	SRAMC AHB I/F clock (T0/T1/T2) * Also changed by writing to ***[CG_ON_POWERDOMAIN]***.CG_PM and ***[CG_OFF_POWERDOMAIN]***.CG_PM.	RW oneToSet	0
22	CG_mpierclk_evm_pclk	EVM clock * Also changed by writing to ***[CG_ON_POWERDOMAIN]***.CG_PM and ***[CG_OFF_POWERDOMAIN]***.CG_PM.	RW oneToSet	1
21	Reserved	—	—	—
20	CG_mpierclk_h2pm_hclk	H2APB clock * Also changed by writing to ***[CG_ON_POWERDOMAIN]***.CG_PM and ***[CG_OFF_POWERDOMAIN]***.CG_PM.	RW oneToSet	1
19:0	Reserved	—	—	—

5.7. CG_ON_PM_1

CG_ON_PM_1			
Description	Clock gating ON (PM) [Write]1: Clock stops. 0: Ignored. [Read]1: Clock is stopped. 0: Clock is being supplied. * Also changed by writing to ***[CG_ON_POWERDOMAIN]***.CG_PM and ***[CG_OFF_POWERDOMAIN]***.CG_PM.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0104		
Physical address View0	0x4000 0104		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:30	Reserved	—	—	—
29	CG_ppier0clk_spim3_sclk	SPIM3 serial clock	RW oneToSet	1
28	CG_ppier0clk_spim3_pclk	SPIM3 APB I/F clock	RW oneToSet	1
27	CG_ppier0clk_spim2_sclk	SPIM2 serial clock	RW oneToSet	1
26	CG_ppier0clk_spim2_pclk	SPIM2 APB I/F clock	RW oneToSet	1

25	CG_ppier0clk_i2c2_sclk	I2C2 serial clock	RW oneToSet	1
24	CG_ppier0clk_i2c2_pclk	I2C2 APB I/F clock	RW oneToSet	1
23	CG_ppier0clk_tmr_ch1_timclk	TMR ch1 timer counter clock	RW oneToSet	1
22	Reserved	—	—	—
21	CG_ppier0clk_tmr_ch0_timclk	TMR ch0 timer counter clock	RW oneToSet	1
20	Reserved	—	—	—
19	CG_ppier0clk_tmr_pclk	TMR APB I/F clock	RW oneToSet	1
18:16	Reserved	—	—	—
15	CG_ppier0clk_advtmr_ch3_timclk	ADVTMR ch3 timer counter clock	RW oneToSet	1
14	Reserved	—	—	—
13	CG_ppier0clk_advtmr_ch2_timclk	ADVTMR ch2 timer counter clock	RW oneToSet	1
12	Reserved	—	—	—
11	CG_ppier0clk_advtmr_ch1_timclk	ADVTMR ch1 timer counter clock	RW oneToSet	1
10	Reserved	—	—	—
9	CG_ppier0clk_advtmr_ch0_timclk	ADVTMR ch0 timer counter clock	RW oneToSet	1
8	Reserved	—	—	—
7	CG_ppier0clk_advtmr_pclk	ADVTMR APB I/F clock	RW oneToSet	1
6	Reserved	—	—	—
5	CG_ppier0clk_wdt_wdtclk	WDT timer counter clock	RW oneToSet	1
4	CG_ppier0clk_wdt_pclk	WDT APB I/F clock	RW oneToSet	1
3	Reserved	—	—	—
2	CG_ppier0clk_rtclv_pclk	RTCLV APB I/F clock	RW oneToSet	1
1	CG_ppier0clk_h2pp0_hclk	H2APBP0 clock	RW oneToSet	1
0	CG_mpierclk_h2hp0_hclk	H2HSYNCDNP0 clock	RW oneToSet	1

5.8. CG_ON_PM_2

CG_ON_PM_2			
Description	Clock gating ON (PM) [Write]1: Clock stops. 0: Ignored. [Read]1: Clock is stopped. 0: Clock is being supplied. * Also changed by writing to ***[CG_ON_POWERDOMAIN]***.CG_PM and ***[CG_OFF_POWERDOMAIN]***.CG_PM.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0108		
Physical address View0	0x4000 0108		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:17	Reserved	—	—	—
16	CG_mpierclk_h2hp1_hclk	H2HSYNCDNP1 clock	RW oneToSet	1

15:12	Reserved	—	—	—
11	CG_uart2clk_uart2_sclk	UART2 serial clock	RW oneToSet	1
10	CG_ppier2clk_uart2_pclk	UART2 APB I/F clock	RW oneToSet	1
9	CG_ppier2clk_h2pp2_hclk	H2APBP2 clock	RW oneToSet	1
8	CG_mpierclk_h2hp2_hclk	H2HSYNCDNP2 clock	RW oneToSet	1
7	CG_ppier0clk_gpio3_pclk	GPIO3 APB I/F clock	RW oneToSet	1
6	CG_ppier0clk_gpio2_pclk	GPIO2 APB I/F clock	RW oneToSet	1
5	CG_ppier0clk_gpio1_pclk	GPIO1 APB I/F clock	RW oneToSet	1
4	CG_ppier0clk_gpio0_pclk	GPIO0 APB I/F clock	RW oneToSet	1
3:1	Reserved	—	—	—
0	CG_ppier0clk_gconf_pclk	GCONF APB I/F clock	RW oneToSet	1

5.9. CG_ON_PE

CG_ON_PE			
Description	Clock gating ON (PE) [Write]1: Clock stops. 0: Ignored. [Read]1: Clock is stopped. 0: Clock is being supplied. * Also changed by writing to ***[CG_ON_POWERDOMAIN]***.CG_PE and ***[CG_OFF_POWERDOMAIN]***.CG_PE.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0110		
Physical address View0	0x4000 0110		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:4	Reserved	—	—	—
3	CG_mpierclk_rng_coreclk	RNG core clock	RW oneToSet	1
2	CG_mpierclk_rng_busclk	RNG APB I/F clock	RW oneToSet	1
1	CG_mpierclk_aesa_coreclk	AESA core clock	RW oneToSet	1
0	CG_mpierclk_aesa_busclk	AESA APB I/F clock	RW oneToSet	1

5.10. CG_ON_PF

CG_ON_PF			
Description	Clock gating ON (PF) [Write]1: Clock stops. 0: Ignored. [Read]1: Clock is stopped. 0: Clock is being supplied. * Also changed by writing to ***[CG_ON_POWERDOMAIN]***.CG_PF and ***[CG_OFF_POWERDOMAIN]***.CG_PF.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0120		
Physical address View0	0x4000 0120		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:3	Reserved	—	—	—
2	CG_spicclk_spic_spclk	SPIC SPI clock	RW oneToSet	0
1	CG_mpierclk_spic_srclk	SPIC SRAM clock	RW oneToSet	0
0	CG_mpierclk_spic_hclk	SPIC AHB I/F clock	RW oneToSet	0

5.11. CG_ON_PD

CG_ON_PD			
Description	Clock gating ON (PD) [Write]1: Clock stops. 0: Ignored. [Read]1: Clock is stopped. 0: Clock is being supplied. * Also changed by writing to ***[CG_ON_POWERDOMAIN]***.CG_PD and ***[CG_OFF_POWERDOMAIN]***.CG_PD.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0128		
Physical address View0	0x4000 0128		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:1	Reserved	—	—	—
0	CG_mpierclk_sdmac_hclk	DMAC clock	RW oneToSet	1

5.12. CG_ON_PU

CG_ON_PU			
Description	Clock gating ON (PU) [Write]1: Clock stops. 0: Ignored. [Read]1: Clock is stopped. 0: Clock is being supplied. * Also changed by writing to ***[CG_ON_POWERDOMAIN]***.CG_PU and ***[CG_OFF_POWERDOMAIN]***.CG_PU.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 012C		
Physical address View0	0x4000 012C		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:5	Reserved	—	—	—
4	CG_usbiclk_usb2fs_usbclk	USB USB clock	RW oneToSet	1
3	CG_usbbclk_usb2fs_hclk	USB AHB I/F clock	RW oneToSet	1
2	CG_mpierclk_h2hupu_hclk	H2HSYNCUPU clock	RW oneToSet	1
1	Reserved	—	—	—
0	CG_mpierclk_h2hdnu_hclk	H2HSYNCDNU slave clock	RW oneToSet	1

5.13. CG_ON_PA12

CG_ON_PA12			
Description	Clock gating ON (PA12) [Write]1: Clock stops. 0: Ignored. [Read]1: Clock is stopped. 0: Clock is being supplied. * Also changed by writing to ***[CG_ON_POWERDOMAIN]***.CG_PA12 and ***[CG_OFF_POWERDOMAIN]***.CG_PA12.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0134		
Physical address View0	0x4000 0134		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:3	Reserved	—	—	—
2	CG_rtcclk_adcc12_rtcclk	ADC12 RTC clock	RW oneToSet	1
1	CG_adcc12aclk_adcc12_adccclk	ADC12 ADC clock	RW oneToSet	1
0	CG_ppier0clk_adcc12_pclk	ADC12 APB I/F clock	RW oneToSet	1

5.14. CG_ON_PA24

CG_ON_PA24			
Description	Clock gating ON (PA24) [Write]1: Clock stops. 0: Ignored. [Read]1: Clock is stopped. 0: Clock is being supplied. * Also changed by writing to ***[CG_ON_POWERDOMAIN]***.CG_PA24 and ***[CG_OFF_POWERDOMAIN]***.CG_PA24.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0138		
Physical address View0	0x4000 0138		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:3	Reserved	—	—	—
2	CG_rtcclk_adcc24_rtcclk	ADC24 RTC clock	RW oneToSet	1
1	CG_adcc24aclk_adcc24_adccclk	ADC24 ADC clock	RW oneToSet	1
0	CG_ppier0clk_adcc24_pclk	ADC24 APB I/F clock	RW oneToSet	1

5.15. CG_ON_PP1

CG_ON_PP1			
Description	Clock gating ON (PP1) [Write]1: Clock stops. 0: Ignored. [Read]1: Clock is stopped. 0: Clock is being supplied. * Also changed by writing to ***[CG_ON_POWERDOMAIN]***.CG_PP1 and ***[CG_OFF_POWERDOMAIN]***.CG_PP1.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 013C		
Physical address View0	0x4000 013C		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:16	Reserved	—	—	—
15	CG_uart1clk_uart1_sclk	UART1 serial clock	RW oneToSet	1
14	CG_ppier1clk_uart1_pclk	UART1 APB I/F clock	RW oneToSet	1
13	CG_uart0clk_uart0_sclk	UART0 serial clock	RW oneToSet	1
12	CG_ppier1clk_uart0_pclk	UART0 APB I/F clock	RW oneToSet	1
11	CG_ppier1clk_spim1_sclk	SPIM1 serial clock	RW oneToSet	1
10	CG_ppier1clk_spim1_pclk	SPIM1 APB I/F clock	RW oneToSet	1
9	CG_ppier1clk_spim0_sclk	SPIM0 serial clock	RW oneToSet	1
8	CG_ppier1clk_spim0_pclk	SPIM0 APB I/F clock	RW oneToSet	1
7	CG_ppier1clk_i2c1_sclk	I2C1 serial clock	RW	1

			oneToSet	
6	CG_ppier1clk_i2c1_pclk	I2C1 APB I/F clock	RW oneToSet	1
5	CG_ppier1clk_i2c0_sclk	I2C0 serial clock	RW oneToSet	1
4	CG_ppier1clk_i2c0_pclk	I2C0 APB I/F clock	RW oneToSet	1
3:1	Reserved	—	—	—
0	CG_ppier1clk_h2pp1_hclk	H2APBP1 clock	RW oneToSet	1

5.16. CG_ON_HARDMACRO

CG_ON_HARDMACRO			
Description	Clock gating ON (HARDMACRO) [Write]1: Clock stops. 0: Ignored. [Read]1: Clock is stopped. 0: Clock is being supplied.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0140		
Physical address View0	0x4000 0140		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:17	Reserved	—	—	—
16	CG_dcdcclk_dcdc_gatedclk	DCDC clock	RW oneToSet	0
15:1	Reserved	—	—	—
0	CG_pmulvclk_pmulv_efuseclk	EFUSE clock	RW oneToSet	0

5.17. CG_ON_REFCLK

CG_ON_REFCLK			
Description	Clock gating ON (REFCLK) [Write]1: Clock stops. 0: Ignored. [Read]1: Clock is stopped. 0: Clock is being supplied.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0148		
Physical address View0	0x4000 0148		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:17	Reserved	—	—	—
16	CG_ref32kclk_adpll_refclk	ADPLL reference clock	RW oneToSet	1
15:1	Reserved	—	—	—
0	CG_ref32kclk_pmulv_refclk	PMULV reference clock	RW oneToSet	1

5.18. CG_OFF_PM_0

CG_OFF_PM_0			
Description	Clock gating OFF (PM/PS0/PS1/PS2) [Write]1: Clock is supplied. 0: Ignored. [Read]1: Clock is being supplied. 0: Clock is stopped.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0180		
Physical address View0	0x4000 0180		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:28	Reserved	—	—	—
27	CG_mpierclk_sramc_pclk	SRAMC APB I/F clock * Also changed by writing to ***[CG_ON_POWERDOMAIN]***.CG_PM and ***[CG_OFF_POWERDOMAIN]***.CG_PM.	RW oneToSet	1
26	CG_mpierclk_sramc_s2hclk	SRAMC PS2 clock * Also changed by writing to ***[CG_ON_POWERDOMAIN]***.CG_PS2 and ***[CG_OFF_POWERDOMAIN]***.CG_PS2.	RW oneToSet	1
25	CG_mpierclk_sramc_s1hclk	SRAMC PS1 clock * Also changed by writing to ***[CG_ON_POWERDOMAIN]***.CG_PS1 and ***[CG_OFF_POWERDOMAIN]***.CG_PS1.	RW oneToSet	1
24	CG_mpierclk_sramc_s0hclk	SRAMC PS0 clock * Also changed by writing to ***[CG_ON_POWERDOMAIN]***.CG_PS0 and ***[CG_OFF_POWERDOMAIN]***.CG_PS0.	RW oneToSet	1
23	CG_mpierclk_sramc_hclk	SRAMC AHB I/F clock (T0/T1/T2) * Also changed by writing to ***[CG_ON_POWERDOMAIN]***.CG_PM and ***[CG_OFF_POWERDOMAIN]***.CG_PM.	RW oneToSet	1
22	CG_mpierclk_evm_pclk	EVM clock * Also changed by writing to ***[CG_ON_POWERDOMAIN]***.CG_PM and ***[CG_OFF_POWERDOMAIN]***.CG_PM.	RW oneToSet	0
21	Reserved	—	—	—
20	CG_mpierclk_h2pm_hclk	H2APB clock * Also changed by writing to ***[CG_ON_POWERDOMAIN]***.CG_PM and ***[CG_OFF_POWERDOMAIN]***.CG_PM.	RW oneToSet	0
19:0	Reserved	—	—	—

5.19. CG_OFF_PM_1

CG_OFF_PM_1			
Description	Clock gating OFF (PM) [Write]1: Clock is supplied. 0: Ignored. [Read]1: Clock is being supplied. 0: Clock is stopped. * Also changed by writing to ***[CG_ON_POWERDOMAIN]***.CG_PM and ***[CG_OFF_POWERDOMAIN]***.CG_PM.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0184		
Physical address View0	0x4000 0184		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:30	Reserved	—	—	—
29	CG_ppier0clk_spim3_sclk	SPIM3 serial clock	RW oneToSet	0
28	CG_ppier0clk_spim3_pclk	SPIM3 APB I/F clock	RW oneToSet	0
27	CG_ppier0clk_spim2_sclk	SPIM2 serial clock	RW oneToSet	0
26	CG_ppier0clk_spim2_pclk	SPIM2 APB I/F clock	RW oneToSet	0
25	CG_ppier0clk_i2c2_sclk	I2C2 serial clock	RW oneToSet	0
24	CG_ppier0clk_i2c2_pclk	I2C2 APB I/F clock	RW oneToSet	0
23	CG_ppier0clk_tmr_ch1_timclk	TMR ch1 timer counter clock	RW oneToSet	0
22	Reserved	—	—	—
21	CG_ppier0clk_tmr_ch0_timclk	TMR ch0 timer counter clock	RW oneToSet	0
20	Reserved	—	—	—
19	CG_ppier0clk_tmr_pclk	TMR APB I/F clock	RW oneToSet	0
18:16	Reserved	—	—	—
15	CG_ppier0clk_advtmr_ch3_timclk	ADVTMR ch3 timer counter clock	RW oneToSet	0
14	Reserved	—	—	—
13	CG_ppier0clk_advtmr_ch2_timclk	ADVTMR ch2 timer counter clock	RW oneToSet	0
12	Reserved	—	—	—
11	CG_ppier0clk_advtmr_ch1_timclk	ADVTMR ch1 timer counter clock	RW oneToSet	0
10	Reserved	—	—	—
9	CG_ppier0clk_advtmr_ch0_timclk	ADVTMR ch0 timer counter clock	RW oneToSet	0
8	Reserved	—	—	—
7	CG_ppier0clk_advtmr_pclk	ADVTMR APB I/F clock	RW oneToSet	0
6	Reserved	—	—	—
5	CG_ppier0clk_wdt_wdtclk	WDT timer counter clock	RW oneToSet	0
4	CG_ppier0clk_wdt_pclk	WDT APB I/F clock	RW oneToSet	0
3	Reserved	—	—	—
2	CG_ppier0clk_rtclv_pclk	RTCLV APB I/F clock	RW oneToSet	0

1	CG_ppier0clk_h2pp0_hclk	H2APBP0 clock	RW oneToSet	0
0	CG_mpierclk_h2hp0_hclk	H2HSYNCDNP0 clock	RW oneToSet	0

5.20. CG_OFF_PM_2

CG_OFF_PM_2			
Description	Clock gating OFF (PM) [Write]1: Clock is supplied. 0: Ignored. [Read]1: Clock is being supplied. 0: Clock is stopped. * Also changed by writing to ***[CG_ON_POWERDOMAIN]***.CG_PM and ***[CG_OFF_POWERDOMAIN]***.CG_PM.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0188		
Physical address View0	0x4000 0188		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:17	Reserved	—	—	—
16	CG_mpierclk_h2hp1_hclk	H2HSYNCDNP1 clock	RW oneToSet	0
15:12	Reserved	—	—	—
11	CG_uart2clk_uart2_sclk	UART2 serial clock	RW oneToSet	0
10	CG_ppier2clk_uart2_pclk	UART2 APB I/F clock	RW oneToSet	0
9	CG_ppier2clk_h2pp2_hclk	H2APBP2 clock	RW oneToSet	0
8	CG_mpierclk_h2hp2_hclk	H2HSYNCDNP2 clock	RW oneToSet	0
7	CG_ppier0clk_gpio3_pclk	GPIO3 APB I/F clock	RW oneToSet	0
6	CG_ppier0clk_gpio2_pclk	GPIO2 APB I/F clock	RW oneToSet	0
5	CG_ppier0clk_gpio1_pclk	GPIO1 APB I/F clock	RW oneToSet	0
4	CG_ppier0clk_gpio0_pclk	GPIO0 APB I/F clock	RW oneToSet	0
3:1	Reserved	—	—	—
0	CG_ppier0clk_gconf_pclk	GCONF APB I/F clock	RW oneToSet	0

5.21. CG_OFF_PE

CG_OFF_PE			
Description	Clock gating OFF (PE) [Write]1: Clock is supplied. 0: Ignored. [Read]1: Clock is being supplied. 0: Clock is stopped. * Also changed by writing to ***[CG_ON_POWERDOMAIN]***.CG_PE and ***[CG_OFF_POWERDOMAIN]***.CG_PE.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0190		
Physical address View0	0x4000 0190		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:4	Reserved	—	—	—
3	CG_mpierclk_rng_coreclk	RNG core clock	RW oneToSet	0
2	CG_mpierclk_rng_busclk	RNG APB I/F clock	RW oneToSet	0
1	CG_mpierclk_aesa_coreclk	AESA core clock	RW oneToSet	0
0	CG_mpierclk_aesa_busclk	AESA APB I/F clock	RW oneToSet	0

5.22. CG_OFF_PF

CG_OFF_PF			
Description	Clock gating OFF (PF) [Write]1: Clock is supplied. 0: Ignored. [Read]1: Clock is being supplied. 0: Clock is stopped. * Also changed by writing to ***[CG_ON_POWERDOMAIN]***.CG_PF and ***[CG_OFF_POWERDOMAIN]***.CG_PF.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 01A0		
Physical address View0	0x4000 01A0		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:3	Reserved	—	—	—
2	CG_spicclk_spic_spclk	SPIC SPI clock	RW oneToSet	1
1	CG_mpierclk_spic_srclk	SPIC SRAM clock	RW oneToSet	1
0	CG_mpierclk_spic_hclk	SPIC AHB I/F clock	RW oneToSet	1

5.23. CG_OFF_PD

CG_OFF_PD				
Description	Clock gating OFF (PD) [Write]1: Clock is supplied. 0: Ignored. [Read]1: Clock is being supplied. 0: Clock is stopped. * Also changed by writing to ***[CG_ON_POWERDOMAIN]***.CG_PD and ***[CG_OFF_POWERDOMAIN]***.CG_PD.			
Address Region	pmulv	**Type:**	RW	
Offset	0x0000 01A8			
Physical address View0	0x4000 01A8			
Physical address View1	—			

Bitfield Details

Bits	Name	Description	Access	Reset
31:1	Reserved	—	—	—
0	CG_mpierclk_sdmac_hclk	DMAC clock	RW oneToSet	0

5.24. CG_OFF_PU

CG_OFF_PU				
Description	Clock gating OFF (PU) [Write]1: Clock is supplied. 0: Ignored. [Read]1: Clock is being supplied. 0: Clock is stopped. * Also changed by writing to ***[CG_ON_POWERDOMAIN]***.CG_PU and ***[CG_OFF_POWERDOMAIN]***.CG_PU.			
Address Region	pmulv	**Type:**	RW	
Offset	0x0000 01AC			
Physical address View0	0x4000 01AC			
Physical address View1	—			

Bitfield Details

Bits	Name	Description	Access	Reset
31:5	Reserved	—	—	—
4	CG_usbiclk_usb2fs_usbclk	USB USB clock	RW oneToSet	0
3	CG_usbbclk_usb2fs_hclk	USB AHB I/F clock	RW oneToSet	0
2	CG_mpierclk_h2hupu_hclk	H2HSYNCUPU clock	RW oneToSet	0
1	Reserved	—	—	—
0	CG_mpierclk_h2hdnu_hclk	H2HSYNCDNU slave clock	RW oneToSet	0

5.25. CG_OFF_PA12

CG_OFF_PA12			
Description	Clock gating OFF (PA12) [Write]1: Clock is supplied. 0: Ignored. [Read]1: Clock is being supplied. 0: Clock is stopped. * Also changed by writing to ***[CG_ON_POWERDOMAIN]***.CG_PA12 and ***[CG_OFF_POWERDOMAIN]***.CG_PA12.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 01B4		
Physical address View0	0x4000 01B4		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:3	Reserved	—	—	—
2	CG_rtcclk_adcc12_rtcclk	ADC12 RTC clock	RW oneToSet	0
1	CG_adcc12aclk_adcc12_adccclk	ADC12 ADC clock	RW oneToSet	0
0	CG_ppier0clk_adcc12_pclk	ADC12 APB I/F clock	RW oneToSet	0

5.26. CG_OFF_PA24

CG_OFF_PA24			
Description	Clock gating OFF (PA24) [Write]1: Clock is supplied. 0: Ignored. [Read]1: Clock is being supplied. 0: Clock is stopped. * Also changed by writing to ***[CG_ON_POWERDOMAIN]***.CG_PA24 and ***[CG_OFF_POWERDOMAIN]***.CG_PA24.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 01B8		
Physical address View0	0x4000 01B8		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:3	Reserved	—	—	—
2	CG_rtcclk_adcc24_rtcclk	ADC24 RTC clock	RW oneToSet	0
1	CG_adcc24aclk_adcc24_adccclk	ADC24 ADC clock	RW oneToSet	0
0	CG_ppier0clk_adcc24_pclk	ADC24 APB I/F clock	RW oneToSet	0

5.27. CG_OFF_PP1

CG_OFF_PP1			
Description	Clock gating OFF (PP1) [Write]1: Clock is supplied. 0: Ignored. [Read]1: Clock is being supplied. 0: Clock is stopped. * Also changed by writing to ***[CG_ON_POWERDOMAIN]***.CG_PP1 and ***[CG_OFF_POWERDOMAIN]***.CG_PP1.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 01BC		
Physical address View0	0x4000 01BC		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:16	Reserved	—	—	—
15	CG_uart1clk_uart1_sclk	UART1 serial clock	RW oneToSet	0
14	CG_ppier1clk_uart1_pclk	UART1 APB I/F clock	RW oneToSet	0
13	CG_uart0clk_uart0_sclk	UART0 serial clock	RW oneToSet	0
12	CG_ppier1clk_uart0_pclk	UART0 APB I/F clock	RW oneToSet	0
11	CG_ppier1clk_spim1_sclk	SPIM1 serial clock	RW oneToSet	0
10	CG_ppier1clk_spim1_pclk	SPIM1 APB I/F clock	RW oneToSet	0
9	CG_ppier1clk_spim0_sclk	SPIM0 serial clock	RW oneToSet	0
8	CG_ppier1clk_spim0_pclk	SPIM0 APB I/F clock	RW oneToSet	0
7	CG_ppier1clk_i2c1_sclk	I2C1 serial clock	RW oneToSet	0
6	CG_ppier1clk_i2c1_pclk	I2C1 APB I/F clock	RW oneToSet	0
5	CG_ppier1clk_i2c0_sclk	I2C0 serial clock	RW oneToSet	0
4	CG_ppier1clk_i2c0_pclk	I2C0 APB I/F clock	RW oneToSet	0
3:1	Reserved	—	—	—
0	CG_ppier1clk_h2pp1_hclk	H2APBP1 clock	RW oneToSet	0

5.28. CG_OFF_HARDMACRO

CG_OFF_HARDMACRO					
Description	Clock gating OFF (HARDMACRO) [Write]1: Clock is supplied. 0: Ignored. [Read]1: Clock is being supplied. 0: Clock is stopped.				
Address Region	pmulv		**Type:**	RW	
Offset	0x0000 01C0				
Physical address View0	0x4000 01C0				
Physical address View1	—				
Bitfield Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:17	Reserved	—		—	—
16	CG_dcdcclk_dcdc_gatedclk	DCDC clock		RW oneToSet	1
15:1	Reserved	—		—	—
0	CG_pmulvclk_pmulv_efuseclk	EFUSE clock		RW oneToSet	1

5.29. CG_OFF_REFCLK

CG_OFF_REFCLK					
Description	Clock gating OFF (HARDMACRO) [Write]1: Clock is supplied. 0: Ignored. [Read]1: Clock is being supplied. 0: Clock is stopped.				
Address Region	pmulv		**Type:**	RW	
Offset	0x0000 01C8				
Physical address View0	0x4000 01C8				
Physical address View1	—				
Bitfield Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:17	Reserved	—		—	—
16	CG_ref32kclk_adpll_refclk	ADPLL reference clock		RW oneToSet	0
15:1	Reserved	—		—	—
0	CG_ref32kclk_pmulv_refclk	PMULV reference clock		RW oneToSet	0

5.30. DCG_PM_0

DCG_PM_0					
Description	Dynamic clock gating (PM) [Write]1: Dynamic clock gating enable. 0: Dynamic clock gating disable [Read] A configured value can be checked.				
Address Region	pmulv		**Type:**	RW	
Offset	0x0000 0200				
Physical address View0	0x4000 0200				
Physical address View1	—				
Bitfield Details					

Bits	Name	Description	Access	Reset
31	DCG_pmulvclk_pmulv_lv0clk	PMULV clock * Also changed by writing to ***[DCG_POWERDOMAIN]***.DCG_PM.	RW modify	0
30	DCG_pmulvclk_h2ppmu_hclk	H2APBPMU clock * Also changed by writing to ***[DCG_POWERDOMAIN]***.DCG_PM.	RW modify	0
29	DCG_pmulvclk_h2hasync_hclk	H2HASYNC master clock * Also changed by writing to ***[DCG_POWERDOMAIN]***.DCG_PM.	RW modify	0
28	DCG_mpierclk_h2hasync_hclk	H2HASYNC slave clock * Also changed by writing to ***[DCG_POWERDOMAIN]***.DCG_PM.	RW modify	0
27	DCG_mpierclk_sramc_pclk	SRAMC APB I/F clock * Also changed by writing to ***[DCG_POWERDOMAIN]***.DCG_PM.	RW modify	0
26	DCG_mpierclk_sramc_s2hclk	SRAMC PS2 clock * Also changed by writing to ***[DCG_POWERDOMAIN]***.DCG_PS2.	RW modify	0
25	DCG_mpierclk_sramc_s1hclk	SRAMC PS1 clock * Also changed by writing to ***[DCG_POWERDOMAIN]***.DCG_PS1.	RW modify	0
24	DCG_mpierclk_sramc_s0hclk	SRAMC PS0 clock * Also changed by writing to ***[DCG_POWERDOMAIN]***.DCG_PS0.	RW modify	0
23	DCG_mpierclk_sramc_hclk	SRAMC AHB I/F clock * Also changed by writing to ***[DCG_POWERDOMAIN]***.DCG_PM.	RW modify	0
22	DCG_mpierclk_evm_pclk	EVM clock * Also changed by writing to ***[DCG_POWERDOMAIN]***.DCG_PM.	RW modify	0
21	Reserved	—	—	—
20	DCG_mpierclk_h2pm_hclk	H2APBM clock * Also changed by writing to ***[DCG_POWERDOMAIN]***.DCG_PM.	RW modify	0
19:1	Reserved	—	—	—
0	DCG_mpierclk_mpier_hclk	MPIER clock * Also changed by writing to ***[DCG_POWERDOMAIN]***.DCG_PM.	RW modify	0

5.31. DCG_PM_1

DCG_PM_1			
Description	Dynamic clock gating (PM) [Write]1: Dynamic clock gating enable. 0: Dynamic clock gating disable [Read] A configured value can be checked. * Also changed by writing to ***[DCG_POWERDOMAIN]***.DCG_PM.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0204		
Physical address View0	0x4000 0204		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:30	Reserved	—	—	—
29	DCG_ppier0clk_spim3_sclk	SPIM3 serial clock	RW modify	0
28	DCG_ppier0clk_spim3_pclk	SPIM3 APB I/F clock	RW	0

			modify	
27	DCG_ppier0clk_spim2_sclk	SPIM2 serial clock	RW modify	0
26	DCG_ppier0clk_spim2_pclk	SPIM2 APB I/F clock	RW modify	0
25	DCG_ppier0clk_i2c2_sclk	I2C2 serial clock	RW modify	0
24	DCG_ppier0clk_i2c2_pclk	I2C2 APB I/F clock	RW modify	0
23	DCG_ppier0clk_tmr_ch1_timclk	TMR ch1 timer counter clock	RW modify	0
22	Reserved	—	—	—
21	DCG_ppier0clk_tmr_ch0_timclk	TMR ch0 timer counter clock	RW modify	0
20	Reserved	—	—	—
19	DCG_ppier0clk_tmr_pclk	TMR APB I/F clock	RW modify	0
18:16	Reserved	—	—	—
15	DCG_ppier0clk_advtmr_ch3_timclk	ADVTMR ch3 timer counter clock	RW modify	0
14	Reserved	—	—	—
13	DCG_ppier0clk_advtmr_ch2_timclk	ADVTMR ch2 timer counter clock	RW modify	0
12	Reserved	—	—	—
11	DCG_ppier0clk_advtmr_ch1_timclk	ADVTMR ch1 timer counter clock	RW modify	0
10	Reserved	—	—	—
9	DCG_ppier0clk_advtmr_ch0_timclk	ADVTMR ch0 timer counter clock	RW modify	0
8	Reserved	—	—	—
7	DCG_ppier0clk_advtmr_pclk	ADVTMR APB I/F clock	RW modify	0
6	Reserved	—	—	—
5	DCG_ppier0clk_wdt_wdtclk	WDT timer counter clock	RW modify	0
4	DCG_ppier0clk_wdt_pclk	WDT APB I/F clock	RW modify	0
3:2	Reserved	—	—	—
1	DCG_ppier0clk_h2pp0_hclk	H2APBP0 clock	RW modify	0
0	DCG_mpierclk_h2hp0_hclk	H2HSYNCDNP0 clock	RW modify	0

5.32. DCG_PM_2

DCG_PM_2			
Description	Dynamic clock gating (PM) [Write]1: Dynamic clock gating enable. 0: Dynamic clock gating disable [Read] A configured value can be checked. * Also changed by writing to ***[DCG_POWERDOMAIN]***.DCG_PM.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0208		
Physical address View0	0x4000 0208		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:17	Reserved	—	—	—

16	DCG_mpierclk_h2hp1_hclk	H2HSYNCDNP1 clock	RW modify	0
15:12	Reserved	—	—	—
11	DCG_uart2clk_uart2_sclk	UART2 serial clock	RW modify	0
10	DCG_ppier2clk_uart2_pclk	UART2 APB I/F clock	RW modify	0
9	DCG_ppier2clk_h2pp2_hclk	H2APBP2 clock	RW modify	0
8	DCG_mpierclk_h2hp2_hclk	H2HSYNCDNP2 clock	RW modify	0
7	DCG_ppier0clk_gpio3_pclk	GPIO3 APB I/F clock	RW modify	0
6	DCG_ppier0clk_gpio2_pclk	GPIO2 APB I/F clock	RW modify	0
5	DCG_ppier0clk_gpio1_pclk	GPIO1 APB I/F clock	RW modify	0
4	DCG_ppier0clk_gpio0_pclk	GPIO0 APB I/F clock	RW modify	0
3:1	Reserved	—	—	—
0	DCG_ppier0clk_gconf_pclk	GCONF APB I/F clock	RW modify	0

5.33. DCG_PE

DCG_PE			
Description	Dynamic clock gating (PE) [Write]1: Dynamic clock gating enable. 0: Dynamic clock gating disable [Read] A configured value can be checked. * Also changed by writing to ***[DCG_POWERDOMAIN]***.DCG_PE.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0210		
Physical address View0	0x4000 0210		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:4	Reserved	—	—	—
3	DCG_mpierclk_rng_coreclk	RNG core clock	RW modify	0
2	DCG_mpierclk_rng_busclk	RNG APB I/F clock	RW modify	0
1	DCG_mpierclk_aesa_coreclk	AESA core clock	RW modify	0
0	DCG_mpierclk_aesa_busclk	AESA APB I/F clock	RW modify	0

5.34. DCG_PF

DCG_PF			
Description	Dynamic clock gating (PF) [Write]1: Dynamic clock gating enable. 0: Dynamic clock gating disable [Read] A configured value can be checked. * Also changed by writing to ***[DCG_POWERDOMAIN]***.DCG_PF.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0220		
Physical address View0	0x4000 0220		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:3	Reserved	—	—	—
2	DCG_spicclk_spic_spclk	SPIC SPI clock	RW modify	0
1	DCG_mpierclk_spic_srclk	SPIC SRAM clock	RW modify	0
0	DCG_mpierclk_spic_hclk	SPIC AHB I/F clock	RW modify	0

5.35. DCG_PD

DCG_PD			
Description	Dynamic clock gating (PD) [Write]1: Dynamic clock gating enable. 0: Dynamic clock gating disable [Read] A configured value can be checked. * Also changed by writing to ***[DCG_POWERDOMAIN]***.DCG_PD.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0228		
Physical address View0	0x4000 0228		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:1	Reserved	—	—	—
0	DCG_mpierclk_sdmac_hclk	DMAC clock	RW modify	0

5.36. DCG_PU

DCG_PU			
Description	Dynamic clock gating (PU) [Write]1: Dynamic clock gating enable. 0: Dynamic clock gating disable [Read] A configured value can be checked. * Also changed by writing to ***[DCG_POWERDOMAIN]***.DCG_PU.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 022C		
Physical address View0	0x4000 022C		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:1	Reserved	—	—	—
0	DCG_mpierclk_h2hdnu_hclk	H2HSYNCDNU slave clock	RW modify	0

5.37. DCG_PA12

DCG_PA12			
Description	Dynamic clock gating (PA12) [Write]1: Dynamic clock gating enable. 0: Dynamic clock gating disable [Read] A configured value can be checked. * Also changed by writing to ***[DCG_POWERDOMAIN]***.DCG_PA12.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0234		
Physical address View0	0x4000 0234		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:2	Reserved	—	—	—
1	DCG_adcc12aclk_adcc12_adccclk	ADC12 ADC clock	RW modify	0
0	DCG_ppier0clk_adcc12_pclk	ADC12 APB I/F clock	RW modify	0

5.38. DCG_PA24

DCG_PA24			
Description	Dynamic clock gating (PA24) [Write]1: Dynamic clock gating enable. 0: Dynamic clock gating disable [Read] A configured value can be checked. * Also changed by writing to ***[DCG_POWERDOMAIN]***.DCG_PA24.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0238		
Physical address View0	0x4000 0238		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset

31:2	Reserved	—	—	—
1	DCG_adcc24aclk_adcc24_adccclk	ADC24 ADC clock	RW modify	0
0	DCG_ppier0clk_adcc24_pclk	ADC24 APB I/F clock	RW modify	0

5.39. DCG_PP1

DCG_PP1			
Description	Dynamic clock gating (PP1) [Write]1: Dynamic clock gating enable. 0: Dynamic clock gating disable [Read] A configured value can be checked. * Also changed by writing to ***[DCG_POWERDOMAIN]***.DCG_PP1.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 023C		
Physical address View0	0x4000 023C		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:16	Reserved	—	—	—
15	DCG_uart1clk_uart1_sclk	UART1 serial clock	RW modify	0
14	DCG_ppier1clk_uart1_pclk	UART1 APB I/F clock	RW modify	0
13	DCG_uart0clk_uart0_sclk	UART0 serial clock	RW modify	0
12	DCG_ppier1clk_uart0_pclk	UART0 APB I/F clock	RW modify	0
11	DCG_ppier1clk_spim1_sclk	SPIM1 serial clock	RW modify	0
10	DCG_ppier1clk_spim1_pclk	SPIM1 APB I/F clock	RW modify	0
9	DCG_ppier1clk_spim0_sclk	SPIM0 serial clock	RW modify	0
8	DCG_ppier1clk_spim0_pclk	SPIM0 APB I/F clock	RW modify	0
7	DCG_ppier1clk_i2c1_sclk	I2C1 serial clock	RW modify	0
6	DCG_ppier1clk_i2c1_pclk	I2C1 APB I/F clock	RW modify	0
5	DCG_ppier1clk_i2c0_sclk	I2C0 serial clock	RW modify	0
4	DCG_ppier1clk_i2c0_pclk	I2C0 APB I/F clock	RW modify	0
3:1	Reserved	—	—	—
0	DCG_ppier1clk_h2pp1_hclk	H2APBP1 clock	RW modify	0

5.40. CLKREQ_CONFIG_PE

CLKREQ_CONFIG_PE			
Description	Sets the clock supply period extension after bus transaction. 0x0: 0cycle (no extension) 0x1: 1cycle 0x2: 2cycle 0x3: 3cycle 0x4: 4cycle 0x5: 5cycle 0x6: 6cycle 0x7: 7cycle 0x8: 8cycle 0x9: 9cycle 0xA: 10cycle 0xB: 11cycle 0xC: 12cycle 0xD: 13cycle 0xE: 14cycle 0xF: 15cycle		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0290		
Physical address View0	0x4000 0290		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:20	Reserved	—	—	—
19:16	POSTCLK_LENGTH_mpierclk_rng_busclk	RNG APB I/F clock	RW modify	0x2
15:4	Reserved	—	—	—
3:0	POSTCLK_LENGTH_mpierclk_aesa_busclk	AESA APB I/F clock	RW modify	0x2

5.41. SRST_ON_PM_0

SRST_ON_PM_0			
Description	Soft reset ON (PM) [Write]1: Reset assert. 0: Ignored. [Read]1: Reset assert in progress. 0: Reset deassert in progress * Also changed by writing to ***[SRST_ON_POWERDOMAIN]***.CG_PM and ***[SRST_OFF_POWERDOMAIN]***.CG_PM.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0300		
Physical address View0	0x4000 0300		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:28	Reserved	—	—	—
27	SRST_asyncrst_sramc_prstn	SRAMC APB I/F reset	RW oneToSet	0
26:25	Reserved	—	—	—
24	SRST_asyncrst_sramc_hrstn	SRAMC AHB I/F reset	RW oneToSet	0
23	Reserved	—	—	—

22	SRST_asyncrst_evm_prstn	EVM reset	RW oneToSet	1
21	Reserved	—	—	—
20	SRST_asyncrst_h2pm_hrstn	H2APBM reset	RW oneToSet	1
19:0	Reserved	—	—	—

5.42. SRST_ON_PM_1

SRST_ON_PM_1			
Description	Soft reset ON (PM) [Write]1: Reset assert. 0: Ignored. [Read]1: Reset assert in progress. 0: Reset deassert in progress * Also changed by writing to ***[SRST_ON_POWERDOMAIN]***.CG_PM and ***[SRST_OFF_POWERDOMAIN]***.CG_PM.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0304		
Physical address View0	0x4000 0304		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:30	Reserved	—	—	—
29	SRST_asyncrst_spim3_srstn	SPIM3 serial reset	RW oneToSet	1
28	SRST_asyncrst_spim3_prstn	SPIM3 APB I/F reset	RW oneToSet	1
27	SRST_asyncrst_spim2_srstn	SPIM2 serial reset	RW oneToSet	1
26	SRST_asyncrst_spim2_prstn	SPIM2 APB I/F reset	RW oneToSet	1
25	SRST_asyncrst_i2c2_srstn	I2C2 serial reset	RW oneToSet	1
24	SRST_asyncrst_i2c2_prstn	I2C2 APB I/F reset	RW oneToSet	1
23:20	Reserved	—	—	—
19	SRST_asyncrst_tmr_prstn	TMR reset	RW oneToSet	1
18:8	Reserved	—	—	—
7	SRST_asyncrst_advtmr_prstn	ADVTMR reset	RW oneToSet	1
6:5	Reserved	—	—	—
4	SRST_asyncrst_wdt_prstn	WDT reset.	RW oneToSet	1
3	SRST_asyncrst_rtclv_busrstn	RTCLV timer reset	RW oneToSet	1
2	SRST_asyncrst_rtclv_prstn	RTCLV APB I/F reset	RW oneToSet	1
1	SRST_asyncrst_h2pp0_hrstn	H2APBP0 reset	RW oneToSet	1
0	SRST_asyncrst_h2hp0_hrstn	H2HSYNCDNP0 reset	RW oneToSet	1

5.43. SRST_ON_PM_2

SRST_ON_PM_2			
Description	Soft reset ON (PM) [Write]1: Reset assert. 0: Ignored. [Read]1: Reset assert in progress. 0: Reset deassert in progress * Also changed by writing to ***[SRST_ON_POWERDOMAIN]***.CG_PM and ***[SRST_OFF_POWERDOMAIN]***.CG_PM.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0308		
Physical address View0	0x4000 0308		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:17	Reserved	—	—	—
16	SRST_asyncrst_h2hp1_hrstn	H2HSYNCDNP1 reset	RW oneToSet	1
15:12	Reserved	—	—	—
11	SRST_asyncrst_uart2_srstn	UART2 serial reset.	RW oneToSet	1
10	SRST_asyncrst_uart2_prstn	UART2 APB I/F reset	RW oneToSet	1
9	SRST_asyncrst_h2pp2_hrstn	H2APBP2 reset	RW oneToSet	1
8	SRST_asyncrst_h2hp2_hrstn	H2HSYNCDNP2 reset	RW oneToSet	1
7	SRST_asyncrst_gpio3_prstn	GPIO3 APB I/F reset	RW oneToSet	1
6	SRST_asyncrst_gpio2_prstn	GPIO2 APB I/F reset	RW oneToSet	1
5	SRST_asyncrst_gpio1_prstn	GPIO1 APB I/F reset	RW oneToSet	1
4	SRST_asyncrst_gpio0_prstn	GPIO0 APB I/F reset	RW oneToSet	1
3:1	Reserved	—	—	—
0	SRST_asyncrst_gconf_prstn	GCONF APB I/F reset	RW oneToSet	1

5.44. SRST_ON_PE

SRST_ON_PE			
Description	Soft reset ON (PE) [Write]1: Reset assert. 0: Ignored. [Read]1: Reset assert in progress. 0: Reset deassert in progress * Also changed by writing to ***[SRST_ON_POWERDOMAIN]***.CG_PE and ***[SRST_OFF_POWERDOMAIN]***.CG_PE.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0310		
Physical address View0	0x4000 0310		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:3	Reserved	—	—	—
2	SRST_asyncrst_rng_rstn	RNG reset	RW	1

			oneToSet	
1	Reserved	—	—	—
0	SRST_asyncrst_aesa_rstn	AESA reset	RW oneToSet	1

5.45. SRST_ON_PF

SRST_ON_PF			
Description	Soft reset ON (PF) [Write]1: Reset assert. 0: Ignored. [Read]1: Reset assert in progress. 0: Reset deassert in progress * Also changed by writing to ***[SRST_ON_POWERDOMAIN]***.CG_PF and ***[SRST_OFF_POWERDOMAIN]***.CG_PF.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0320		
Physical address View0	0x4000 0320		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:4	Reserved	—	—	—
3	SRST_asyncrst_spic_spifrstn	SPIC SPIF reset	RW oneToSet	0
2	SRST_asyncrst_spic_sprstn	SPIC SPI reset	RW oneToSet	0
1	SRST_asyncrst_spic_srrstn	SPIC SRAM reset	RW oneToSet	0
0	SRST_asyncrst_spic_hrstn	SPIC AHB I/F reset	RW oneToSet	0

5.46. SRST_ON_PD

SRST_ON_PD			
Description	Soft reset ON (PD) [Write]1: Reset assert. 0: Ignored. [Read]1: Reset assert in progress. 0: Reset deassert in progress * Also changed by writing to ***[SRST_ON_POWERDOMAIN]***.CG_PD and ***[SRST_OFF_POWERDOMAIN]***.CG_PD.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0328		
Physical address View0	0x4000 0328		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:1	Reserved	—	—	—
0	SRST_asyncrst_sdmac_hrstn	DMAC reset	RW oneToSet	1

5.47. SRST_ON_PU

SRST_ON_PU			
Description	Soft reset ON (PU) [Write]1: Reset assert. 0: Ignored. [Read]1: Reset assert in progress. 0: Reset deassert in progress * Also changed by writing to ***[SRST_ON_POWERDOMAIN]***.CG_PU and ***[SRST_OFF_POWERDOMAIN]***.CG_PU.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 032C		
Physical address View0	0x4000 032C		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:5	Reserved	—	—	—
4	SRST_asyncrst_usb2fs_usbrstn	USB USB reset	RW oneToSet	1
3	SRST_asyncrst_usb2fs_hrstn	USB AHB I/F reset	RW oneToSet	1
2	SRST_asyncrst_h2hupu_hrstn	H2HSYNCUPU reset	RW oneToSet	1
1	Reserved	—	—	—
0	SRST_asyncrst_h2hdnu_hrstn	H2HSYNCDNU reset	RW oneToSet	1

5.48. SRST_ON_PA12

SRST_ON_PA12			
Description	Soft reset ON (PM) [Write]1: Reset assert. 0: Ignored. [Read]1: Reset assert in progress. 0: Reset deassert in progress * Also changed by writing to ***[SRST_ON_POWERDOMAIN]***.CG_PM and ***[SRST_OFF_POWERDOMAIN]***.CG_PM.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0334		
Physical address View0	0x4000 0334		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:2	Reserved	—	—	—
1	SRST_asyncrst_adcc12_adcrstn	ADCC12 ADC reset	RW oneToSet	1
0	SRST_asyncrst_adcc12_prstn	ADCC12 APB I/F reset	RW oneToSet	1

5.49. SRST_ON_PA24

SRST_ON_PA24			
Description	Soft reset ON (PA24) [Write]1: Reset assert. 0: Ignored. [Read]1: Reset assert in progress. 0: Reset deassert in progress * Also changed by writing to ***[SRST_ON_POWERDOMAIN]***.CG_PA24 and ***[SRST_OFF_POWERDOMAIN]***.CG_PA24.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0338		
Physical address View0	0x4000 0338		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:2	Reserved	—	—	—
1	SRST_asyncrst_adcc24_adcrstn	ADCC24 ADC reset	RW oneToSet	1
0	SRST_asyncrst_adcc24_prstn	ADCC24 APB I/F reset	RW oneToSet	1

5.50. SRST_ON_PP1

SRST_ON_PP1			
Description	Soft reset ON (PP1) [Write]1: Reset assert. 0: Ignored. [Read]1: Reset assert in progress. 0: Reset deassert in progress * Also changed by writing to ***[SRST_ON_POWERDOMAIN]***.CG_PP1 and ***[SRST_OFF_POWERDOMAIN]***.CG_PP1.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 033C		
Physical address View0	0x4000 033C		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:16	Reserved	—	—	—
15	SRST_asyncrst_uart1_srstn	UART1 serial reset.	RW oneToSet	1
14	SRST_asyncrst_uart1_prstn	UART1 APB I/F reset	RW oneToSet	1
13	SRST_asyncrst_uart0_srstn	UART0 serial reset.	RW oneToSet	1
12	SRST_asyncrst_uart0_prstn	UART0 APB I/F reset	RW oneToSet	1
11	SRST_asyncrst_spim1_srstn	SPIM1 serial reset	RW oneToSet	1
10	SRST_asyncrst_spim1_prstn	SPIM1 APB I/F reset	RW oneToSet	1
9	SRST_asyncrst_spim0_srstn	SPIM0 serial reset	RW oneToSet	1
8	SRST_asyncrst_spim0_prstn	SPIM0 APB I/F reset	RW oneToSet	1
7	SRST_asyncrst_i2c1_srstn	I2C1 serial reset	RW oneToSet	1
6	SRST_asyncrst_i2c1_prstn	I2C1 APB I/F reset	RW	1

			oneToSet	
5	SRST_asyncrst_i2c0_srstn	I2C0 serial reset	RW oneToSet	1
4	SRST_asyncrst_i2c0_prstn	I2C0 APB I/F reset	RW oneToSet	1
3:1	Reserved	—	—	—
0	SRST_asyncrst_h2pp1_hrstn	H2APBP1 reset	RW oneToSet	1

5.51. SRST_OFF_PM_0

SRST_OFF_PM_0			
Description	Soft reset OFF (PM) [Write]1: Reset deassert. 0: Ignored. [Read]1: Reset deassert in progress. 0: Reset assert in progress * Also changed by writing to ***[SRST_ON_POWERDOMAIN]***.CG_PM and ***[SRST_OFF_POWERDOMAIN]***.CG_PM.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0380		
Physical address View0	0x4000 0380		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:28	Reserved	—	—	—
27	SRST_asyncrst_sramc_prstn	SRAMC APB I/F reset	RW oneToSet	1
26:25	Reserved	—	—	—
24	SRST_asyncrst_sramc_hrstn	SRAMC AHB I/F reset	RW oneToSet	1
23	Reserved	—	—	—
22	SRST_asyncrst_evm_prstn	EVM reset	RW oneToSet	0
21	Reserved	—	—	—
20	SRST_asyncrst_h2pm_hrstn	H2APBM reset	RW oneToSet	0
19:0	Reserved	—	—	—

5.52. SRST_OFF_PM_1

SRST_OFF_PM_1			
Description	Soft reset OFF (PM) [Write]1: Reset deassert. 0: Ignored. [Read]1: Reset deassert in progress. 0: Reset assert in progress * Also changed by writing to ***[SRST_ON_POWERDOMAIN]***.CG_PM and ***[SRST_OFF_POWERDOMAIN]***.CG_PM.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0384		
Physical address View0	0x4000 0384		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:30	Reserved	—	—	—

29	SRST_asyncrst_spim3_srstn	SPIM3 serial reset	RW oneToSet	0
28	SRST_asyncrst_spim3_prstn	SPIM3 APB I/F reset	RW oneToSet	0
27	SRST_asyncrst_spim2_srstn	SPIM2 serial reset	RW oneToSet	0
26	SRST_asyncrst_spim2_prstn	SPIM2 APB I/F reset	RW oneToSet	0
25	SRST_asyncrst_i2c2_srstn	I2C2 serial reset	RW oneToSet	0
24	SRST_asyncrst_i2c2_prstn	I2C2 APB I/F reset	RW oneToSet	0
23:20	Reserved	—	—	—
19	SRST_asyncrst_tmr_prstn	TMR reset	RW oneToSet	0
18:8	Reserved	—	—	—
7	SRST_asyncrst_advtmr_prstn	ADVTMR reset	RW oneToSet	0
6:5	Reserved	—	—	—
4	SRST_asyncrst_wdt_prstn	WDT reset.	RW oneToSet	0
3	SRST_asyncrst_rtclv_busrstn	RTCLV timer reset	RW oneToSet	0
2	SRST_asyncrst_rtclv_prstn	RTCLV APB I/F reset	RW oneToSet	0
1	SRST_asyncrst_h2pp0_hrstn	H2APBP0 reset	RW oneToSet	0
0	SRST_asyncrst_h2hp0_hrstn	H2HSYNCDNP0 reset	RW oneToSet	0

5.53. SRST_OFF_PM_2

SRST_OFF_PM_2			
Description	Soft reset OFF (PM) [Write]1: Reset deassert. 0: Ignored. [Read]1: Reset deassert in progress. 0: Reset assert in progress * Also changed by writing to ***[SRST_ON_POWERDOMAIN]***.CG_PM and ***[SRST_OFF_POWERDOMAIN]***.CG_PM.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0388		
Physical address View0	0x4000 0388		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:17	Reserved	—	—	—
16	SRST_asyncrst_h2hp1_hrstn	H2HSYNCDNP1 reset	RW oneToSet	0
15:12	Reserved	—	—	—
11	SRST_asyncrst_uart2_srstn	UART2 serial reset.	RW oneToSet	0
10	SRST_asyncrst_uart2_prstn	UART2 APB I/F reset	RW oneToSet	0
9	SRST_asyncrst_h2pp2_hrstn	H2APBP2 reset	RW oneToSet	0
8	SRST_asyncrst_h2hp2_hrstn	H2HSYNCDNP2 reset	RW oneToSet	0
7	SRST_asyncrst_gpio3_prstn	GPIO3 APB I/F reset	RW oneToSet	0

6	SRST_asyncrst_gpio2_prstn	GPIO2 APB I/F reset	RW oneToSet	0
5	SRST_asyncrst_gpio1_prstn	GPIO1 APB I/F reset	RW oneToSet	0
4	SRST_asyncrst_gpio0_prstn	GPIO0 APB I/F reset	RW oneToSet	0
3:1	Reserved	—	—	—
0	SRST_asyncrst_gconf_prstn	GCONF APB I/F reset	RW oneToSet	0

5.54. SRST_OFF_PE

SRST_OFF_PE			
Description	Soft reset OFF (PE) [Write]1: Reset deassert. 0: Ignored. [Read]1: Reset deassert in progress. 0: Reset assert in progress * Also changed by writing to ***[SRST_ON_POWERDOMAIN]***.CG_PE and ***[SRST_OFF_POWERDOMAIN]***.CG_PE.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0390		
Physical address View0	0x4000 0390		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:3	Reserved	—	—	—
2	SRST_asyncrst_rng_rstn	RNG reset	RW oneToSet	0
1	Reserved	—	—	—
0	SRST_asyncrst_aesa_rstn	AESA reset	RW oneToSet	0

5.55. SRST_OFF_PF

SRST_OFF_PF			
Description	Soft reset OFF (PF) [Write]1: Reset deassert. 0: Ignored. [Read]1: Reset deassert in progress. 0: Reset assert in progress * Also changed by writing to ***[SRST_ON_POWERDOMAIN]***.CG_PF and ***[SRST_OFF_POWERDOMAIN]***.CG_PF.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 03A0		
Physical address View0	0x4000 03A0		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:4	Reserved	—	—	—
3	SRST_asyncrst_spic_spifrstn	SPIC SPIF reset	RW oneToSet	1
2	SRST_asyncrst_spic_sprstn	SPIC SPI reset	RW oneToSet	1
1	SRST_asyncrst_spic_srrstn	SPIC SRAM reset	RW oneToSet	1
0	SRST_asyncrst_spic_hrstn	SPIC AHB I/F reset	RW oneToSet	1

5.56. SRST_OFF_PD

SRST_OFF_PD			
Description	Soft reset OFF (PD) [Write]1: Reset deassert. 0: Ignored. [Read]1: Reset deassert in progress. 0: Reset assert in progress * Also changed by writing to ***[SRST_ON_POWERDOMAIN]***.CG_PD and ***[SRST_OFF_POWERDOMAIN]***.CG_PD.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 03A8		
Physical address View0	0x4000 03A8		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:1	Reserved	—	—	—
0	SRST_asyncrst_sdmac_hrstn	DMAC reset	RW oneToSet	0

5.57. SRST_OFF_PU

SRST_OFF_PU			
Description	Soft reset OFF (PU) [Write]1: Reset deassert. 0: Ignored. [Read]1: Reset deassert in progress. 0: Reset assert in progress * Also changed by writing to ***[SRST_ON_POWERDOMAIN]***.CG_PU and ***[SRST_OFF_POWERDOMAIN]***.CG_PU.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 03AC		
Physical address View0	0x4000 03AC		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:5	Reserved	—	—	—
4	SRST_asyncrst_usb2fs_usbrstn	USB USB reset	RW oneToSet	0
3	SRST_asyncrst_usb2fs_hrstn	USB AHB I/F reset	RW oneToSet	0
2	SRST_asyncrst_h2hupu_hrstn	H2HSYNCUPU reset	RW oneToSet	0
1	Reserved	—	—	—
0	SRST_asyncrst_h2hdnu_hrstn	H2HSYNCDNU reset	RW oneToSet	0

5.58. SRST_OFF_PA12

SRST_OFF_PA12			
Description	Soft reset OFF (PA12) [Write]1: Reset deassert. 0: Ignored. [Read]1: Reset deassert in progress. 0: Reset assert in progress * Also changed by writing to ***[SRST_ON_POWERDOMAIN]***.CG_PA12 and ***[SRST_OFF_POWERDOMAIN]***.CG_PA12.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 03B4		
Physical address View0	0x4000 03B4		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:2	Reserved	—	—	—
1	SRST_asyncrst_adcc12_adcrstn	ADCC12 ADC reset	RW oneToSet	0
0	SRST_asyncrst_adcc12_prstn	ADCC12 APB I/F reset	RW oneToSet	0

5.59. SRST_OFF_PA24

SRST_OFF_PA24			
Description	Soft reset OFF (PA24) [Write]1: Reset deassert. 0: Ignored. [Read]1: Reset deassert in progress. 0: Reset assert in progress * Also changed by writing to ***[SRST_ON_POWERDOMAIN]***.CG_PA24 and ***[SRST_OFF_POWERDOMAIN]***.CG_PA24.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 03B8		
Physical address View0	0x4000 03B8		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:2	Reserved	—	—	—
1	SRST_asyncrst_adcc24_adcrstn	ADCC24 ADC reset	RW oneToSet	0
0	SRST_asyncrst_adcc24_prstn	ADCC24 APB I/F reset	RW oneToSet	0

5.60. SRST_OFF_PP1

SRST_OFF_PP1			
Description	Soft reset OFF (PP1) [Write]1: Reset deassert. 0: Ignored. [Read]1: Reset deassert in progress. 0: Reset assert in progress * Also changed by writing to ***[SRST_ON_POWERDOMAIN]***.CG_PP1 and ***[SRST_OFF_POWERDOMAIN]***.CG_PP1.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 03BC		
Physical address View0	0x4000 03BC		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:16	Reserved	—	—	—
15	SRST_asyncrst_uart1_srstn	UART1 serial reset.	RW oneToSet	0
14	SRST_asyncrst_uart1_prstn	UART1 APB I/F reset	RW oneToSet	0
13	SRST_asyncrst_uart0_srstn	UART0 serial reset.	RW oneToSet	0
12	SRST_asyncrst_uart0_prstn	UART0 APB I/F reset	RW oneToSet	0
11	SRST_asyncrst_spim1_srstn	SPIM1 serial reset	RW oneToSet	0
10	SRST_asyncrst_spim1_prstn	SPIM1 APB I/F reset	RW oneToSet	0
9	SRST_asyncrst_spim0_srstn	SPIM0 serial reset	RW oneToSet	0
8	SRST_asyncrst_spim0_prstn	SPIM0 APB I/F reset	RW oneToSet	0
7	SRST_asyncrst_i2c1_srstn	I2C1 serial reset	RW oneToSet	0
6	SRST_asyncrst_i2c1_prstn	I2C1 APB I/F reset	RW oneToSet	0
5	SRST_asyncrst_i2c0_srstn	I2C0 serial reset	RW oneToSet	0
4	SRST_asyncrst_i2c0_prstn	I2C0 APB I/F reset	RW oneToSet	0
3:1	Reserved	—	—	—
0	SRST_asyncrst_h2pp1_hrstn	H2APBP1 reset	RW oneToSet	0

5.61. CTRL_MODETRAN

CTRL_MODETRAN			
Description	PowerMode Control for #E36		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0400		
Physical address View0	0x4000 0400		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:1	Reserved	—	—	—
0	CTRL_MODETRAN	0: ES2.1 and before 1: ES2.2 and after * This register is valid after ES2.2. * It is prohibited to set one until ES2.1 and must apply the workaround(refer to errata #E36).	RW modify	0

5.62. CSM_MAIN

CSM_MAIN			
Description	Clock source setting (CD_MPIER/CD_PPIER0/CD_PPIER1/CD_PPIER2/CD_SPIC/CD_USBB)		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0404		
Physical address View0	0x4000 0404		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:3	Reserved	—	—	—
2:0	CSMSEL_MAIN	000: SIOSC4M 001: OSC12M 010: PLL 011: ADPLL 100: OSC32K/SIOSC32K 101: ignored 110: ignored 111: ignored * OSC32K and SIOSC32K are switched with ***[CSM_RTC]***. * The initial value is determined with a value stored in EFUSE.	RW modify	0x0

5.63. CSM_CPUTRC

CSM_CPUTRC			
Description	Clock source setting (CD_CPUTRC)		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0408		
Physical address View0	0x4000 0408		
Physical address View1	—		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	—	—	—
0	CSMSEL_CPUTRC	0: SIOSC4M 1: OSC12M	RW modify	0

5.64. CSM_CPUST

CSM_CPUST			
Description	Clock source setting (CD_CPUST)		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 040C		
Physical address View0	0x4000 040C		
Physical address View1	—		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:3	Reserved	—	—	—
2:0	CSMSEL_CPUST	000: SIOSC4M 001: OSC12M 010: ignored 011: ignored 100: OSC32K/SIOSC32K 101: ignored 110: ignored 111: ignored * OSC32K and SIOSC32K are switched with ***[CSM_RTC]***.	RW modify	0x0

5.65. CSM_USBI

CSM_USBI			
Description	Clock source setting (CD USBI)		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0410		
Physical address View0	0x4000 0410		
Physical address View1	—		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	—	—	—
0	CSMSEL_USBI	0: PLL 1: ADPLL	RW modify	0

5.66. CSM_UART0

CSM_UART0			
Description	Clock source setting (CD UART0)		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0414		
Physical address View0	0x4000 0414		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:3	Reserved	—	—	—
2:0	CSMSEL_UART0	000: SIOSC4M 001: OSC12M 010: PLL 011: ADPLL 100: OSC32K/SIOSC32K 101: ignored 110: ignored 111: ignored * OSC32K and SIOSC32K are switched with ***[CSM_RTC]***.	RW modify	0x0

5.67. CSM_UART1

CSM_UART1			
Description	Clock source setting (CD UART1)		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0418		
Physical address View0	0x4000 0418		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:3	Reserved	—	—	—
2:0	CSMSEL_UART1	000: SIOSC4M 001: OSC12M 010: PLL 011: ADPLL 100: OSC32K/SIOSC32K 101: ignored 110: ignored 111: ignored * OSC32K and SIOSC32K are switched with ***[CSM_RTC]***.	RW modify	0x0

5.68. CSM_UART2

CSM_UART2					
Description	Clock source setting (CD UART2)				
Address Region	pmulv		**Type:**	RW	
Offset	0x0000 041C				
Physical address View0	0x4000 041C				
Physical address View1	—				
Bitfield Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:3	Reserved	—		—	—
2:0	CSMSEL_UART2	000: SIOSC4M 001: OSC12M 010: PLL 011: ADPLL 100: OSC32K/SIOSC32K 101: ignored 110: ignored 111: ignored * OSC32K and SIOSC32K are switched with ***[CSM_RTC]***.		RW modify	0x0

5.69. CSM_ADCC12A

CSM_ADCC12A					
Description	Clock source setting (CD ADCC12)				
Address Region	pmulv		**Type:**	RW	
Offset	0x0000 0420				
Physical address View0	0x4000 0420				
Physical address View1	—				
Bitfield Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:3	Reserved	—		—	—
2:0	CSMSEL_ADCC12A	000: SIOSC4M 001: OSC12M 010: PLL 011: ADPLL 100: ignored 101: 1/3 frequency division of OSC12M 110: 1/3 frequency division of PLL 111: 1/9 frequency division of PLL * If the value is 0b101 to 111, set 0x1 to ***[PRESCAL_ADCC12A]***.		RW modify	0x0

5.70. CSM_ADCC24A

CSM_ADCC24A			
Description	Clock source setting (CD ADCC24)		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0424		
Physical address View0	0x4000 0424		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:3	Reserved	—	—	—
2:0	CSMSEL_ADCC24A	000: SIOSC4M 001: OSC12M 010: PLL 011: ADPLL 100: ignored 101: 1/3 frequency division of OSC12M 110: ignored 111: 1/9 frequency division of PLL * If the value is 0b101 or 0b111, set 0x1 to ***[PRESCAL_ADCC24A]***.	RW modify	0x0

5.71. PRESCAL_MAIN

PRESCAL_MAIN			
Description	Prescaler setting (CD_MPIER/CD_PPIER0/CD_PPIER1/CD_PPIER2/CD_SPIC/CD_USBB) 0x0: Stop 0x1: 1/1 frequency division 0x2: 1/2 frequency division 0x3: 1/3 frequency division 0x4: 1/4 frequency division 0x5: 1/5 frequency division 0x6: 1/6 frequency division 0x7: 1/7 frequency division 0x8: 1/8 frequency division 0x9: 1/9 frequency division 0xA: 1/10 frequency division 0xB: 1/12 frequency division 0xC: 1/18 frequency division 0xD: 1/24 frequency division 0xE: 1/36 frequency division 0xF: 1/48 frequency division		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0484		
Physical address View0	0x4000 0484		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:24	Reserved	—	—	—
23:20	PSSEL_CD_PPIER2	CD_PPIER2 * The frequency is divided for the clock selected with CSM_MAIN. * Frequency=fCSM_MAIN/(DIVPSSEL_C	RW modify	0x0

		D_MPIER * DIVPSSEL_CD_PPIER2)		
19:16	PSSEL_CD_PPIER1	CD_PPIER1 * The frequency is divided for the clock selected with CSM_MAIN. * Frequency=fCSM_MAIN/(DIVPSSEL_CD_MPIER * DIVPSSEL_CD_PPIER1)	RW modify	0x0
15:12	PSSEL_CD_PPIER0	CD_PPIER0 * The frequency is divided for the clock selected with CSM_MAIN. * Frequency=fCSM_MAIN/(DIVPSSEL_CD_MPIER * DIVPSSEL_CD_PPIER0)	RW modify	0x0
11:8	PSSEL_CD_USBB	CD_USBB * The frequency is divided for the clock selected with CSM_MAIN. * Frequency=fCSM_MAIN/(DIVPSSEL_CD_MPIER * DIVPSSEL_CD_USBB)	RW modify	0x0
7:4	PSSEL_CD_SPIC	CD_SPIC * The frequency is divided for the clock selected with CSM_MAIN. * Frequency=fCSM_MAIN/DIVPSSEL_CD_SPIC	RW modify	0x1
3:0	PSSEL_CD_MPIER	CD_MPIER * 0x0: Setting prohibited	RW modify	0x1

5.72. PRESCAL_CPUST

PRESCAL_CPUST			
Description	Prescaler setting (CD_CPUST) 0x0: Stop 0x1: 1/1 frequency division 0x2: 1/2 frequency division 0x3: 1/3 frequency division 0x4: 1/4 frequency division 0x5: 1/5 frequency division 0x6: 1/6 frequency division 0x7: 1/7 frequency division 0x8: 1/8 frequency division 0x9: 1/9 frequency division 0xA: 1/10 frequency division 0xB: 1/12 frequency division 0xC: 1/18 frequency division 0xD: 1/24 frequency division 0xE: 1/36 frequency division 0xF: 1/48 frequency division		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 048C		
Physical address View0	0x4000 048C		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:4	Reserved	—	—	—
3:0	PSSEL_CD_CPUST	CD_CPUST	RW modify	0x1

5.73. PRESCAL_USBI

PRESCAL_USBI			
Description	Prescaler setting (CD_USBI) 0x0: Stop 0x1: 1/1 frequency division 0x2: 1/2 frequency division 0x3: 1/3 frequency division 0x4: 1/4 frequency division 0x5: 1/5 frequency division 0x6: 1/6 frequency division 0x7: 1/7 frequency division 0x8: 1/8 frequency division 0x9: 1/9 frequency division 0xA: 1/10 frequency division 0xB: 1/12 frequency division 0xC: 1/18 frequency division 0xD: 1/24 frequency division 0xE: 1/36 frequency division 0xF: 1/48 frequency division		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0490		
Physical address View0	0x4000 0490		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:4	Reserved	—	—	—
3:0	PSSEL_CD_USBI	CD_USBI	RW modify	0x0

5.74. PRESCAL_UART0

PRESCAL_UART0			
Description	Prescaler setting (CD_UART0) 0x0: Stop 0x1: 1/1 frequency division 0x2: 1/2 frequency division 0x3: 1/3 frequency division 0x4: 1/4 frequency division 0x5: 1/5 frequency division 0x6: 1/6 frequency division 0x7: 1/7 frequency division 0x8: 1/8 frequency division 0x9: 1/9 frequency division 0xA: 1/10 frequency division 0xB: 1/12 frequency division 0xC: 1/18 frequency division 0xD: 1/24 frequency division 0xE: 1/36 frequency division 0xF: 1/48 frequency division		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0494		
Physical address View0	0x4000 0494		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:4	Reserved	—	—	—
3:0	PSSEL_CD_UART0	CD_UART0	RW modify	0x0

5.75. PRESCAL_UART1

PRESCAL_UART1			
Description	Prescaler setting (CD_UART1) 0x0: Stop 0x1: 1/1 frequency division 0x2: 1/2 frequency division 0x3: 1/3 frequency division 0x4: 1/4 frequency division 0x5: 1/5 frequency division 0x6: 1/6 frequency division 0x7: 1/7 frequency division 0x8: 1/8 frequency division 0x9: 1/9 frequency division 0xA: 1/10 frequency division 0xB: 1/12 frequency division 0xC: 1/18 frequency division 0xD: 1/24 frequency division 0xE: 1/36 frequency division 0xF: 1/48 frequency division		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0498		
Physical address View0	0x4000 0498		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:4	Reserved	—	—	—
3:0	PSSEL_CD_UART1	CD_UART1	RW modify	0x0

5.76. PRESCAL_UART2

PRESCAL_UART2			
Description	Prescaler setting (CD_UART2) 0x0: Stop 0x1: 1/1 frequency division 0x2: 1/2 frequency division 0x3: 1/3 frequency division 0x4: 1/4 frequency division 0x5: 1/5 frequency division 0x6: 1/6 frequency division 0x7: 1/7 frequency division 0x8: 1/8 frequency division 0x9: 1/9 frequency division 0xA: 1/10 frequency division 0xB: 1/12 frequency division 0xC: 1/18 frequency division 0xD: 1/24 frequency division 0xE: 1/36 frequency division 0xF: 1/48 frequency division		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 049C		
Physical address View0	0x4000 049C		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:4	Reserved	—	—	—
3:0	PSSEL_CD_UART2	CD_UART2	RW modify	0x0

5.77. PRESCAL_ADCC12A

PRESCAL_ADCC12A			
Description	Prescaler setting (CD_ADCC12A) 0x0: Stop 0x1: 1/1 frequency division 0x2: 1/2 frequency division 0x3: reserved 0x4: 1/4 frequency division 0x5: reserved 0x6: 1/6 frequency division 0x7: reserved 0x8: 1/8 frequency division 0x9: reserved 0xA: 1/10 frequency division 0xB: 1/12 frequency division 0xC: 1/18 frequency division 0xD: 1/24 frequency division 0xE: 1/36 frequency division 0xF: 1/48 frequency division * With ***[CSM_ADCC12A]***=0b101 to 111, use the setting of "0x1: 1/1 frequency division".		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 04A0		
Physical address View0	0x4000 04A0		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:4	Reserved	—	—	—
3:0	PSSEL_CD_ADCC12A	CD_ADCC12A	RW modify	0x0

5.78. PRESCAL_ADCC24A

PRESCAL_ADCC24A			
Description	Prescaler setting (CD_ADCC24A) 0x0: Stop 0x1: 1/1 frequency division 0x2: 1/2 frequency division 0x3: reserved 0x4: 1/4 frequency division 0x5: reserved 0x6: 1/6 frequency division 0x7: reserved 0x8: 1/8 frequency division 0x9: reserved 0xA: 1/10 frequency division 0xB: 1/12 frequency division 0xC: 1/18 frequency division 0xD: 1/24 frequency division 0xE: 1/36 frequency division 0xF: 1/48 frequency division * With ***[CSM_ADCC24A]***=0b101 or 0b111, use the setting of "0x1: 1/1 frequency division".		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 04A4		
Physical address View0	0x4000 04A4		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:4	Reserved	—	—	—
3:0	PSSEL_CD_ADCC24A	CD_ADCC24A	RW modify	0x0

5.79. CONFIG_OSC12M

CONFIG_OSC12M			
Description	OSC12M control		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0500		
Physical address View0	0x4000 0500		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:2	Reserved	—	—	—
1	Reserved	—	—	—
0	OSC12M_EN	Enable control 0: Stops OSC. 1: Starts OSC. * The initial value is determined with a value stored in EFUSE.	RW modify	0

5.80. CONFIG_PLL_0

CONFIG_PLL_0					
Description	PLL control				
Address Region	pmulv		**Type:**	RW	
Offset	0x0000 0508				
Physical address View0	0x4000 0508				
Physical address View1	—				
Bitfield Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31	PLL_SWEN	SW control enable 0: Any terminals of PLL other than BP cannot be controlled from SW. 1: All terminals of PLL can be controlled from SW.		RW modify	0
30:1	Reserved	—		—	—
0	PLL_BP	Sets the bypass mode. 0: Normal mode 1: Bypass mode * Can be controlled from SW regardless of the value of ***[CONFIG_PLL_0]***.PLL_SWEN. * The initial value is determined with a value stored in EFUSE.		RW modify	1

5.81. CONFIG_PLL_1

CONFIG_PLL_1					
Description	PLL control Multiplication setting 0x00000093：x4(OSC12M × 4=48MHz) 0x00000092：x3(OSC12M × 3=36MHz) 0x00000091：x2(OSC12M × 2=24MHz)				
Address Region	pmulv		**Type:**	RW	
Offset	0x0000 050C				
Physical address View0	0x4000 050C				
Physical address View1	—				
Bitfield Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:0	PLL_ND	multipilication setting		RW modify	0x3

5.82. CONFIG_ADPLL_0

CONFIG_ADPLL_0			
Description	ADPLL control		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0510		
Physical address View0	0x4000 0510		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:16	Reserved	—	—	—
15:12	Reserved	—	—	—
11:4	Reserved	—	—	—
3	Reserved	—	—	—
2	Reserved	—	—	—
1	Reserved	—	—	—
0	ADPLL_ENPLL	Operation control 0: Disable 1: Enable	RW modify	0

5.83. CONFIG_ADPLL_1

CONFIG_ADPLL_1			
Description	ADPLL control		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0514		
Physical address View0	0x4000 0514		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:14	Reserved	—	—	—
13:4	ADPLL_NTWIN	Normalized Tuning Word input	RO	0x000
3	Reserved	—	—	—
2	ADPLL_NTWOUT_LATEN	Normalized Tuning Word output latch enable control 0: Disable 1: Enable	RW modify	0
1	Reserved	—	—	—
0	ADPLL_NTWMODE	Sets the Normalized Tuning Word mode. 0: Disable (Internal Mode) 1: Enable (External Mode)	RW modify	0

5.84. CONFIG_DCDC_LVREG_1

CONFIG_DCDC_LVREG_1			
Description	DCDC control		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0528		
Physical address View0	0x4000 0528		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31	Reserved	—	—	—
30:28	Reserved	—	—	—
27	Reserved	—	—	—
26:24	Reserved	—	—	—
23:22	Reserved	—	—	—
21:20	Reserved	—	—	—
19	Reserved	—	—	—
18	DCDC_SSFAST	Soft start control 0: Enable (slow) 1: Disable (fast)	RW modify	0
17	Reserved	—	—	—
16	Reserved	—	—	—
15:13	Reserved	—	—	—
12	Reserved	—	—	—
11:10	Reserved	—	—	—
9:8	Reserved	—	—	—
7:4	Reserved	—	—	—
3	Reserved	—	—	—
2:0	Reserved	—	—	—

5.85. CONFIG_LDOF_0

CONFIG_LDOF_0			
Description	LDOF control		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0530		
Physical address View0	0x4000 0530		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:18	Reserved	—	—	—
17:16	Reserved	—	—	—
15:2	Reserved	—	—	—
1	LDOF_POWERGOODM	Low voltage detection 0: Low voltage 1: Proper voltage * 0 -> 1 in the reset release sequence	RO	1
0	LDOF_STANDBYMX	Enable control 0: Power down 1: Operation * 0 -> 1 in the reset release sequence	RW modify	1

5.86. OVERRIDE_EFUSE_OSC12M

OVERRIDE_EFUSE_OSC12M			
Description	OSC12M control * With ***[SELECT_EFUSE]***.SEL_EFUSE_OSC12M=0, EFUSE data is reloaded with write access. With ***[SELECT_EFUSE]***.SEL_EFUSE_OSC12M=1, write data is applied. * The initial value is determined with a value stored in EFUSE.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0580		
Physical address View0	0x4000 0580		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:4	Reserved	—	—	—
3:0	OVERRIDE_EFUSE_OSC12M_MAIN_GM	XO_Main GM adjustment 0000: Mode0(recommended) 0001: Mode1 0011: Mode2 0111: Mode3 *The setting value other than above is prohibited. *The setting value will be changed from 0b0111 to 0b0000 by boot sequencer.	RW modify	0x7

5.87. SELECT_EFUSE

SELECT_EFUSE			
Description	Selects data to be stored in the OVERRIDE register. 0: EFUSE data 1: Write data		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 05C0		
Physical address View0	0x4000 05C0		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:13	Reserved	—	—	—
12	SEL_EFUSE_SiOSC4M	SIOSC4M * Control of ***[OVERRIDE_EFUSE_SiOSC4M]***	RW modify	0
11	SEL_EFUSE_SiOSC32K	SIOSC32K * Control of ***[OVERRIDE_EFUSE_SiOSC32K]***	RW modify	0
10	SEL_EFUSE_OSC32K	OSC32K * Control of ***[OVERRIDE_EFUSE_OSC32K]***	RW modify	0
9	Reserved	—	—	—
8	Reserved	—	—	—
7	Reserved	—	—	—
6	Reserved	—	—	—
5	SEL_EFUSE_BGR	BGR * Control of ***[OVERRIDE_EFUSE_BGR_0]***,	RW modify	0

		[OVERRIDE_EFUSE_BGR_1]		
4	Reserved	—	—	—
3	Reserved	—	—	—
2	Reserved	—	—	—
1	Reserved	—	—	—
0	SEL_EFUSE_OSC12M	OSC12M * Control of ***[OVERRIDE_EFUSE_OSC12M]***	RW modify	0

5.88. EFUSE_REVISIONID

EFUSE_REVISIONID			
Description	REVISIONID * The initial value is determined with a value stored in EFUSE.		
Address Region	pmulv	**Type:**	RO
Offset	0x0000 05DC		
Physical address View0	0x4000 05DC		
Physical address View1	—		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:0	EFUSE_REVISIONID	[31:28]: Reserved [27:24]: ID for geomagnetic sensor(revision ID for the mounted geomagnetic sensor chip) 0000: not mounted 0001: geomagnetic sensor identification1 0010: geomagnetic sensor identification2 [23:20]: ID for gyro sensor(revision ID for the mounted gyro sensor chip) 0000: not mounted 0001: gyro sensor identification1 0010: gyro sensor identification2 [19:16]: ID for acceleration sensor(revision ID for the mounted acceleration sensor chip) 0000: not mounted 0001: acceleration sensor identification1(ES) 0010: acceleration sensor identification2(CS) [15:12]: BLE ID(revision ID for the mounted BLE chip) 0000: not mounted 0001: BLE identification1(ROM2) 0010: BLE identification2(#3 ROM4) 0011: BLE identification3(#3 ROM5) [11:8]: FLASH ID(revision ID for the mounted FLASH chip) 0000: not mounted 0001: FLASH identification1 0010: FLASH identification2 [7:4]: MCU Major ID(for example, when the function update) 0000:ES1.0/ES1.1 0001:ES2.0 [3:0]: MCU Minor ID(for example, bug	RO	—

		fix) *TZ1001/TWVM1000 ES2.0a will be 32'h00023110. *TZ1001/TWVM1000 ES2.1 will be 32'h00023111. *TZ1001/TWVM1000 ES2.2 will be 32'h00023112. *TZ1011 ES2.2 will be 32'h01883112. *TZ1021 ES2.1 will be 32'h00000111. *TZ1021 ES2.2 will be 32'h00000112. *TZ1031 ES2.2 will be 32'h00883112.		

5.89. EFUSE_BOOTSEQ

EFUSE_BOOTSEQ				
Description	BOOTSEQ * The initial value is determined with a value stored in EFUSE.			
Address Region	pmulv	**Type:**	RO	
Offset	0x0000 05E0			
Physical address View0	0x4000 05E0			
Physical address View1	—			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:9	Reserved	—	—	—
8	Reserved	—	—	—
7:6	Reserved	—	—	—
5:4	EFUSE_SEL_CSM_MAIN	Selects CSM_MAIN at CPU start. 00: PLL 01: OSC12M other: SIOSC4M	RO	—
3:1	Reserved	—	—	—
0	EFUSE_SEL_FLASH	FLASH selection 0: winbond 1: macronics	RO	—

5.90. EFUSE_SIOSC4M

EFUSE_SiOSC4M				
Description	SiOS4M Oscillation frequency adjustment * The initial value is determined with a value stored in EFUSE.			
Address Region	pmulv	**Type:**	RO	
Offset	0x0000 05E4			
Physical address View0	0x4000 05E4			
Physical address View1	—			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:24	EFUSE_SiOSC4M_CTRIM_MODED	Mode D (0.9 V)	RO	—
23:16	EFUSE_SiOSC4M_CTRIM_M	Mode C (1.0 V)	RO	—

	ODEC			
15:8	EFUSE_SiOSC4M_CTRIM_MODEB	Mode B (1.1 V)	RO	—
7:0	EFUSE_SiOSC4M_CTRIM_MODEA	Mode A (1.2 V)	RO	—

5.91. BROWNOUTRESET

BROWNOUTRESET			
Description	Brownout soft reset * Used together with the Brownout interrupt. The Brownout reset can be made by writing 1 to this register after a CPU interrupt.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0600		
Physical address View0	0x4000 0600		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:1	Reserved	—	—	—
0	BOR	[Write]1: Assert. 0: Ignored. [Read]1: Assert. 0: Deassert	RW oneToSet	0

5.92. MOVE_VOLTAGE_START

MOVE_VOLTAGE_START			
Description	Voltage Mode transition setting		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0700		
Physical address View0	0x4000 0700		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:4	Reserved	—	—	—
3:2	VMSTATUS	Voltage Mode status 00: Mode A (1.2 V) 01: Mode B (1.1 V) 10: Mode C (1.0 V) 11: Mode D (0.9 V)	RO	0x0
1	Reserved	—	—	—
0	START	Starts Voltage Mode transition. [Write]1: Start. 0: Ignored. [Read]1: Transition in progress. 0: Stop	RW oneToSet	0

5.93. MOVE_POWER_VOLTAGE_MODE

MOVE_POWER_VOLTAGE_MODE			
Description	Power/Voltage Mode transition setting		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0704		
Physical address View0	0x4000 0704		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:9	Reserved	—	—	—
8	FAST_MODE	High-speed return mode (only WAIT/WAIT-RETENTION/RETENTION) 0: Normal return mode Returns to Voltage Mode used before transition. 1: High-speed return mode ModeD is started up at return. So, a higher speed return is made because the mode is not returned to Voltage Mode before transition.	RW modify	0
7:4	POWER_MODE	Sets a Power Mode transition destination. 0000: ACTIVE (Voltage Mode transition) 0001: SLEEP0 0010: SLEEP1 0011: SLEEP2 0100: WAIT 0101: WAIT-RETENTION 0110: reserved 0111: RETENTION 1000: RTC 1001: STOP other: reserved	RW modify	0x0
3:2	Reserved	—	—	—
1:0	VOLTAGE_MODE	Sets a Voltage Mode transition destination. 00: Mode A (1.2 V) 01: Mode B (1.1 V) 10: Mode C (1.0 V) 11: Mode D (0.9 V)	RW modify	0x0

5.94. POWERDOMAIN_CTRL

POWERDOMAIN_CTRL			
Description	Starts power supply domain control. [Write]1: Start. 0: Ignored. [Read]1: Transition in progress. 0: Stop * The power supply domain cannot be controlled for PM with SW.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0710		
Physical address View0	0x4000 0710		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:12	Reserved	—	—	—
11	START_PP1	For PP1 power supply domain control	RW modify	0
10	START_PA24	For PA24 power supply domain control	RW modify	0
9	START_PA12	For PA12 power supply domain control	RW modify	0
8	Reserved	—	—	—
7	START_PD	For PD power supply domain control	RW modify	0
6	START_PC	For PC power supply domain control	RW modify	0
5	START_PF	For PF power supply domain control	RW modify	0
4	START_PS2	For PS2 power supply domain control	RW modify	0
3	START_PS1	For PS1 power supply domain control	RW modify	0
2	START_PS0	For PS0 power supply domain control	RW modify	0
1	START_PE	For PE power supply domain control	RW modify	0
0	Reserved	—	—	—

5.95. POWERDOMAIN_CTRL_MODE

POWERDOMAIN_CTRL_MODE			
Description	Sets a power supply domain control transition destination. 00: Power On 01: Power Off 10: RETENTION 11: WAIT (only PS0, PS1, and PS2 settable)		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0714		
Physical address View0	0x4000 0714		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:24	Reserved	—	—	—
23:22	PDMODE_PP1	For PP1 power supply domain control	RW modify	0x0

21:20	PDMODE_PA24	For PA24 power supply domain control	RW modify	0x1
19:18	PDMODE_PA12	For PA12 power supply domain control	RW modify	0x1
17:16	Reserved	—	—	—
15:14	PDMODE_PD	For PD power supply domain control	RW modify	0x1
13:12	PDMODE_PC	For PC power supply domain control	RW modify	0x0
11:10	PDMODE_PF	For PF power supply domain control	RW modify	0x0
9:8	PDMODE_PS2	For PS2 power supply domain control	RW modify	0x0
7:6	PDMODE_PS1	For PS1 power supply domain control	RW modify	0x0
5:4	PDMODE_PS0	For PS0 power supply domain control	RW modify	0x0
3:2	PDMODE_PE	For PE power supply domain control	RW modify	0x1
1:0	Reserved	—	—	—

5.96. POWERDOMAIN_CTRL_STATUS

POWERDOMAIN_CTRL_STATUS			
Description	Power supply domain control status 00: Power On 01: Power Off 10: RETENTION 11: WAIT (only PS0, PS1, and PS2 used)		
Address Region	pmulv	**Type:**	RO
Offset	0x0000 0718		
Physical address View0	0x4000 0718		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:24	Reserved	—	—	—
23:22	PDSTATUS_PP1	For PP1 power supply domain control	RO	0x0
21:20	PDSTATUS_PA24	For PA24 power supply domain control	RO	0x1
19:18	PDSTATUS_PA12	For PA12 power supply domain control	RO	0x1
17:16	Reserved	—	—	—
15:14	PDSTATUS_PD	For PD power supply domain control	RO	0x1
13:12	PDSTATUS_PC	For PC power supply domain control	RO	0x0
11:10	PDSTATUS_PF	For PF power supply domain control	RO	0x0
9:8	PDSTATUS_PS2	For PS2 power supply domain control	RO	0x0
7:6	PDSTATUS_PS1	For PS1 power supply domain control	RO	0x0
5:4	PDSTATUS_PS0	For PS0 power supply domain control	RO	0x0
3:2	PDSTATUS_PE	For PE power supply domain control	RO	0x1
1:0	Reserved	—	—	—

5.97. POWERDOMAIN_CTRL_MODE_FOR_WAIT

POWERDOMAIN_CTRL_MODE_FOR_WAIT			
Description	Sets a power supply domain control transition destination in WAIT mode. 00: Power On 01: Power Off 10: Setting prohibited 11: WAIT (only PS0, PS1, and PS2 used)		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0720		
Physical address View0	0x4000 0720		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:10	Reserved	—	—	—
9:8	PDMODE_FOR_WAIT_PS2	For PS2 power supply domain control	RW modify	0x3
7:6	PDMODE_FOR_WAIT_PS1	For PS1 power supply domain control	RW modify	0x3
5:4	PDMODE_FOR_WAIT_PS0	For PS0 power supply domain control	RW modify	0x3
3:0	Reserved	—	—	—

5.98. POWERDOMAIN_CTRL_MODE_FOR_WRET

POWERDOMAIN_CTRL_MODE_FOR_WRET			
Description	Sets a power supply domain control transition destination in WAIT-RETENTION mode. 00: Power On 01: Power Off (PC unsettable) 10: RETENTION (PS0, PS1, and PS2 unsettable) 11: WAIT (only PS0, PS1, and PS2 used)		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0724		
Physical address View0	0x4000 0724		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:24	Reserved	—	—	—
23:22	PDMODE_FOR_WRET_PP1	For PP1 power supply domain control	RW modify	0x2
21:20	PDMODE_FOR_WRET_PA24	For PA24 power supply domain control	RW modify	0x2
19:18	PDMODE_FOR_WRET_PA12	For PA12 power supply domain control	RW modify	0x2
17:16	Reserved	—	—	—
15:14	PDMODE_FOR_WRET_PD	For PD power supply domain control	RW modify	0x2
13:12	PDMODE_FOR_WRET_PC	For PC power supply domain control	RW modify	0x2
11:10	PDMODE_FOR_WRET_PF	For PF power supply domain control	RW modify	0x2
9:8	PDMODE_FOR_WRET_PS2	For PS2 power supply domain control	RW modify	0x3
7:6	PDMODE_FOR_WRET_PS1	For PS1 power supply domain control	RW	0x3

			modify	
5:4	PDMODE_FOR_WRET_PS0	For PS0 power supply domain control	RW modify	0x3
3:2	PDMODE_FOR_WRET_PE	For PE power supply domain control	RW modify	0x2
1:0	Reserved	—	—	—

5.99. POWERDOMAIN_CTRL_MODE_FOR_RET

POWERDOMAIN_CTRL_MODE_FOR_RET			
Description	Sets a power supply domain control transition destination in RETENTION mode. 00: Setting prohibited 01: Power Off(PC unsettable) 10: RETENTION 11: Setting prohibited		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0728		
Physical address View0	0x4000 0728		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:24	Reserved	—	—	—
23:22	PDMODE_FOR_RET_PP1	For PP1 power supply domain control	RW modify	0x2
21:20	PDMODE_FOR_RET_PA24	For PA24 power supply domain control	RW modify	0x2
19:18	PDMODE_FOR_RET_PA12	For PA12 power supply domain control	RW modify	0x2
17:16	Reserved	—	—	—
15:14	PDMODE_FOR_RET_PD	For PD power supply domain control	RW modify	0x2
13:12	PDMODE_FOR_RET_PC	For PC power supply domain control	RW modify	0x2
11:10	PDMODE_FOR_RET_PF	For PF power supply domain control	RW modify	0x2
9:8	PDMODE_FOR_RET_PS2	For PS2 power supply domain control	RW modify	0x2
7:6	PDMODE_FOR_RET_PS1	For PS1 power supply domain control	RW modify	0x2
5:4	PDMODE_FOR_RET_PS0	For PS0 power supply domain control	RW modify	0x2
3:2	PDMODE_FOR_RET_PE	For PE power supply domain control	RW modify	0x2
1:0	Reserved	—	—	—

5.100. VOLTAGEMODE_SETTING

VOLTAGEMODE_SETTING			
Description	Voltage Mode setting		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0730		
Physical address View0	0x4000 0730		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:4	Reserved	—	—	—
3	VOLTAGESOURCE_MODED	0: LDOS, 1: LDOM	RW modify	0
2	VOLTAGESOURCE_MODEC	0: DCDC, 1: LDOM	RW modify	0
1	VOLTAGESOURCE_MODEB	0: DCDC, 1: LDOM	RW modify	0
0	VOLTAGESOURCE_MODEA	0: DCDC	RO	0

5.101. WAITTIME_LDOF

WAITTIME_LDOF			
Description	Wait time at LDOF Power On/Off switching 0 µs(0x00) to 630 µs(0x3F) *units of 10 µs		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0740		
Physical address View0	0x4000 0740		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:22	Reserved	—	—	—
21:16	WAITTIME_LDOF_PWOFF	Sets the period from Off control until power to the target is turned off (initial value: 300 µs).	RW modify	0x1E
15:6	Reserved	—	—	—
5:0	WAITTIME_LDOF_PWON	Sets the period from On control until power is stably supplied to the target (initial value: 300 µs).	RW modify	0x1E

5.102. WAITTIME_PSW

WAITTIME_PSW					
Description	Wait time at Internal Power Switch Power On/Off switching (only PS0, PS1, and PS2 used) 1 µs(0x0) to 16 µs(0xf) *units of 1 µs				
Address Region	pmulv		**Type:**	RW	
Offset	0x0000 0744				
Physical address View0	0x4000 0744				
Physical address View1	—				
Bitfield Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:20	Reserved	—		—	—
19:16	WAITTIME_PSW_PWOFF	Sets the period from Off control until power to the target is turned off (initial value: 16 µs)		RW modify	0xF
15:4	Reserved	—		—	—
3:0	WAITTIME_PSW_PWON	Sets the period from On control until power is stably supplied to the target (initial value: 16 µs).		RW modify	0xF

5.103. WAITTIME_DVSCTL

WAITTIME_DVSCTL					
Description	Wait time at power source or voltage switching *units of 1 µs				
Address Region	pmulv		**Type:**	RW	
Offset	0x0000 0748				
Physical address View0	0x4000 0748				
Physical address View1	—				
Bitfield Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:25	Reserved	—		—	—
24:20	WAITTIME_SBSTIME	Wait time until voltage is switched (step time when voltage is increased every 0.1 V) (initial value: 10 µs) 0 µs(0x00) to 31 µs(0x1F) * 0 setting: No step execution * units of 1 µs		RW modify	0x0A
19:17	Reserved	—		—	—
16:8	WAITTIME_CHGTIME	Wait time until the power source is switched (initial value: 30 µs) 0 µs(0x000) to 511 µs(0x1FF) *units of 1 µs		RW modify	0x01E
7:6	Reserved	—		—	—
5:0	WAITTIME_DCDC_tDE	Wait time from a rising edge of DCDC EN_DCDCREF until a rising edge of EN_DCDC (initial value: 30 µs) 0 µs(0x00) to 63 µs(0x3F) * units of 1 µs		RW modify	0x1E

5.104. POWERMODE_SLEEP_CG_ON

POWERMODE_SLEEP_CG_ON			
Description	Block to be subject to clock gating ON addition control in SLEEP mode 0: No clock stop addition control 1: Clock stop addition control available		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0780		
Physical address View0	0x4000 0780		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:30	Reserved	—	—	—
29	SLEEP_CG_ON_cpustclk_cpu_stclk	CPU SYSTICK clock	RW modify	0
28	SLEEP_CG_ON_cputrcclk_cpu_traceclk	CPU trace clock	RW modify	0
27	SLEEP_CG_ON_evm	EVM	RW modify	0
26	SLEEP_CG_ON_rtclv	RTCLV	RW modify	0
25	SLEEP_CG_ON_adcc24	ADCC24	RW modify	0
24	SLEEP_CG_ON_adcc12	ADCC12	RW modify	0
23	SLEEP_CG_ON_gpio3	GPIO3	RW modify	0
22	SLEEP_CG_ON_gpio2	GPIO2	RW modify	0
21	SLEEP_CG_ON_gpio1	GPIO1	RW modify	0
20	SLEEP_CG_ON_gpio0	GPIO0	RW modify	0
19	SLEEP_CG_ON_gconf	GCONF	RW modify	0
18	SLEEP_CG_ON_tmr	TMR	RW modify	0
17	SLEEP_CG_ON_advtmr	ADVTMR	RW modify	0
16	SLEEP_CG_ON_wdt	WDT	RW modify	0
15	SLEEP_CG_ON_spim3	SPIM3	RW modify	0
14	SLEEP_CG_ON_spim2	SPIM2	RW modify	0
13	SLEEP_CG_ON_spim1	SPIM1	RW modify	0
12	SLEEP_CG_ON_spim0	SPIM0	RW modify	0
11	SLEEP_CG_ON_i2c2	I2C2	RW modify	0
10	SLEEP_CG_ON_i2c1	I2C1	RW modify	0
9	SLEEP_CG_ON_i2c0	I2C0	RW modify	0
8	SLEEP_CG_ON_uart2	UART2	RW modify	0
7	SLEEP_CG_ON_uart1	UART1	RW	0

			modify	
6	SLEEP_CG_ON_uart0	UART0	RW modify	0
5	SLEEP_CG_ON_spic	SPIC	RW modify	0
4	SLEEP_CG_ON_sramc	SRAMC	RW modify	0
3	SLEEP_CG_ON_rng	RNG	RW modify	0
2	SLEEP_CG_ON_aesa	AESA	RW modify	0
1	SLEEP_CG_ON_sdmac	SDMAC	RW modify	0
0	SLEEP_CG_ON_mpier	MPIER	RW modify	0

5.105. POWERMODE_SLEEP_PRESCAL

POWERMODE_SLEEP_PRESCAL			
Description	prescaler setting in SLEEP mode		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 0790		
Physical address View0	0x4000 0790		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:1	Reserved	—	—	—
0	SLEEP_PSSEL_mpierclk_cpu_fclk	CPU free-run clock 0: 1/1 frequency division 1: 1/4 frequency division * Only with a mode transition by sleeping. With a mode transition by sleepdeep, CPU free-run clock is stopped. * Frequency=fCSM_MAIN/(DIVPSSEL_CD_MPIER * DIVSLEEP_PSSEL_mpierclk_cpu_fclk)	RW modify	0

5.106. CG_ON_PC_SCRT

CG_ON_PC_SCRT				
Description	Clock gating ON (PC) [Write]1: Clock stops. 0: Ignored. [Read]1: Clock is stopped. 0: Clock is being supplied. * Also changed by writing to ***[CG_ON_POWERDOMAIN_SCRT]***.CG_PC_SCRT and ***[CG_OFF_POWERDOMAIN_SCRT]***.CG_PC_SCRT.			
Address Region	pmulv	**Type:**	RW	
Offset	0x0000 1124			
Physical address View0	0x4000 1124			
Physical address View1	—			

Bitfield Details

Bits	Name	Description	Access	Reset
31:4	Reserved	—	—	—
3	Reserved	—	—	—
2	CG_cputrcclk_cpu_traceclk	CPU trace clock	RW oneToSet	1
1	Reserved	—	—	—
0	Reserved	—	—	—

5.107. CG_OFF_PC_SCRT

CG_OFF_PC_SCRT				
Description	Clock gating OFF (PC) [Write]1: Clock is supplied. 0: Ignored. [Read]1: Clock is being supplied. 0: Clock is stopped. * Also changed by writing to ***[CG_ON_POWERDOMAIN_SCRT]***.CG_PC_SCRT and ***[CG_OFF_POWERDOMAIN_SCRT]***.CG_PC_SCRT.			
Address Region	pmulv	**Type:**	RW	
Offset	0x0000 11A4			
Physical address View0	0x4000 11A4			
Physical address View1	—			

Bitfield Details

Bits	Name	Description	Access	Reset
31:4	Reserved	—	—	—
3	Reserved	—	—	—
2	CG_cputrcclk_cpu_traceclk	CPU trace clock	RW oneToSet	0
1	Reserved	—	—	—
0	Reserved	—	—	—

5.108. CG_ON_PA

CG_ON_PA			
Description	Clock gating ON (PA) [Write]1: Clock stops. 0: Ignored. [Read]1: Clock is stopped. 0: Clock is being supplied.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 2000		
Physical address View0	0x4000 2000		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:17	Reserved	—	—	—
16	CG_CLK32K_OUT	External clock	RW oneToSet	1
15:9	Reserved	—	—	—
8	CG_32KOSC_pmulv	PMULV clock	RW oneToSet	1
7:1	Reserved	—	—	—
0	CG_rtcclk_rtchv_rtcclk	RTCHV clock	RW oneToSet	1

5.109. CG_OFF_PA

CG_OFF_PA			
Description	Clock gating OFF (PA) [Write]1: Clock is supplied. 0: Ignored. [Read]1: Clock is being supplied. 0: Clock is stopped.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 2010		
Physical address View0	0x4000 2010		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:17	Reserved	—	—	—
16	CG_CLK32K_OUT	External clock	RW oneToSet	0
15:9	Reserved	—	—	—
8	CG_32KOSC_pmulv	PMULV clock	RW oneToSet	0
7:1	Reserved	—	—	—
0	CG_rtcclk_rtchv_rtcclk	RTCHV clock	RW oneToSet	0

5.110. SRST_ON_PA

SRST_ON_PA				
Description	Soft reset ON (PA) [Write]1: Reset assert. 0: Ignored. [Read]1: Reset assert in progress. 0: Reset deassert in progress.			
Address Region	pmulv	**Type:**	RW	
Offset	0x0000 2020			
Physical address View0	0x4000 2020			
Physical address View1	—			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	—	—	—
0	SRST_asyncrst_rtchv_rtcrstn	RTCHV reset	RW oneToSet	1

5.111. SRST_OFF_PA

SRST_OFF_PA				
Description	Soft reset OFF (PA) [Write]1: Reset deassert. 0: Ignored. [Read]1: Reset deassert in progress. 0: Reset assert in progress.			
Address Region	pmulv	**Type:**	RW	
Offset	0x0000 2030			
Physical address View0	0x4000 2030			
Physical address View1	—			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	—	—	—
0	SRST_asyncrst_rtchv_rtcrstn	RTCHV reset	RW oneToSet	0

5.112. CSM_RTC

CSM_RTC				
Description	Clock source setting (CD_RTC)			
Address Region	pmulv	**Type:**	RW	
Offset	0x0000 2080			
Physical address View0	0x4000 2080			
Physical address View1	—			
Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	—	—	—
0	CSMSEL_RTC	0: OSC32K 1: SIOSC32K	RW modify	0

5.113. RTCLV_RSYNC_SETTING

RTCLV_RSYNC_SETTING			
Description	RTCLV timer reset selection		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 20C0		
Physical address View0	0x4000 20C0		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:2	Reserved	—	—	—
1:0	RTCLV_RSYNC_SETTING	00: Synchronized to SiOSC4M 01: Synchronized to OSC32K/SIOSC32K (1 cycle) 10: Synchronized to OSC32K/SIOSC32K (2 cycles) 11: reserved * OSC32K and SIOSC32K are switched with ***[CSM_RTC]***.	RW modify	0x0

5.114. CONFIG_OSC32K

CONFIG_OSC32K			
Description	OSC32K control		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 2100		
Physical address View0	0x4000 2100		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:3	Reserved	—	—	—
2	OSC32K_BOOST_DISABLE	High-speed startup disable control 0: High-speed mode enable 1: High-speed mode disable	RW modify	0
1	Reserved	—	—	—
0	OSC32K_EN	Enable control 0: Stops OSC. 1: Starts OSC.	RW modify	0

5.115. CONFIG_SIOSC32K

CONFIG_SiOSC32K			
Description	SIOSC32K control		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 2104		
Physical address View0	0x4000 2104		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:28	Reserved	—	—	—
27:24	Reserved	—	—	—
23:21	Reserved	—	—	—
20:16	Reserved	—	—	—
15:1	Reserved	—	—	—
0	SiOSC32K_EN	Enable control 0: Power down 1: Oscillation	RW modify	0

5.116. CONFIG_SIOSC4M

CONFIG_SiOSC4M			
Description	SIOSC4M control		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 2108		
Physical address View0	0x4000 2108		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:5	Reserved	—	—	—
4	SiOSC4M_CTRIM_LAT	CTRIM latch control 0: Through latch 1: Hold (100ns or more)	RW modify	0
3:1	Reserved	—	—	—
0	Reserved	—	—	—

5.117. CONFIG_DCDC_HVREG

CONFIG_DCDC_HVREG			
Description	DCDC control		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 210C		
Physical address View0	0x4000 210C		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:5	Reserved	—	—	—
4	Reserved	—	—	—
3:2	Reserved	—	—	—

1	DCDC_POWERGOOD	Low voltage detection 0: Low voltage 1: Proper voltage * 0 -> 1 in the power-on sequence	RO	1
0	DCDC_STANDBYX	DCDC enable control 0: Power down 1: Operation * 0 -> 1 in the power-on sequence	RW modify	1

5.118. CONFIG_LVD_0

CONFIG_LVD_0					
Description	LVD control				
Address Region	pmulv		**Type:**	RW	
Offset	0x0000 2118				
Physical address View0	0x4000 2118				
Physical address View1	—				
Bitfield Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:2	Reserved	—		—	—
1	LVD_POWERGOOD	Low voltage detection 0: Low voltage 1: Proper voltage * 0 -> 1 in the power-on sequence		RO	1
0	Reserved	—		—	—

5.119. CONFIG_LDOM_0

CONFIG_LDOM_0					
Description	LDOM control				
Address Region	pmulv		**Type:**	RW	
Offset	0x0000 2120				
Physical address View0	0x4000 2120				
Physical address View1	—				
Bitfield Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:18	Reserved	—		—	—
17:16	Reserved	—		—	—
15:2	Reserved	—		—	—
1	LDOM_POWERGOODM	Low voltage detection 0: Low voltage 1: Proper voltage		RO	0
0	LDOM_STANDBYMX	Enable control 0: Power down 1: Operation		RW modify	0

5.120. CONFIG_LDOM_1

CONFIG_LDOM_1			
Description	LDOM control		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 2124		
Physical address View0	0x4000 2124		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:3	Reserved	—	—	—
2:0	LDOM_SETOUT	Sets output voltage. 0bx00: 1.2 V 0bx01: 1.1 V 0bx10: 1.0 V 0bx11: 0.9 V (x: don't care)	RW modify	0x3

5.121. CONFIG_LDOS_0

CONFIG_LDOS_0			
Description	LDOS control		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 2130		
Physical address View0	0x4000 2130		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:18	Reserved	—	—	—
17:16	Reserved	—	—	—
15:1	Reserved	—	—	—
0	LDOS_STANDBYMX	Enable control 0: Power down 1: Operation	RW modify	0

5.122. CONFIG_LDOS_1

CONFIG_LDOS_1			
Description	LDOS control		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 2134		
Physical address View0	0x4000 2134		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:3	Reserved	—	—	—
2:0	LDOS_SETOUT	Sets output voltage. 000: 1.2 V 001: 1.1 V 010: 1.0 V 011: 0.9 V 1xx: 0.8 V (x: don't care)	RW modify	0x3

5.123. OVERRIDE_EFUSE_OSC32K

OVERRIDE_EFUSE_OSC32K			
Description	OSC32K control * With ***[SELECT_EFUSE]***.SEL_EFUSE_OSC32K=0, EFUSE data is reloaded with write access. With ***[SELECT_EFUSE]***.SEL_EFUSE_OSC32K=1, write data is applied. * The initial value is determined with a value stored in EFUSE.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 2180		
Physical address View0	0x4000 2180		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:20	Reserved	—	—	—
19:16	Reserved	—	—	—
15:13	Reserved	—	—	—
12:8	OVERRIDE_EFUSE_OSC32K_TRIMIN_VREF_GMBIAS	Voltage adjustment bit for Gm constant bias (current switching) 00000: Mode0/Mode3 00001: Mode1 00010: Mode2 00011: Mode4/Mode5/Mode6/Mode7 *The setting value other than above are prohibited	RW modify	0x00
7:5	Reserved	—	—	—
4:0	OVERRIDE_EFUSE_OSC32K_TRIMIN	Adjustment bit (current switching or the like assumed) 00110: Mode0/Mode1/Mode2/Mode4 00111: Mode3/Mode5 01111: Mode6 11111: Mode7 *The setting value other than above are prohibited	RW modify	0x00

5.124. OVERRIDE_EFUSE_SIOSC32K

OVERRIDE_EFUSE_SiOSC32K			
Description	SIOSC32K control * With ***[SELECT_EFUSE]***.SEL_EFUSE_SIOSC32K=0, EFUSE data is reloaded with write access. With ***[SELECT_EFUSE]***.SEL_EFUSE_SIOSC32K=1, write data is applied. * The initial value is determined with a value stored in EFUSE.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 2184		
Physical address View0	0x4000 2184		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:5	Reserved	—	—	—
4:0	OVERRIDE_EFUSE_SiOSC32K_TRIMIN_FREQ	Oscillation frequency adjustment	RW modify	0x00

5.125. OVERRIDE_EFUSE_SIOSC4M

OVERRIDE_EFUSE_SiOSC4M			
Description	SIOSC4M control * With ***[SELECT_EFUSE]***.SEL_EFUSE_SIOSC4M=0, EFUSE data is reloaded with write access. With ***[SELECT_EFUSE]***.SEL_EFUSE_SIOSC4M=1, write data s applied.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 2188		
Physical address View0	0x4000 2188		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:8	Reserved	—	—	—
7:0	OVERRIDE_EFUSE_SiOSC4M_CTRIM	Oscillation frequency adjustment	RW modify	0x00

5.126. OVERRIDE_EFUSE_BGR_0

OVERRIDE_EFUSE_BGR_0			
Description	BGR control * With ***[SELECT_EFUSE]***.SEL_EFUSE_BGR=0, EFUSE data is reloaded with right access. With ***[SELECT_EFUSE]***.SEL_EFUSE_BGR=1, write data is applied. * The initial value is determined with a value stored in EFUSE.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 2190		
Physical address View0	0x4000 2190		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:29	Reserved	—	—	—
28:24	OVERRIDE_EFUSE_BGR_TR	LDOM POWERGOOD output voltage	RW	0x00

	IMIN_PG_LDODM	adjustment	modify	
23:21	Reserved	—	—	—
20:16	OVERRIDE_EFUSE_BGR_TRIMIN_LDODM	LDOM output voltage adjustment	RW modify	0x00
15:13	Reserved	—	—	—
12:8	OVERRIDE_EFUSE_BGR_TRIMIN_PG_LDOF	LDOF POWERGOOD output voltage adjustment	RW modify	0x00
7:5	Reserved	—	—	—
4:0	OVERRIDE_EFUSE_BGR_TRIMIN_LDOF	LDOF output voltage adjustment	RW modify	0x00

5.127. OVERRIDE_EFUSE_BGR_1

OVERRIDE_EFUSE_BGR_1			
Description	BGR control * With ***[SELECT_EFUSE]***.SEL_EFUSE_BGR=0, EFUSE data is reloaded with right access. With ***[SELECT_EFUSE]***.SEL_EFUSE_BGR=1, write data is applied. * The initial value is determined with a value stored in EFUSE.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 2194		
Physical address View0	0x4000 2194		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:21	Reserved	—	—	—
20:16	OVERRIDE_EFUSE_BGR_TRIMIN_TEMP_BGR	BGR temperature characteristic adjustment	RW modify	0x07
15:14	Reserved	—	—	—
13:8	OVERRIDE_EFUSE_BGR_TRIMIN_PG_LVD	LVD POWERGOOD output voltage adjustment	RW modify	0x1F
7:5	Reserved	—	—	—
4:0	OVERRIDE_EFUSE_BGR_TRIMIN_LDODS	LDOS output voltage adjustment	RW modify	0x00

5.128. STATUS_LVPWR

STATUS_LVPWR			
Description	Power Mode status * [8:0]=0x000: ACTIVE mode		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 2200		
Physical address View0	0x4000 2200		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:9	Reserved	—	—	—
8	STATUS_LVPWR_STARTUP	1: STARTUP mode. 0: Others * 1 -> 0 in the reset release sequence	RW modify	0
7	STATUS_LVPWR_STOP	1: STOP mode. 0: Others	RW modify	0
6	STATUS_LVPWR_RTC	1: RTC mode. 0: Others	RW modify	0

5	STATUS_LVPWR_RETENTION	1: RETENTION mode. 0: Others	RW modify	0
4	STATUS_LVPWR_WAIT_RETENTION	1: WAIT-RETENTION mode. 0: Others	RW modify	0
3	STATUS_LVPWR_WAIT	1: WAIT mode. 0: Others	RW modify	0
2	Reserved	—	—	—
1	Reserved	—	—	—
0	Reserved	—	—	—

5.129. STATUS_LVRST

STATUS_LVRST			
Description	Reset factor [Write]1: Factor clear. 0: Ignored		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 2204		
Physical address View0	0x4000 2204		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:25	Reserved	—	—	—
24	STATUS_LVRST_STOP	[Read]1: Return from STOP mode. 0: Others	RW oneToClear	0
23:21	Reserved	—	—	—
20	STATUS_LVRST_RTC	[Read]1: Return from RTC mode. 0: Others	RW oneToClear	0
19:17	Reserved	—	—	—
16	STATUS_LVRST_BOR	[Read]1: BOR. 0: Others	RW oneToClear	—
15:13	Reserved	—	—	—
12	STATUS_LVRST_cpu_SYSRESETREQ	[Read]1: CPU system reset request. 0: Others	RW oneToClear	0
11:9	Reserved	—	—	—
8	STATUS_LVRST_cpu_LOCKUP	[Read]1: Reset by a CPU hardware fault. 0: Others	RW oneToClear	0
7:5	Reserved	—	—	—
4	STATUS_LVRST_wdt_wdtResetout	[Read]1: WDT reset. 0: Others	RW oneToClear	0
3:1	Reserved	—	—	—
0	STATUS_LVRST_SYS_RESET_N	[Read]1: MCU_SYS_RESET_N terminal. 0: Others * 0 -> 1 in the power-on sequence	RW oneToClear	1

5.130. BROWNOUTMODE

BROWNOUTMODE			
Description	Brownout mode switching		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 2210		
Physical address View0	0x4000 2210		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31	BROWNOUT_EN	Brownout detection enable 0: Disable 1: Enable	RW modify	0
30:6	Reserved	—	—	—
5	BOMODE_INT_FOR_RTC_STOP	In RTC/STOP mode 0: Return to ACTIVE mode by BrownOut interrupt 1: BrownOut reset is asserted by BrownOut interrupt.	RW modify	0
4:1	Reserved	—	—	—
0	BOMODE	BrownOut Mode 0: Brownout reset 1: Brownout interrupt	RW modify	0

5.131. CTRL_IO_AON_0

CTRL_IO_AON_0			
Description	IO reset control (AON(PM) IO domain)		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 2300		
Physical address View0	0x4000 2300		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:1	Reserved	—	—	—
0	CTRL_IO_AON_PM_RESX	0: pull-up/pull-down/Hi-z(Depends on the IO cell) 1: (Depends on the LATI status.) * 0 -> in the reset release sequence	RW modify	1

5.132. CTRL_IO_AON_1

CTRL_IO_AON_1			
Description	IO setting retention control (AON(PM) IO domain)		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 2304		
Physical address View0	0x4000 2304		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:1	Reserved	—	—	—
0	CTRL_IO_AON_PM_LATI	(For RESX=H) 0: Normal 1: retain	RW modify	0

5.133. CTRL_IO_AON_2

CTRL_IO_AON_2			
Description	IO input standby control (AON(PM) IO domain) 0: Standby. 1: Active		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 2308		
Physical address View0	0x4000 2308		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:9	Reserved	—	—	—
8	CTRL_IO_ADC24_SYNC_STBX	MCU_ADC24_SYNC terminal	RW modify	0
7	Reserved	—	—	—
6	CTRL_IO_UA2_CTS_N_STBX	MCU_UA2_CTS_N terminal	RW modify	0
5	CTRL_IO_UA2_RTS_N_STBX	MCU_UA2_RTS_N terminal	RW modify	0
4	CTRL_IO_UA2D_STBX	MCU_UA2_RXD terminal MCU_UA2_TXD terminal	RW modify	0
3	Reserved	—	—	—
2	CTRL_IO_SPIM3_STBX	MCU_SPIM3_CS_N terminal MCU_SPIM3_CLK terminal MCU_SPIM3_MOSI terminal MCU_SPIM3_MISO terminal	RW modify	0
1	CTRL_IO_SPIM2_STBX	MCU_SPIM2_CS_N terminal MCU_SPIM2_CLK terminal MCU_SPIM2_MOSI terminal MCU_SPIM2_MISO terminal	RW modify	0
0	CTRL_IO_I2C2_STBX	MCU_I2C2_DATA terminal MCU_I2C2_CLK terminal	RW modify	0

5.134. CTRL_IO_AON_3

CTRL_IO_AON_3			
Description	IO input standby control (AON(PM) IO domain) 0: Standby. 1: Active		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 230C		
Physical address View0	0x4000 230C		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31	CTRL_IO_GPIO_31_STBX	MCU_GPIO_31 terminal	RW modify	0
30	CTRL_IO_GPIO_30_STBX	MCU_GPIO_30 terminal	RW modify	0
29	CTRL_IO_GPIO_29_STBX	MCU_GPIO_29 terminal	RW modify	0
28	CTRL_IO_GPIO_28_STBX	MCU_GPIO_28 terminal	RW modify	0
27	CTRL_IO_GPIO_27_STBX	MCU_GPIO_27 terminal	RW modify	0
26	CTRL_IO_GPIO_26_STBX	MCU_GPIO_26 terminal	RW modify	0
25	CTRL_IO_GPIO_25_STBX	MCU_GPIO_25 terminal	RW modify	0
24	CTRL_IO_GPIO_24_STBX	MCU_GPIO_24 terminal	RW modify	0
23:16	Reserved	—	—	—
15	CTRL_IO_GPIO_15_STBX	MCU_GPIO_15 terminal	RW modify	0
14	CTRL_IO_GPIO_14_STBX	MCU_GPIO_14 terminal	RW modify	0
13	CTRL_IO_GPIO_13_STBX	MCU_GPIO_13 terminal	RW modify	0
12	CTRL_IO_GPIO_12_STBX	MCU_GPIO_12 terminal	RW modify	0
11	CTRL_IO_GPIO_11_STBX	MCU_GPIO_11 terminal	RW modify	0
10	CTRL_IO_GPIO_10_STBX	MCU_GPIO_10 terminal	RW modify	0
9	CTRL_IO_GPIO_9_STBX	MCU_GPIO_9 terminal	RW modify	0
8	CTRL_IO_GPIO_8_STBX	MCU_GPIO_8 terminal	RW modify	0
7	CTRL_IO_GPIO_7_STBX	MCU_GPIO_7 terminal	RW modify	0
6	CTRL_IO_GPIO_6_STBX	MCU_GPIO_6 terminal	RW modify	0
5	CTRL_IO_GPIO_5_STBX	MCU_GPIO_5 terminal	RW modify	0
4	CTRL_IO_GPIO_4_STBX	MCU_GPIO_4 terminal	RW modify	0
3	CTRL_IO_GPIO_3_STBX	MCU_GPIO_3 terminal	RW modify	0
2	CTRL_IO_GPIO_2_STBX	MCU_GPIO_2 terminal	RW modify	0
1	CTRL_IO_GPIO_1_STBX	MCU_GPIO_1 terminal	RW modify	0
0	Reserved	—	—	—

5.135. CTRL_IO_AON_4

CTRL_IO_AON_4			
Description	IO reset control (AON(PP1) IO domain)		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 2310		
Physical address View0	0x4000 2310		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:1	Reserved	—	—	—
0	CTRL_IO_AON_PP1_RESX	0: pull-up/pull-down/Hi-z(Depends on the IO cell) 1: (Depends on the LATI status.) * 0 -> in the reset release sequence	RW modify	1

5.136. CTRL_IO_AON_5

CTRL_IO_AON_5			
Description	IO setting retention control (AON(PP1) IO domain)		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 2314		
Physical address View0	0x4000 2314		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:1	Reserved	—	—	—
0	CTRL_IO_AON_PP1_LATI	(For RESX=H) 0: Normal 1: retain	RW modify	0

5.137. CTRL_IO_AON_6

CTRL_IO_AON_6			
Description	IO input standby control (AON(PP1) IO domain) 0: Standby. 1: Active		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 2318		
Physical address View0	0x4000 2318		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:24	Reserved	—	—	—
23	CTRL_IO_SPIM1_MISO_STBX	MCU_SPIM1_MISO terminal	RW modify	0
22	CTRL_IO_SPIM1_MOSI_STBX	MCU_SPIM1_MOSI terminal	RW modify	0
21	CTRL_IO_SPIM1_CLK_STBX	MCU_SPIM1_CLK terminal	RW modify	0

20	CTRL_IO_SPIM1_CS_N_STBX	MCU_SPIM1_CS_N terminal	RW modify	0
19	CTRL_IO_SPIM0_MISO_STBX	MCU_SPIM0_MISO terminal	RW modify	0
18	CTRL_IO_SPIM0_MOSI_STBX	MCU_SPIM0_MOSI terminal	RW modify	0
17	CTRL_IO_SPIM0_CLK_STBX	MCU_SPIM0_CLK terminal	RW modify	0
16	CTRL_IO_SPIM0_CS_N_STBX	MCU_SPIM0_CS_N terminal	RW modify	0
15	CTRL_IO_I2C1_CLK_STBX	MCU_I2C1_CLK terminal	RW modify	0
14	CTRL_IO_I2C1_DATA_STBX	MCU_I2C1_DATA terminal	RW modify	0
13	CTRL_IO_I2C0_CLK_STBX	MCU_I2C0_CLK terminal	RW modify	0
12	CTRL_IO_I2C0_DATA_STBX	MCU_I2C0_DATA terminal	RW modify	0
11	CTRL_IO_UA1_CTS_N_STBX	MCU_UA1_CTS_N terminal	RW modify	0
10	CTRL_IO_UA1_RTS_N_STBX	MCU_UA1_RTS_N terminal	RW modify	0
9	CTRL_IO_UA1_TXD_STBX	MCU_UA1_TXD terminal	RW modify	0
8	CTRL_IO_UA1_RXD_STBX	MCU_UA1_RXD terminal	RW modify	0
7:1	Reserved	—	—	—
0	CTRL_IO_UART0_STBX	MCU_UA0_RXD terminal MCU_UA0_TXD terminal	RW modify	0

5.138. PSW_PU

PSW_PU			
Description	Internal Power Switch control of the PU power supply domain [Write]1: Power is supplied. 0: Power is turned off. [Read]1: Power is being supplied. 0: Power is being turned off.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 2420		
Physical address View0	0x4000 2420		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:2	Reserved	—	—	—
1	PSW_PU_VDDCS	VDDC strong switch control	RW modify	0
0	PSW_PU_VDDCW	VDDC weak switch control	RW modify	0

5.139. PSW_EFUSE

PSW_EFUSE			
Description	Internal Power Switch control of the EFUS power supply domain [Write]1: Power is supplied. 0: Power is turned off. [Read]1: Power is being supplied. 0: Power is being turned off.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 2440		
Physical address View0	0x4000 2440		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:2	Reserved	—	—	—
1	PSW_EFUSE_VDDCS	VDDC strong switch control * 0 -> 1 in the reset release sequence	RW modify	1
0	PSW_EFUSE_VDDCW	VDDC weak switch control * 0 -> 1 in the reset release sequence	RW modify	1

5.140. PSW_PLL

PSW_PLL			
Description	Internal Power Switch control of the PLL power supply domain [Write]1: Power is supplied. 0: Power is turned off. [Read]1: Power is being supplied. 0: Power is being turned off.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 2444		
Physical address View0	0x4000 2444		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:2	Reserved	—	—	—
1	PSW_PLL_VDDCS	VDDC strong switch control * Switching from 0 to 1 may occur in the reset release sequence.	RW modify	0
0	PSW_PLL_VDDCW	VDDC weak switch control * Switching from 0 to 1 may occur in the reset release sequence.	RW modify	0

5.141. PSW_ADPLL

PSW_ADPLL					
Description	Internal Power Switch control of the ADPLL power supply domain [Write]1: Power is supplied. 0: Power is turned off. [Read]1: Power is being supplied. 0: Power is being turned off.				
Address Region	pmulv		**Type:**	RW	
Offset	0x0000 2448				
Physical address View0	0x4000 2448				
Physical address View1	—				
Bitfield Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:2	Reserved	—		—	—
1	PSW_ADPLL_VDDCS	VDDC strong switch control		RW modify	0
0	PSW_ADPLL_VDDCW	VDDC weak switch control		RW modify	0

5.142. PSW_IO_USB

PSW_IO_USB					
Description	Internal Power Switch control of the IO_USB [Write]1: Power is supplied. 0: Power is turned off. [Read]1: Power is being supplied. 0: Power is being turned off.				
Address Region	pmulv		**Type:**	RW	
Offset	0x0000 2450				
Physical address View0	0x4000 2450				
Physical address View1	—				
Bitfield Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:2	Reserved	—		—	—
1	PSW_IO_USB_VDDCS	VDDC strong switch control		RW modify	0
0	PSW_IO_USB_VDDCW	VDDC weak switch control		RW modify	0

5.143. PSW_HARDMACRO

PSW_HARDMACRO					
Description	Internal Power Switch control of Hard Macro [Write]1: Power is supplied. 0: Power is turned off. [Read]1: Power is being supplied. 0: Power is being turned off.				
Address Region	pmulv		**Type:**	RW	
Offset	0x0000 2454				
Physical address View0	0x4000 2454				
Physical address View1	—				
Bitfield Details					
Bits	**Name**	**Description**		**Access**	**Reset**
31:6	Reserved	—		—	—

5	PSW_ACC_VDDCS	ACC VDDC strong switch control	RW modify	0
4	PSW_ACC_VDDCW	ACC VDDC weak switch control	RW modify	0
3	PSW_MAG_VDDCS	MAG VDDC strong switch control	RW modify	0
2	PSW_MAG_VDDCW	MAG VDDC weak switch control	RW modify	0
1	PSW_GYRO_VDDCS	GYRO VDDC strong switch control	RW modify	0
0	PSW_GYRO_VDDCW	GYRO VDDC weak switch control	RW modify	0

5.144. ISO_PU

ISO_PU			
Description	PU power supply domain isolation control [Write]1: Signal is fixed. 0: No signal is fixed. [Read]1: Signal is being fixed. 0: No signal is fixed.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 2520		
Physical address View0	0x4000 2520		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:2	Reserved	—	—	—
1	OUTISOEN_PU	Output signal isolation control	RW modify	1
0	INISOEN_PU	Input signal isolation control	RW modify	1

5.145. ISO_EFUSE

ISO_EFUSE			
Description	EFUSE power supply domain isolation control [Write]1: Signal is fixed. 0: No signal is fixed. [Read]1: Signal is being fixed. 0: No signal is fixed.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 2540		
Physical address View0	0x4000 2540		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:2	Reserved	—	—	—
1	OUTISOEN_EFUSE	Output signal isolation control * 1 -> 0 in the reset release sequence	RW modify	0
0	INISOEN_EFUSE	Input signal isolation control * 1 -> 0 in the reset release sequence	RW modify	0

5.146. ISO_PLL

ISO_PLL			
Description	PLL power supply domain isolation control [Write]1: Signal is fixed. 0: No signal is fixed. [Read]1: Signal is being fixed. 0: No signal is fixed.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 2544		
Physical address View0	0x4000 2544		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:2	Reserved	—	—	—
1	OUTISOEN_PLL	Output signal isolation control * Switching from 1 to 0 may occur in the reset release sequence.	RW modify	1
0	INISOEN_PLL	Input signal isolation control * Switching from 1 to 0 may occur in the reset release sequence.	RW modify	1

5.147. ISO_ADPLL

ISO_ADPLL			
Description	ADPLL power supply domain isolation control [Write]1: Signal is fixed. 0: No signal is fixed. [Read]1: Signal is being fixed. 0: No signal is fixed.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 2548		
Physical address View0	0x4000 2548		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:2	Reserved	—	—	—
1	OUTISOEN_ADPLL	Output signal isolation control	RW modify	1
0	INISOEN_ADPLL	Input signal isolation control	RW modify	1

5.148. IRQ_SETTING_0

IRQ_SETTING_0			
Description	Setting of Wakeup detection * The following "bit*" is a bit number in 4 bits of setting registers for every interrupt. bit0: Rising edge detection bit1: Falling edge detection bit2: Low level detection bit3: High level detection 1: enable 0: disable * If all bits are set to 0, it will be the state of mask. * If 1 is written to bit0 and bit1, the both edge is detected.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 2700		
Physical address View0	0x4000 2700		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:28	IRQ_GPIO7_setting	MCU_GPIO_7 terminal	RW modify	0x0
27:24	IRQ_GPIO6_setting	MCU_GPIO_6 terminal	RW modify	0x0
23:20	IRQ_GPIO5_setting	MCU_GPIO_5 terminal	RW modify	0x0
19:16	IRQ_GPIO4_setting	MCU_GPIO_4 terminal	RW modify	0x0
15:12	IRQ_GPIO3_setting	MCU_GPIO_3 terminal	RW modify	0x0
11:8	IRQ_GPIO2_setting	MCU_GPIO_2 terminal	RW modify	0x0
7:4	IRQ_GPIO1_setting	MCU_GPIO_1 terminal	RW modify	0x0
3:0	IRQ_GPIO0_setting	MCU_GPIO_0 terminal	RW modify	0x0

5.149. IRQ_SETTING_1

IRQ_SETTING_1			
Description	Setting of Wakeup detection * The following "bit*" is a bit number in 4 bits of setting registers for every interrupt. bit0: Rising edge detection bit1: Falling edge detection bit2: Low level detection bit3: High level detection 1: enable 0: disable * If all bits are set to 0, it will be the state of mask. * If 1 is written to bit0 and bit1, the both edge is detected.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 2704		
Physical address View0	0x4000 2704		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:28	IRQ_CPU_DEBUGIN_setting	CPU debug interrupt	RW modify	0x0
27:24	IRQ_RTCHVWAKEUP_setting	RTCHV wakeup interrupt	RW modify	0x0
23:20	IRQ_BROWNOUT_setting	Brownout interrupt	RW modify	0x0
19:16	IRQ_GPIO30_setting	MCU_GPIO_30 terminal	RW modify	0x0
15:12	IRQ_GPIO27_setting	MCU_GPIO_27 terminal	RW modify	0x0
11:8	IRQ_GPIO26_setting	MCU_GPIO_26 terminal	RW modify	0x0
7:4	IRQ_GPIO25_setting	MCU_GPIO_25 terminal	RW modify	0x0
3:0	IRQ_GPIO24_setting	MCU_GPIO_24 terminal	RW modify	0x0

5.150. IRQ_STATUS

IRQ_STATUS			
Description	Cause of Wakeup [Write]1: Wakeup cause clear. 0: Ignored [Read]1: Wakeup cause available. 0: No wakeup cause * All detected cause can be checked.		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 2708		
Physical address View0	0x4000 2708		
Physical address View1	—		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:18	Reserved	—	—	—
17	IRQ_CPU_DEBUGIN	CPU debug interrupt	RW oneToClear	0
16	IRQ_RTCHVWAKEUP	RTCHV wakeup interrupt	RW oneToClear	0
15	IRQ_BROWNOUT	Brownout interrupt	RW oneToClear	0
14:13	Reserved	—	—	—
12	IRQ_GPIO30	MCU_GPIO_30 terminal	RW oneToClear	0
11	IRQ_GPIO27	MCU_GPIO_27 terminal	RW oneToClear	0
10	IRQ_GPIO26	MCU_GPIO_26 terminal	RW oneToClear	0
9	IRQ_GPIO25	MCU_GPIO_25 terminal	RW oneToClear	0
8	IRQ_GPIO24	MCU_GPIO_24 terminal	RW oneToClear	0
7	IRQ_GPIO7	MCU_GPIO_7 terminal	RW oneToClear	0
6	IRQ_GPIO6	MCU_GPIO_6 terminal	RW oneToClear	0
5	IRQ_GPIO5	MCU_GPIO_5 terminal	RW oneToClear	0
4	IRQ_GPIO4	MCU_GPIO_4 terminal	RW oneToClear	0
3	IRQ_GPIO3	MCU_GPIO_3 terminal	RW	0

			oneToClear	
2	IRQ_GPIO2	MCU_GPIO_2 terminal	RW oneToClear	0
1	IRQ_GPIO1	MCU_GPIO_1 terminal	RW oneToClear	0
0	IRQ_GPIO0	MCU_GPIO_0 terminal	RW oneToClear	0

5.151. WAKEUP_EN

WAKEUP_EN			
Description	Setting of Wakeup interrupt 0: Wakeup interrupt disable 1: Wakeup interrupt enable		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 270C		
Physical address View0	0x4000 270C		
Physical address View1	—		

Bitfield Details

Bits	Name	Description	Access	Reset
31:18	Reserved	—	—	—
17	WAKEUP_CPU_DEBUGIN_enable	CPU debug interrupt	RW modify	0
16	WAKEUP_RTCHVWAKEUP_enable	RTCHV wakeup interrupt	RW modify	0
15	WAKEUP_BROWNOUT_enable	Brownout interrupt	RW modify	0
14:13	Reserved	—	—	—
12	WAKEUP_GPIO30_enable	MCU_GPIO_30 terminal	RW modify	0
11	WAKEUP_GPIO27_enable	MCU_GPIO_27 terminal	RW modify	0
10	WAKEUP_GPIO26_enable	MCU_GPIO_26 terminal	RW modify	0
9	WAKEUP_GPIO25_enable	MCU_GPIO_25 terminal	RW modify	0
8	WAKEUP_GPIO24_enable	MCU_GPIO_24 terminal	RW modify	0
7	WAKEUP_GPIO7_enable	MCU_GPIO_7 terminal	RW modify	0
6	WAKEUP_GPIO6_enable	MCU_GPIO_6 terminal	RW modify	0
5	WAKEUP_GPIO5_enable	MCU_GPIO_5 terminal	RW modify	0
4	WAKEUP_GPIO4_enable	MCU_GPIO_4 terminal	RW modify	0
3	WAKEUP_GPIO3_enable	MCU_GPIO_3 terminal	RW modify	0
2	WAKEUP_GPIO2_enable	MCU_GPIO_2 terminal	RW modify	0
1	WAKEUP_GPIO1_enable	MCU_GPIO_1 terminal	RW modify	0
0	WAKEUP_GPIO0_enable	MCU_GPIO_0 terminal	RW modify	0

5.152. WAKEUP_STATUS

WAKEUP_STATUS			
Description	Cause of Wakeup interrupt 0: No wakeup interrupt cause 1: Wakeup interrupt available * Only cause that set 1 to ***[WAKEUP_EN]*** can be checked.		
Address Region	pmulv	**Type:**	RO
Offset	0x0000 2710		
Physical address View0	0x4000 2710		
Physical address View1	—		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:18	Reserved	—	—	—
17	WAKEUP_CPU_DEBUGIN_status	CPU debug interrupt	RO	0
16	WAKEUP_RTCHVWAKEUP_status	RTCHV wakeup interrupt	RO	0
15	WAKEUP_BROWNOUT_status	Brownout interrupt	RO	0
14:13	Reserved	—	—	—
12	WAKEUP_GPIO30_status	MCU_GPIO_30 terminal	RO	0
11	WAKEUP_GPIO27_status	MCU_GPIO_27 terminal	RO	0
10	WAKEUP_GPIO26_status	MCU_GPIO_26 terminal	RO	0
9	WAKEUP_GPIO25_status	MCU_GPIO_25 terminal	RO	0
8	WAKEUP_GPIO24_status	MCU_GPIO_24 terminal	RO	0
7	WAKEUP_GPIO7_status	MCU_GPIO_7 terminal	RO	0
6	WAKEUP_GPIO6_status	MCU_GPIO_6 terminal	RO	0
5	WAKEUP_GPIO5_status	MCU_GPIO_5 terminal	RO	0
4	WAKEUP_GPIO4_status	MCU_GPIO_4 terminal	RO	0
3	WAKEUP_GPIO3_status	MCU_GPIO_3 terminal	RO	0
2	WAKEUP_GPIO2_status	MCU_GPIO_2 terminal	RO	0
1	WAKEUP_GPIO1_status	MCU_GPIO_1 terminal	RO	0
0	WAKEUP_GPIO0_status	MCU_GPIO_0 terminal	RO	0

5.153. CTRL_CDBGPWRUPREQ

CTRL_CDBGPWRUPREQ			
Description	Reset Control at the JTAG connection		
Address Region	pmulv	**Type:**	RW
Offset	0x0000 2808		
Physical address View0	0x4000 2808		
Physical address View1	—		

Bitfield Details				
Bits	**Name**	**Description**	**Access**	**Reset**
31:1	Reserved	—	—	—
0	CDBGPWRUPREQ_EN	control by the following cause of reset: - CPU system reset request - Reset by the CPU hardware fault - WDT reset 0: all blocks except for the PA power domain 1: CPU core and WDT(when the cause of reset is WDT reset)	RW modify	1

6. Revision History

Table 6.1 Revision History

Revision	Date	Description
0.1	2014-03-19	Newly released
0.2	2014-04-16	4.1.4.1.2. OSC32K Added trimming value change procedure. 4.1.4.1.3. SIOSC4M Corrected SIOSC4M trimming value change procedure. 4.2.3.8. PADPLL Domain control Deleted ***[CONFIG_BGR_0]***.BGR_PDX33_ADPLL control. Added Wait time.
0.3	2014-05-08	Corrected the error in Figure 4.1.
0.4	2014-10-14	Revised for rev.2.0
1.0	2015-01-16	Official version
1.1	2015-02-12	Revised 5. Details of Registers section.
1.2	2015-06-23	4.3.3**:** added the description of ACTIVE-WFI. 4.3.2.5**:** change the procedure of Voltagemode (from ModeA to ModeB and from ModeB to ModeA)
1.3	2015-07-02	4.1.4.5**:** delete the procedure of start-up and stop about OSC12M.
1.4	2015-08-19	Added description 4.3.3.7 Revised Technical Data Sheet Hardware Specification reference number in 4.1.4.1. / 4.1.4.2. / 4.1.4.4.
1.5	2015-12-28	Added description 4.3.3.3 and 4.3.3.4. "are changed to 4 MHz clock whose source is the SIOSC4M" ->Because this description is confusion, added "divided by one"
1.6	2018-02-07	Changed header, footer and the last page. Changed corporate name and descriptions. Modified description of the trademark. Corrected typos.

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