

TOSHIBA Diode Silicon Epitaxial Planar Type

HN2D02FU

Ultra High Speed Switching Application

- HN2D02FU is composed of 3 independent diodes.
- Low forward voltage : $V_F(3) = 0.98V$ (typ.)
- Fast reverse recovery time : $t_{rr} = 1.6$ ns (typ.)
- Small total capacitance : $C_T = 0.5$ pF (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Maximum (peak) reverse Voltage	V_{RM}	85	V
Reverse voltage	V_R	80	V
Maximum (peak) forward current	I_{FM}	240 *	mA
Average forward current	I_O	80 *	mA
Surge current (10ms)	I_{FSM}	1 *	A
Power dissipation	P	200	mW
Junction temperature	T_j	125	°C
Storage temperature	T_{stg}	-55 to 125	°C

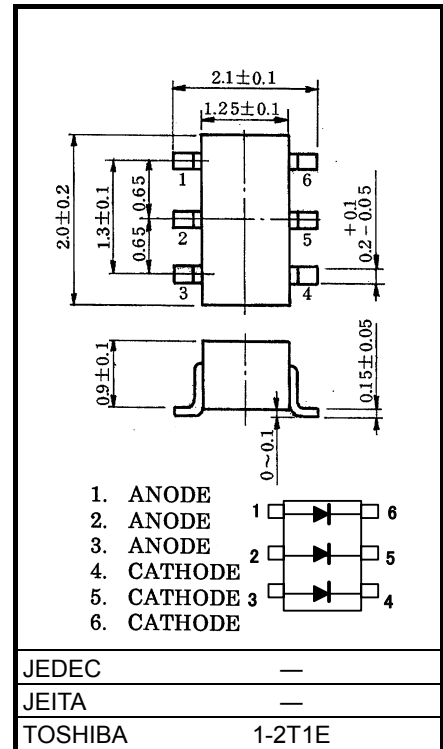
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

* : This is absolute maximum rating of single diode (Q1 or Q2 or Q3).
In the case of using 2 ro 3 diodes, the absolute maximum ratings per diodes is 75 % of the single diode one.

Electrical Characteristics (Q1, Q2, Q3 Common, Ta = 25°C)

Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Forward voltage	$V_F(1)$	$I_F = 1$ mA	—	0.62	—	V
	$V_F(2)$	$I_F = 10$ mA	—	0.75	—	
	$V_F(3)$	$I_F = 100$ mA	—	0.98	1.20	
Reverse current	$I_R(1)$	$V_R = 30$ V	—	—	0.1	μA
	$I_R(2)$	$V_R = 80$ V	—	—	0.5	
Total capacitance	C_T	$V_R = 0, f = 1$ MHz	—	0.5	3.0	pF
Reverse recovery time	t_{rr}	$I_F = 10$ mA (Fig.1)	—	1.6	4.0	ns

Unit: mm



Weight: 6.8 mg (typ.)

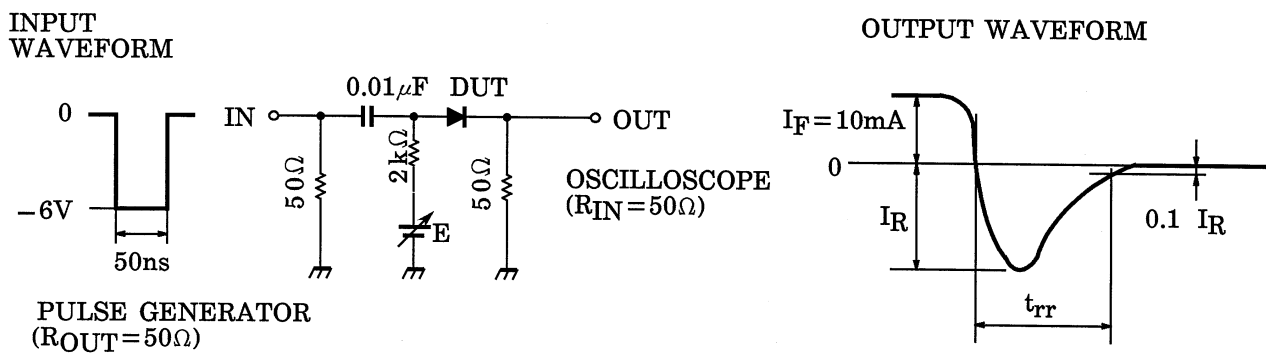
Start of commercial production
1990-10

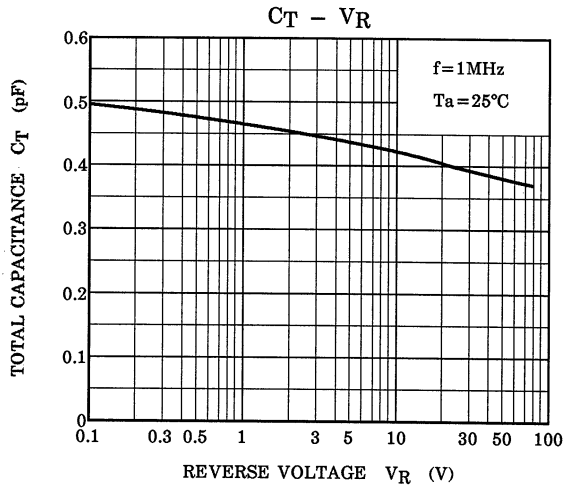
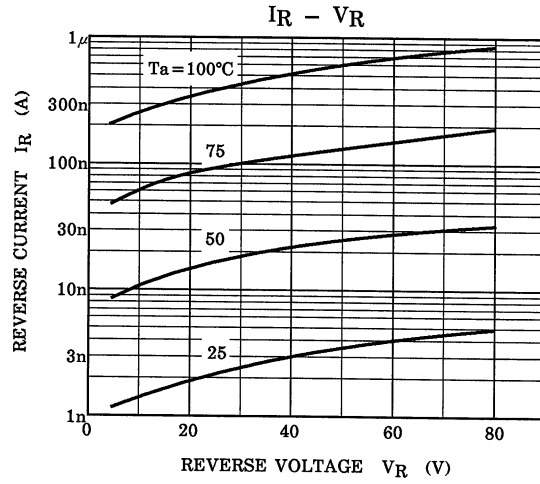
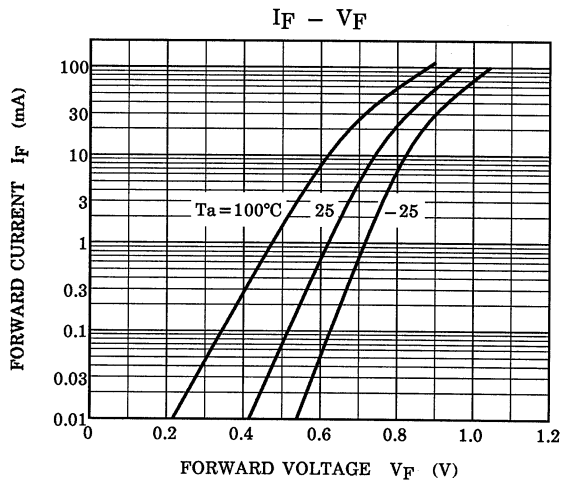
Marking

Pin Assignment (top view)



Fig.1 Reverse Recovery Time (t_{rr}) Test Circuit





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