32-bit RISC Microcontroller

TXZ Family

Reference Manual

Boundary-scan

(BSC-A)

Revision 1.0

2017-08

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Preface

Related document

Document name
Data Sheet
Input/Output Ports
Product Information

Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the “0b” when the number of bit can be distinctly understood from a sentence.
- “_N” is added to the end of signal names to indicate low active signals.
- It is called “assert” that a signal moves to its active level, “deassert” to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by *[ ]* defines the register.
  Example: ***[ABCD]***
- “n” substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1], [XYZ2], [XYZ3] → [XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, “x” means A, B, and C …
  Example: ***[ADACR0], [ADBCR0], [ADCCR0] → [ADxCR0]***
  In case of channel, “x” means 0, 1, and 2…
  Example: ***[T32A0RUNA], [T32A1RUNA], [T32A2RUNA] → [T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is “-“, follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value. In the cases that default is “-“, follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

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Terms and Abbreviations

Some of abbreviations used in this document are as follows:

JTAG	Joint Test Action Group

1. Outlines

This product provides a boundary-scan interface that is compatible with Joint Test Action Group(JTAG) specifications.

With the evolution of ever-denser integrated circuits (ICs), surface-mounted devices, double-sided component mounting on printed-circuit boards (PCBs), and set-in recesses, in-circuit tests that depend upon physical contact like the connection of the internal board and chip has become more and more difficult to use. The more ICs have be-come complex, the larger and more difficult the test program became.

As one of the solutions, boundary-scan circuits started to be developed. A boundary-scan circuit is a series of shift register cells placed between the pins and the internal circuitry of the IC to which the said pins are connected. Normally, these boundary-scan cells are bypassed; when the IC enters test mode, however, the scan cells can be directed by the test program to pass data along the shift register path and perform various diagnostic tests. To accomplish this, the tests use the five signals, TCK, TMS, TDI, TDO and TRST_N.

The JTAG boundary-scan mechanism (hereinafter referred to as JTAG mechanism in the chapter) allows testing of the connections between the processor, the printed circuit board to which it is attached, and the other components on the circuit board.

The JTAG mechanism cannot test the processor itself.

This chapter describes the JTAG interface, with the descriptions of boundary scan and the pins and signals used by the interface.

Table 1.1 Features

Function Classification	Description
JTAG standard version	IEEE Standard 1149.1 -1990 (Includes IEEE Standard 1149.1a - 1993)
JTAG instructions	Standard instructions (BYPASS, SAMPLE/PRELOAD, EXTEST) HIGHZ instruction CLAMP instruction
IDCODE	Not available
Pins	Pins excluded from boundary scan register (BSR) ● Oscillator circuit pins (X1, X2, XT1, XT2) ● JTAG control pins (BSC) ● Power supply/GND pins (including reference supply pin for ADC and DAC) ● Function pins(TDI/TDO/TMS/TCK/TRST_N) ● Regulator pins ● Reset pin(RESET_N)

2. Configuration

The microcontroller supports debugging by connecting the JTAG interface with a JTAG-compliant development tool.

For information about debugging, refer to the specification of the development tool used.

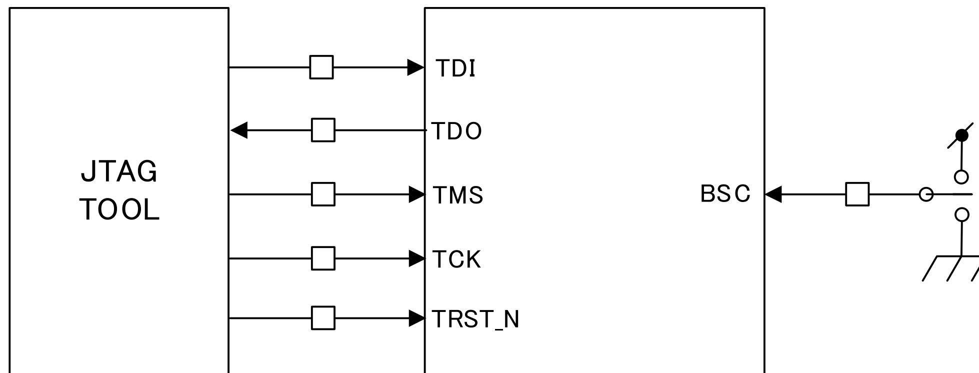

Figure 2.1 Example of connection with a JTAG development tool

Table 2.1 Table of Signals

No.	Symbol	Signal Name	I/O	Related Reference Manual
1	TDI	JTAG serial data input	Input	Input/Output Ports
2	TDO	JTAG serial data output	Output	Input/Output Ports
3	TMS	JTAG test mode select	Input	Input/Output Ports
4	TCK	JTAG serial clock input	Input	Input/Output Ports
5	TRST_N	JTAG test reset input	Input	Input/Output Ports
6	BSC	ICE/JTAG test select input (compatible with the Enable signal)	Input	Data Sheet

Table 2.2 Mode setting pin

Mode Setting Pin (BSC)	Operation mode
0	It operates Debug Mode.
1	It operates in Boundary Scan Mode

3. Function and Operation

The processor contains the following JTAG controller and registers.

- Instruction register
- Boundary scan register
- Bypass register
- Device identification register
- Test Access Port (TAP) controller

JTAG basically operates to monitor the TMS input signal with the TAP controller state machine. When the monitoring starts, the TAP controller determines the test functionality to be implemented. This includes both loading the JTAG instruction register (IR) and beginning a serial data scan through a data register (DR), as shown in Table 3.1. The data scan is transferred to next statement by state of TMS pin. The data register is selected according to the contents of the instruction register.

3.1. Instruction Register

The JTAG instruction register includes four shift register-based cells. This register is used to select the test to be performed and/or the test data register to be accessed. As listed in Table 3.1, this instruction codes select either the boundary scan register or the bypass register.

Table 3.1 JTAG Instruction Register Bit Configuration

instruction code (MSB -> LSB)	instruction	Selected data register
0000	EXTEST	Boundary scan register
0001	SAMPLE/PRELOAD	Boundary scan register
0100 to 1110	-	-
0010	HIGHZ	Bypass register
0011	CLAMP	Bypass register
1111	BYPASS	Bypass register

Figure 3.1 shows the format of the instruction register.

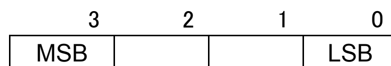

Figure 3.1 Instruction register

The instruction code is shifted out to the instruction register from the LSB.

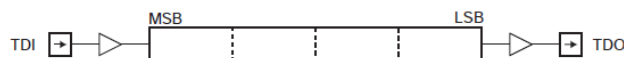

Figure 3.2 Instruction Register Shift Direction

The bypass register is 1 bit wide. When the TAP controller is in the Shift-DR (bypass) state, the data on the TDI pin is shifted into the bypass register, and the bypass register output shifts to the data out on the TDO output pin.

In essence, the bypass register is an alternative route which allows bypassing of board-level devices in the serial

boundary-scan chain, which are not required for a specific test. The logical location of the bypass register in the boundary-scan chain is shown in Figure 3.3.

Use of the bypass register speeds up access to the boundary scan register in the IC that remains active in the board-level test data path.

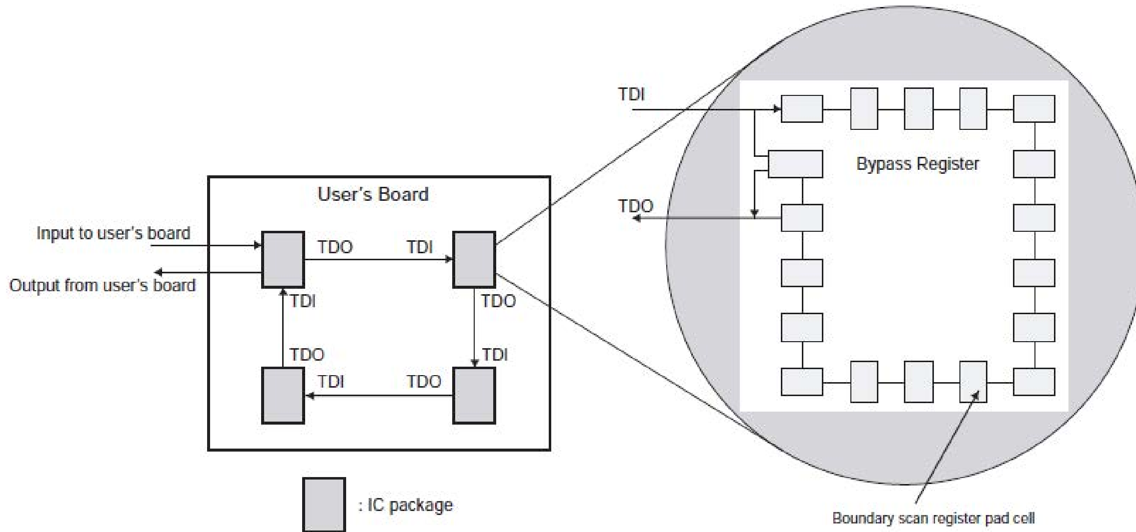

Figure 3.3 Bypass Register Operation

3.2. Boundary Scan Register

The boundary scan register provides all the inputs and outputs of the microcontroller except some analog outputs and control signals. The pins of this product allow any pattern to be driven by scanning the data into the boundary scan register in the Shift-DR state. Incoming data to the processor is examined by enabling the boundary scan register and shifting the data when the BSR is in the Capture-DR state.

The boundary scan register is shift register-based path containing cells connected to the in-put and output pads on this product.

The TDI input is loaded to the LSB of the boundary scan register. The MSB of the boundary scan register is shifted out on the TDO output.

3.3. TAP Controller

The processor incorporates the 16-state TAP controller stipulated in the IEEE JTAG specification.

3.3.1. Resetting the TAP Controller

The TAP controller state machine can be put into the Reset state by the following method.

Assertion of the TRST_N signal input (low) resets the TAP controller. After the processor reset state is released, keep the TMS input signal asserted through five consecutive rising edges of TCK input. Then TAP controller is reset. Keeping TMS asserted maintains the Reset state.

3.3.2. State Transitions of the TAP Controller

The state transition diagram of the TAP controller is shown in Figure 3.4. Each arrow between states is labeled with a 1 or 0, indicating the logic value of TMS that must be set up before the rising edge of TCK to cause the transition.

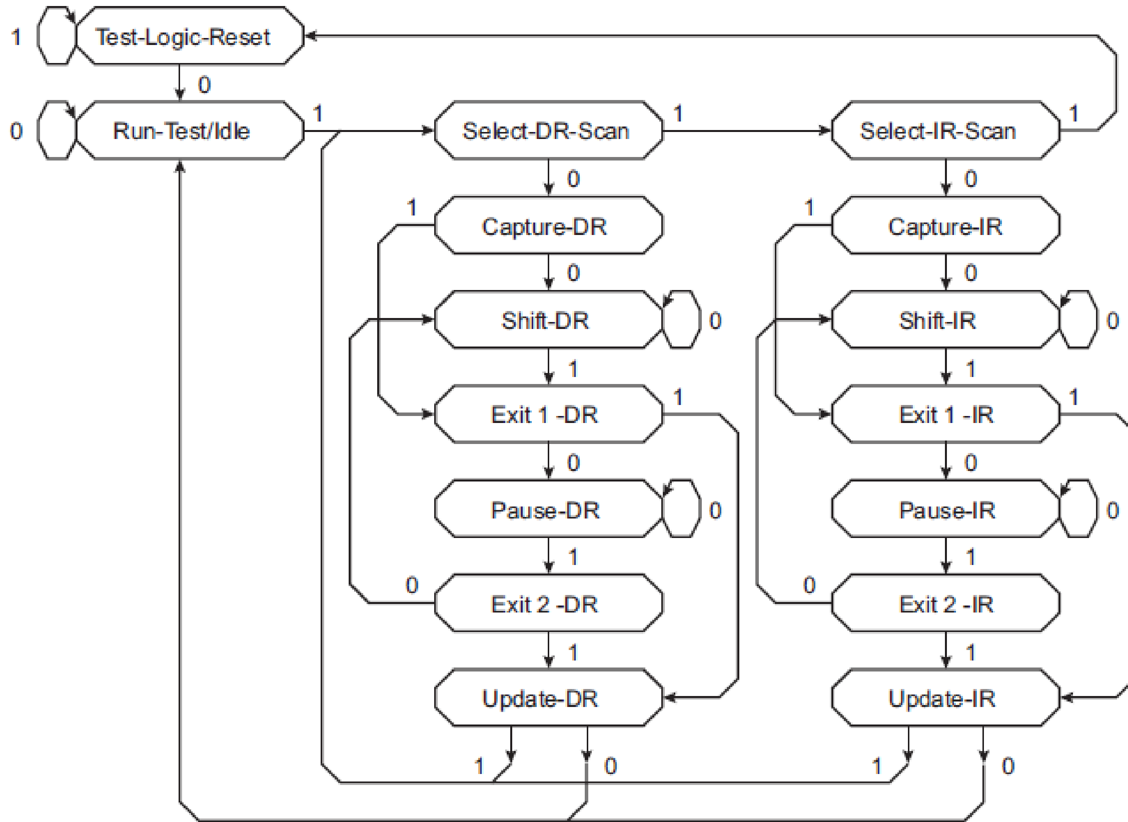

Figure 3.4 TAP Controller State Transition Diagram

The following paragraphs describe each of the controller states. The left column in Figure 3.4 is the data column, and the right column is the instruction column. The data column and instruction column reference the data register (DR) and the instruction register (IR), respectively.

– Test-Logic-Reset

When the TAP controller is in the Reset state, the device identification register is selected by default. The MSB of the boundary scan register is cleared to 0 which disables the outputs.

The TAP controller remains in this state while TMS is high. If TMS is held low while the TAP controller is in this state, then the controller moves to the Run-Test/Idle state.

– Run-Test/Idle

In the Run-Test/Idle state, the IC is put in test mode only when certain instructions such as a built-in self test (BIST) instruction are present. For instructions that do not cause any activities in this state, all test data registers selected by the current instruction retain their previous states.

The TAP controller remains in this state while TMS is held low. When TMS is held high, the controller moves to the Select-DR-Scan state.

– Select-DR-Scan

This is a temporary controller state. Here, the IC does not execute any specific functions.

If TMS is held low when the TAP controller is in this state, the controller moves to the Capture-DR state. If TMS is held high, the controller moves to the Select-IR-Scan state.

– Select-IR-Scan

This is a temporary controller state. Here, the IC does not execute any specific functions.

If TMS is held low when the TAP controller is in this state, the controller moves to the Capture-IR state, If TMS is held high, the controller returns to the Test-Logic-Reset state..

– Capture-DR

In this state, if the test data register selected by the current instruction has parallel inputs, then data is parallel loaded into the shift portion of the data register. If the test data register does not have parallel inputs, or if data needs not be loaded into the selected data register, then the data register retains its previous state.

If TMS is held low when the TAP controller is in this state, the controller moves to the Shift-DR state. If TMS is held high, the controller moves to the Exit 1-DR state.

– Shift-DR

In this controller state, the test data register connected between TDI and TDO shifts data out serially.

When the TAP controller is in this state, then it remains in the Shift-DR state if TMS is held low, or moves to the Exit 1-DR state if TMS is held high.

– Exit 1-DR

This is a temporary controller state.

If TMS is held low when the TAP controller is in this state, the controller moves to the Pause-DR state. If TMS is held high, the controller moves to the Update-DR state.

– Pause-DR

This state allows the shifting of the data register selected by the instruction register to be temporarily suspended. Both the instruction register and the data register retain their current states.

When the TAP controller is in this state, then it remains in the Pause-DR state if TMS is held low, or moves to the Exit 2-DR state if TMS is held high.

– Exit 2-DR

This is a temporary controller state.

When the TAP controller is in this state, it returns to the Shift-DR state if TMS is held low, or moves on to the Update-DR state if TMS is held high.

– Update-DR

In this state, data is latched, on the rising edge of TCK, onto the parallel outputs of the data registers from the shift register path. The data held at the parallel output does not change while data is shifted in the associated shift register path.

When the TAP controller is in this state, it moves to either the Run-Test/Idle state if TMS is held low, or the Select-DR-Scan state if TMS is held high.

– Capture-IR

In this state, data is parallel-loaded into the instruction register. The data to be loaded is "0001". The Capture-IR state is used for testing the instruction register. Faults in the instruction register, if any, may be detected by shifting out the loaded data.

When the TAP controller is in this state, it moves to either the Shift-IR state if TMS is held low, or

the Exit 1-IR state if TMS is high.

– Shift-IR

In this state, the instruction register is connected between TDI and TDO and shifts the captured data toward its serial output on the rising edge of TCK.

When the TAP controller is in this state, it remains in the Shift-IR state if TMS is low, or moves to the Exit 1-IR state if TMS is high.

– Exit 1-IR

This is a temporary controller state.

When the TAP controller is in this state, it moves to either the Pause-IR state if TMS is held low, or the Update-IR state if TMS is held high.

– Pause-IR

This state allows the shifting of the instruction register to be temporarily suspended. Both the instruction register and the data register retain their current states.

When the TAP controller is in this state, it remains in the Pause-IR state if TMS is held low, or moves to the Exit 2-IR state if TMS is held high.

– Exit 2-IR

This is a temporary controller state.

When the TAP controller is in this state, it moves to either the Shift-IR state if TMS is held low, or the Update-IR state if TMS is held high.

– Update-IR

This state allows the instruction previously shifted into the instruction register to be output in parallel on the rising edge of TCK. Then it becomes the current instruction, setting a new operational mode.

When the TAP controller is in this state, it moves to either the Run-Test/Idle state if TMS is low, or the Select-DR-Scan state if TMS is high.

3.4. Test Access Port (TAP)

The Test Access Port (TAP) consists of the five signal pins: TRST_N, TDI, TDO, TMS and TCK. These pins control a test by communicating the serial test data and instructions.

As Figure 3.5 shows, data is serially scanned into one of the three registers (instruction register, bypass register or boundary scan register) on the TDI pin, or it is scanned out from one of these three registers on the TDO pin.

The TMS input controls the state transitions of the main TAP controller state machine. The TCK input is a special test clock that allows serial JTAG data to be shifted synchronously, independent of any chip-specific or system clocks.

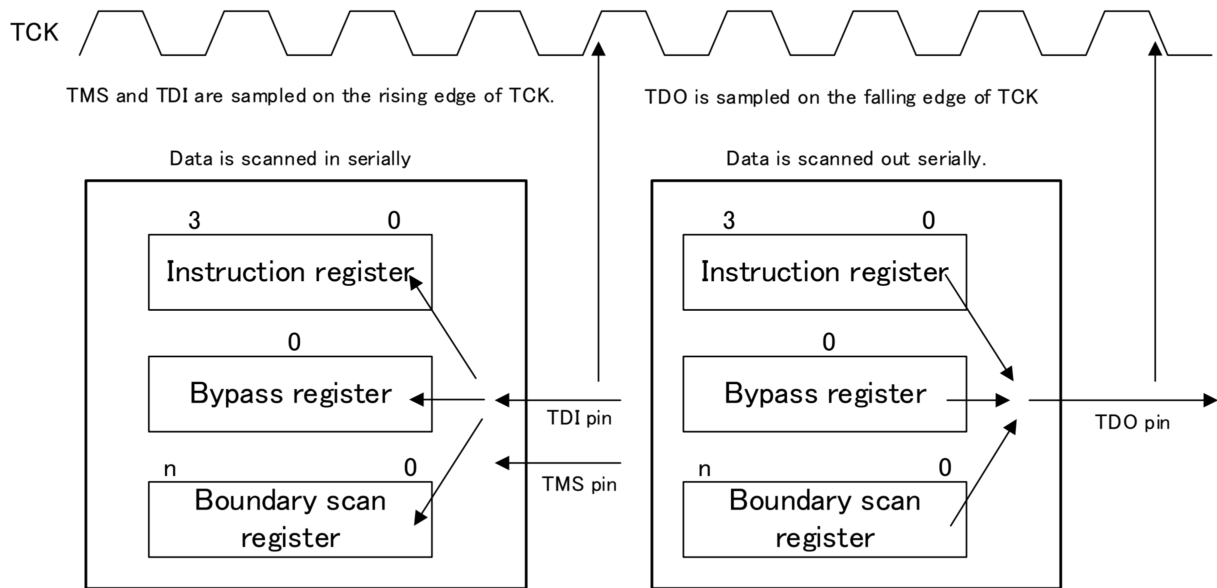

Figure 3.5 JTAG Test Access Port

Data on the TDI and TMS pins are sampled on the rising edge of the TCK input clock signal. Data on the TDO pin changes on the falling edge of the TCK clock signal.

3.5. Boundary Scan Order

Please refer the Reference Manual of "Product Information" about the boundary scan order.

4. Instructions Register Explanation

4.1. EXTEST instruction

The EXTEST instruction is used for external interconnect tests. The EXTEST instruction permits BSR cells at output pins to shift out test patterns in the Update-DR state and those at input pins to capture test results in the Capture-DR state.

Typically, before EXTEST is executed, the initialization pattern is shifted into the boundary scan register using the SAMPLE/PRELOAD instruction. If the boundary scan register is not reset, indeterminate data will be transferred in the Update-DR state and bus conflicts between ICs may occur. Figure 4.1. shows data flow when the EXTEST instruction is selected.

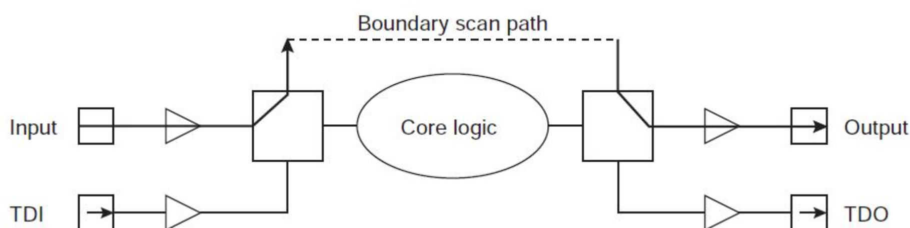

Figure 4.1 Test Data Flow when the EXTEST Instruction is selected

The following steps describe the basic test procedure of the external interconnect test.

1. Reset the TAP controller to the Test-Logic-Reset state.
2. Load the instruction register with the SAMPLE/PRELOAD instruction. This causes the boundary scan register to be connected between TDI and TDO.
3. Reset the boundary scan register by shifting certain data in.
4. Load the test pattern into the boundary scan register.
5. Load the instruction register with the EXTEST instruction.
6. Capture the data applied to the input pin into the boundary scan register.
7. Shift out the captured data while simultaneously shifting the next test pattern in.
8. Send out the test pattern in the boundary scan register at the output on the output pin.
9. Repeat steps 6 to 8 for each test pattern.

4.2. SAMPLE/PRELOAD instruction

This instruction targets the boundary scan register between TDI and TDO. As its name implies, the SAMPLE/PRELOAD instruction provides two functions.

SAMPLE allows the input and output pads of an IC to be monitored. While it does so, it does not disconnect the system logic from the IC pins. SAMPLE is executed in the Capture-DR state. It is mainly used to capture the values of the IC's I/O pins on the rising edge of TCK during normal operation. Figure 4.2 shows the flow of data for the SAMPLE phase of the SAMPLE/PRELOAD instruction.

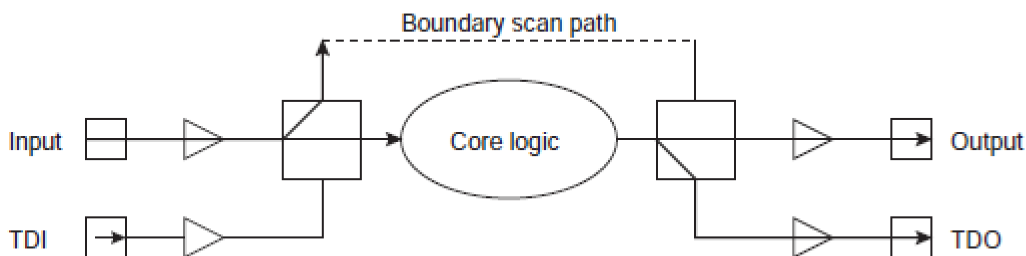

Figure 4.2 Test Data Flow while the SAMPLE is selected

PRELOAD allows the boundary scan register to be reset before any other instruction is selected. For example, prior to selection of the EXTEST instruction, PRELOAD is used to load reset data into the boundary scan register. PRELOAD permits data shifting of the boundary scan register without interfering with the normal operation of the system logic. Figure 4.3 shows the data flow for the PRELOAD phase of the SAMPLE/PRELOAD instruction.

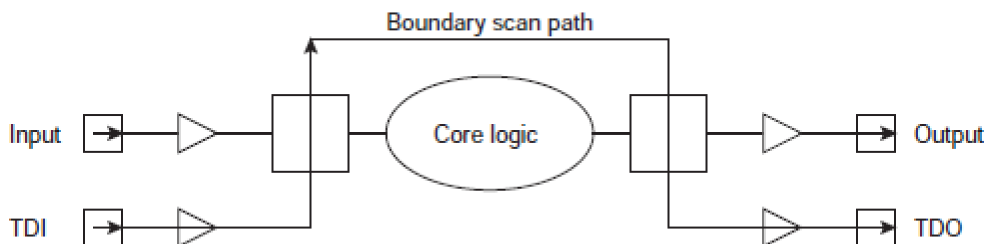

Figure 4.3 Test Data Flow while PRELOAD is selected

4.3. BYPASS instruction

This instruction targets the bypass register between TDI and TDO. The bypass register provides the shortest serial path that bypasses the IC (between TDI and TDO) when the test does not require control or monitoring of the IC. The BYPASS instruction does not cause interference in the normal operation of the on-chip system logic. Figure 4.4 shows the data flow through the bypass register when the BYPASS instruction is selected.

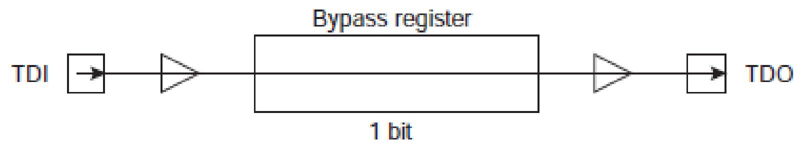

Figure 4.4 Test Data Flow when the BYPASS Instruction is selected

4.4. CLAMP instruction

The CLAMP instruction outputs the value that boundary scan register is programmed according to the PRELOAD instruction, and execute Bypass operation.

The CLAMP instruction selects the bypass register between TDI and TDO.

4.5. HIGHZ instruction

The HIGHZ instruction disables the output of the internal logical circuits. When the HIGHZ instruction is executed, it places the 3-state output pins in the high-impedance state.

The HIGHZ instruction also selects the bypass register between TDI and TDO.

5. Precaution

This section describes the cautions of the JTAG boundary-scan operations specific to the processor.

- The JTAG circuit can be released from the reset state by either of the following two methods:

  Assert TRST_N, initialize the JTAG circuit, and then deassertion TRST_N

  Supply the TCK signal for 5 or more clock pulses to TCK while pulling the TMS pin High.
- When switching a JTAG boundary scan test (behavior of BSC terminal is "1") and a NORMAL mode (behavior of BSC terminal is"0"), please start a power supply again.
- If TRST_N pin does not support, please input rising edge of TCK to a test logic reset 5 times in the condition of the "TMS=High".
- The BSC cannot use during an external reset period.

6. Revision History

Table 6.1 Revision History

Revision	Date	Description
1.0	2017-08-30	First release

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