32-bit RISC Microcontroller

TXZ Family

Reference Manual
Remote Control Signal Preprocessor (RMC-A)

Revision 2.0

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TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1], [XYZ2], [XYZ3]-> [XYZn]***
- "x" substitutes suffix number or character of two or more same kind of units and channels in same register name in the Register List.

  In case of unit, "x" means A, B, and C ..
  Example: ***[ADACR0], [ADBCR0], [ADCCR0]->[ADxCR0]***
  In case of channel, "x" means 0, 1, and 2..
  Example: [***T32A0RUNA], [T32A1RUNA], [T32A2RUNA]->[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***.EFG = 0x01 (hexadecimal), ***[XYZn]***.VW = 1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

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Terms and Abbreviations

Some of abbreviations used in this document are as follows:

RMC	Remote Control Signal Preprocessor
MAX	Maximum

1. Outline

Remote control signal preprocessor (hereafter referred to as RMC) receives a remote control signal of which carrier is removed. Please refer to a bottom for the list of functions.

Function Classification	Function	Operation
The reception of the remote control signal	Sampling clock	A sampling clock can be selected from either low speed clock (32.768kHz) or timer trigger for clock source.
	Noise filter	Noise canceling time can be adjusted. (15 phases)
	Leader detection	Detection is possible at the cycle of a reader, and a setup of Low width. >Without the leader in a state of the leader waiting. >Begin in leaders only for Low width. >Fixed phase method in a period.
	Data reception	A maximum of 72 bits of reception are possible. >Two kinds of data bit 0/1 judgments allow. (1) Judgment by the threshold setting. (2) Judgment by the falling edge interrupt.
	Interrupt	Generating of each remote control interruption(INTRMCx) is controllable. > Leader detection interrupt > Low width detection interrupt > Maximum data bit cycle interrupt > Falling edge interrupt

2. Block Diagram

Figure 2.1 shows the block diagram of RMC.

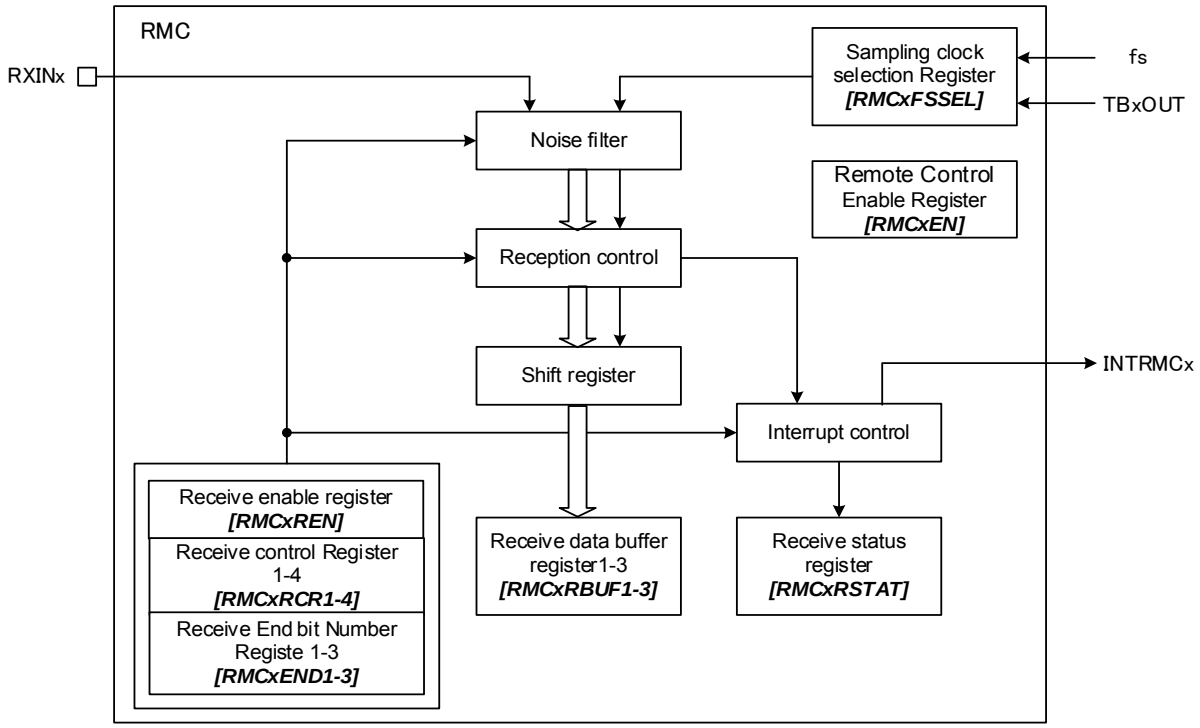

Figure 2.1 RMC block diagram

Table 2.1 List of signals

No.	Symbol	Signal name	I/O	Related Reference Manual
1	RXINx	Remote control data entry	Input	Product Information
2	fs	Low speed clock	Input	Clock Control and Operation Mode
3	TBxOUT	Timer trigger for clock source	Input	Product Information
4	INTRMCx	Remote control interrupt	Output	Exception

3. Function and Operation

3.1. Clock supply

When RMC is used, setting of system supply stop register of fsys / fc is unnecessary.
For the source clock, see Table 3.1.

Table 3.1 Source clock

Source clock	Supply setting
Low speed clock (fs)	Supply the low speed clock (fs). For details, refer to "Clock Control and Operation Mode" of the reference manual.
Timer trigger (TBxOUT)	Please set the clock supply according to the function of the connection destination. Refer to "Product Information" of the reference manual for details of connection destination.

3.2. Reception of Remote Control Signal

3.2.1. Sampling clock

A remote control signal is sampled by 32.768kHz low speed clock (fs) or a Timer trigger (TBxOUT). ***[RMCxFSSEL]***<RMCCLK> selects the sampling clock. When the sampling clock is changed by ***[RMCxFSSEL]*** <RMCCLK>, it should be checked that the remote control operation stops (is disabled; ***[RMCxREN]***<RMCREN> = 0). And ***[RMCxFSSEL]***<RMCCLK> should be set before setting any other registers which relate to the signal reception of the remote controller.

For the timer connected to TBxOUT, refer to “Product Information” in reference manual. When Low speed clock (fs) is used, fs clock should be enabled. For the details, refer to “Clock Control and Operation Mode” in reference manual.

The frequency of the input signal to TBxOUT should be in the range of 30 to 34 kHz.

3.2.2. Basic operation

As for the signal input by RXINx, a signal performed noise reduction of through a noise filter circuit is input into a reception control circuit.

If the leader is detected in the reception control circuit, ***[RMCxRSTAT]***<RMCRLDR> will set at the time of detection/interruption generating of the low width or the data bit cycle MAX. At this time, if you set the ***[RMCxRCR2]***<RMCLIEN>=1, leader detection will generate a leader detection interrupt. When a leader detection interrupt occurs,***[RMCxRSTAT]***<RMCRLIF> is set. The 0/1 judgment of the data bit is performed one by one after reader detection, and the a maximum of 72 bits of results are stored in the shift register. If it is set as ***[RMCxRCR2]***<RMCEDIEN> =1, the remote control input falling edge interrupt will occur for every falling edge of the data bit. ***[RMCxRSTAT]***<RMCEDIF> is set to remote control input falling edge interruption developmental time.

Reception operation is ended by detection of the maximum data bit cycle, and detection of the Low width of the preset value, and is transmitted to ***[RMCxRBUF1]***, ***[RMCxRBUF2]*** and ***[RMCxRBUF3]*** register from the shift register, and the interrupt generates it. Only when ***[RMCxEND1]***< RMCEND1>, ***[RMCxEND2]***<RMCEND2>, or ***[RMCxEND3]***<RMCEND3> register is set up and the received bit number is in agreement (to the low width detection or the maximum data bit cycle detection), interruption is generated.

Receiving the data is continued when the waveform which fulfills the conditions of the reception end is not inputted, even if it receives the data of 73 bits or more. In this case, the contents of the data buffer are not guaranteed.

To check the status of RMC if reception is completed, read the receive status register(***[RMCxRSTAT]***).

On completion of reception, RMC is waiting for the next leader.

When the setup which receives the remote control signal of only the data bit is carried out, detection of the leader is not carried out but receives as the data from the beginning.

Before reading the received data, the receive data is written and replaced after ending the next reception.

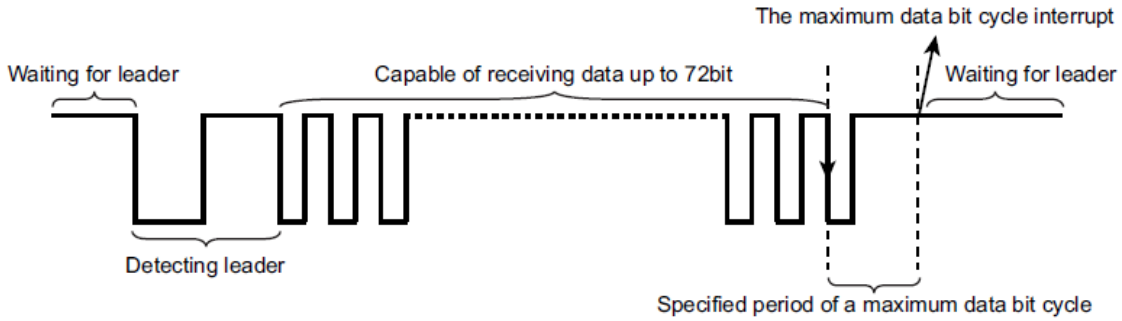

Figure 3.1 Data reception completes by detecting the maximum data bit cycle

3.2.3. Preparation

Before starting receiving process, configure how to receive remote control signal using the Receive Control Registers (***[RMCxRCR1]***, ***[RMCxRCR2]***, ***[RMCxRCR3]***, and ***[RMCxRCR4]***).

3.2.3.1. Settings of Noise Cancelling Time

Configure noise cancelling time with the ***[RMCxRCR4]***<RMCNC[3:0]>.

Noise canceling is applied to remote control signals sampled by the sampling clock.

RMC monitors a sampled remote control signal in each rising edge of a sampling clock. If "High" is monitored, RMC recognizes that the signal was changed to "Low" after monitoring cycles of "Low" specified in <RMCNC>. If "Low" is monitored, RMC recognizes that the signal was changed to "High" after monitoring cycles of "High" specified in <RMCNC>.

The following figure shows how RMC operates according to the noise cancel setting of <RMCNC[3:0]> = 0011 (3 cycles). Subsequent to noise cancellation, the signal is changed from "High" to "Low" upon monitoring 3 cycles of "Low", and the signal is changed from "Low" to "High" upon monitoring 3 cycles of "High".

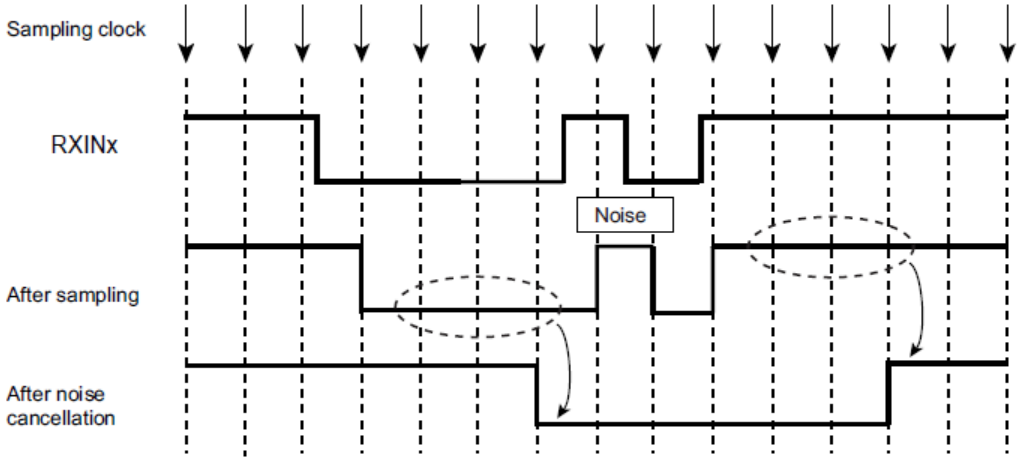

Figure 3.2 Noise Cancel (In the case of *[RMCxRCR4]*<RMCNC[3:0]>=0011 (3Cycles))

3.2.3.2. Settings of Detecting Leader

Set the leader cycle and a "Low" width of the leader to ***[RMCxRCR1]***<RMCLLMIN[7:0]> <RMCLLMAX[7:0]> <RMCLCMIN[7:0]> <RMCLCMAX[7:0]>. When you configure those above, follow the rule shown below.

Table 3.2 Leader and Rules

Leader	Rules
"Low" width + "High" Width	<RMCLCMAX[7:0]> > <RMCLCMIN[7:0]> <RMCLLMAX[7:0]> > <RMCLLMIN[7:0]> <RMCLCMIN[7:0]> > <RMCLLMAX[7:0]>
Only "High" width	<RMCLCMAX[7:0]> > <RMCLCMIN[7:0]> <RMCLLMAX[7:0]> = 0x00 <RMCLLMIN[7:0]> = don't care
No leader	<RMCLCMAX[7:0]> = 0x00 <RMCLCMIN[7:0]> = don't care <RMCLLMAX[7:0]> = don't care <RMCLLMIN[[7:0]> = don't care

Note: For “Low width only”, ***[RMCxRCR4]***<RMCPO> = 1 should be set.

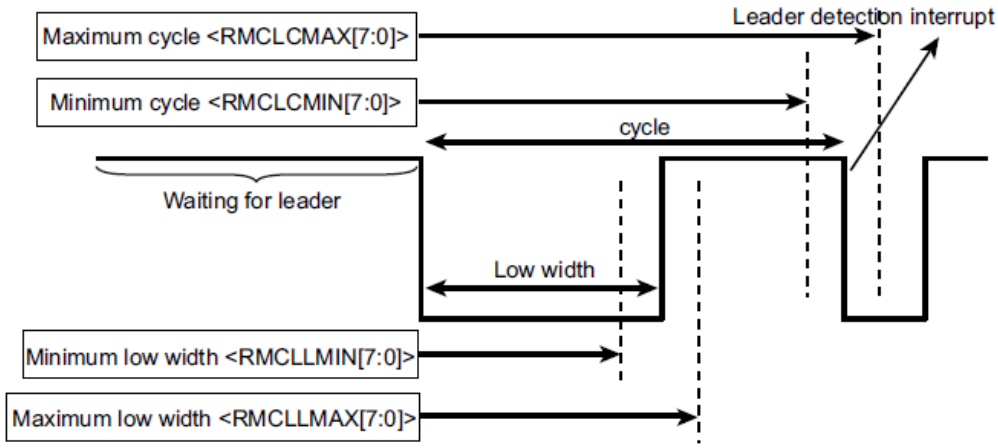

Figure 3.3 Leader wave form and the *[RMCxRCR1]* register settings

If you want to generate an interrupt when detecting a leader, configure the ***[RMCxRCR2]***<RMCLIEN>.
A remote control signal without a leader cannot generate a leader detection interrupt.

3.2.3.3. Setting of 0/1 determination data bit

Based on a falling edge cycle, the data bit of a cycle modulation is determined as 0 or 1.

There are two kinds of determinations:

As for data bit determination of a remote control signal in a phase method, see "3.2.9 Receving a Remote Control Signal in a Phase Method".

1. Determination by threshold.

   Configure a threshold value to ***[RMCxRCR3]***<RMCDATL[6:0]> which determines data bit as "0" or "1". If the determination value is equal to threshold value or more, it is determined as "1". If the determination value is less than threshold value, it is determined as "0".

2. Determination by falling edge interrupt inputs.

   By setting "1" to the ***[RMCxRCR2]***<RMCEDIEN>, a remote control signal input falling edge interrupt can be generated in each falling edge of the data bit. Using this interrupt together with a timer enables the determination to be done by software.

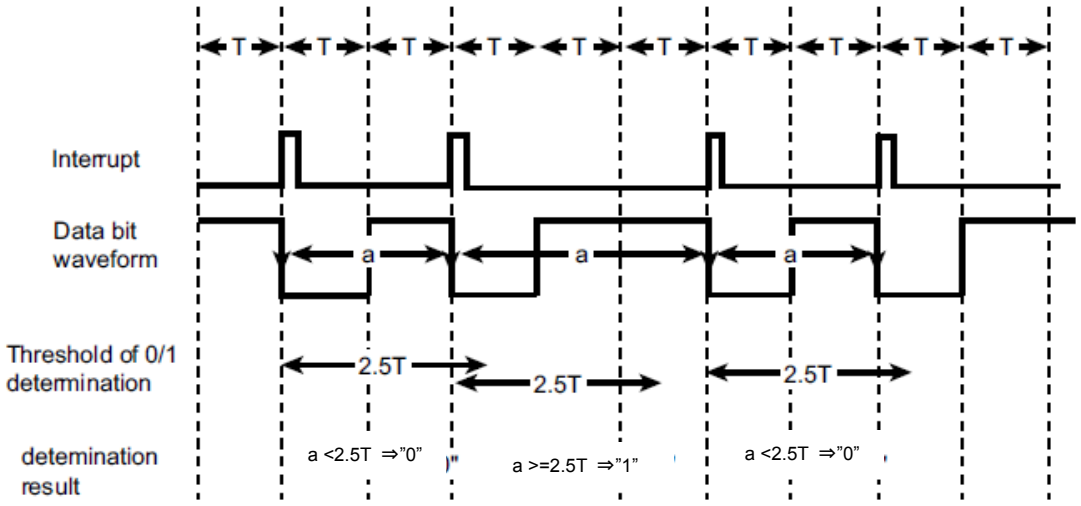

Figure 3.4 Determination method of data bit (In case that threshold is 2.5T)

3.2.3.4. Settings of Reception Completion

To complete data reception, settings of detecting the maximum data bit cycle and "Low" width are required. If multiple factors are specified, reception is completed by the factor detected first. Make sure to configure the reception completion settings.

(1) Completion by the maximum data bit cycle

To complete reception by detecting a maximum data bit cycle, you need to configure the ***[RMCxRCR2]*** <RMCDMAX[7:0]>.

If the falling edge of the data bit cycle isn't monitored after time specified as threshold in the <RMCDMAX[7:0]>, a maximum data bit cycle is detected. The detection completes reception and generates an interrupt. After interrupt inputs generated, ***[RMCxRSTAT]***<RMCDMAXIF > is set to "1".

To generate interrupt by setting the number of receive data is set a ***[RMCxEND1 to 3]*** register of each <RMCEND1>, <RMCEND2>, <RMCEND3>. In this case when the number of set reception bit agreed with the number of bit which received at the time of the outbreak of MAX on the number of receive data is set a ***[RMCxEND1 to 3]*** register of each <RMCEND1>, <RMCEND2>, <RMCEND3>, it occurs by an MAX interrupt in data bit period.

As specified to ***[RMCxEND1 to 3]***, it is able to set three kinds of the receive data bit.
When it can receive the Maximum Data bit , the number of bit is not match the setting value in <RMCEND1>, <RMCEND2>, <RMCEND3>, the interrupt does not occur , it wait for Leader Reception.

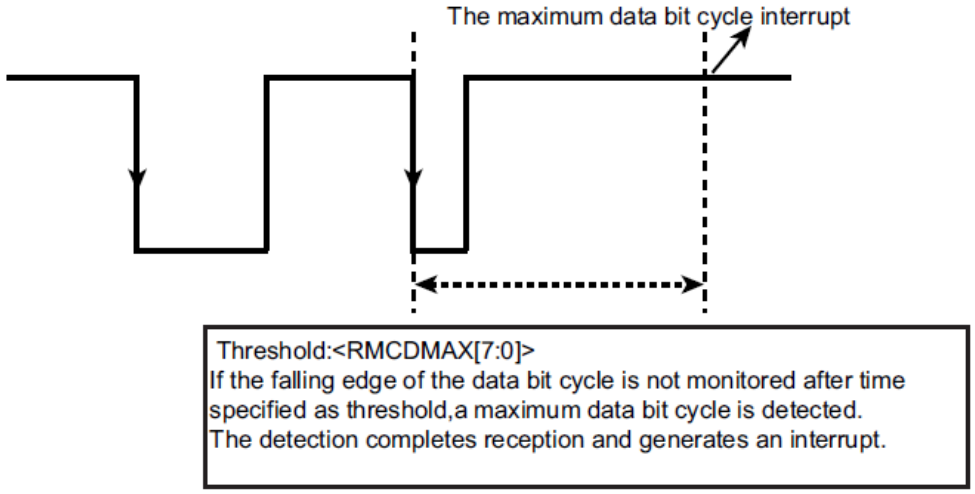

Figure 3.5 Reception completion by detecting a maximum data bit cycle

(2) Completion by detecting "Low" width

To complete reception by detecting the "Low" width, you need to configure the ***[RMCxRCR2]*** <RMCLL[7:0]>.
After the falling edge of the data bit is detected, if the signal stays "Low" longer than specified, excess "Low" width is detected. The detection completes reception and generates an interrupt.

After interrupt inputs generated, ***[RMCxRSTAT]***<RMCLOIF> is set to "1".

To generate interrupt by setting the number of receive data is set a ***[RMCxEND1 to 3]*** register of each <RMCEND1>, <RMCEND2>, <RMCEND3>. In this case when the number of set reception bit agreed with the number of bit which received at the time of the outbreak of the low width detection on the number of receive data is set a ***[RMCxEND1 to 3]*** register of each <RMCEND1>, <RMCEND2>, <RMCEND3>, it occurs by the low width detection interrupt.

As specified to ***[RMCxEND1 to 3]***, it is able to set three kinds of the receive data bit.
When it can receive the Low width detection, the number of bit is not match the setting value in <RMCEND1>, <RMCEND2>, <RMCEND3>, the interrupt does not occur , it wait for Leader Reception.

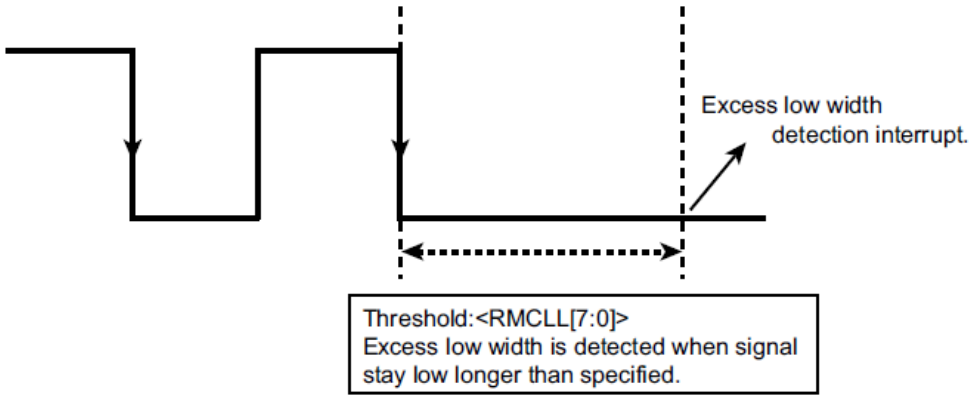

Figure 3.6 Completion by detecting "Low" width

3.2.4. Enabling Reception

By enabling the ***[RMCxREN]***<RMCREN> after configuring the ***[RMCxRCR1]***,***[RMCxRCR2]***,***[RMCxRCR3]*** and ***[RMCxRCR4]*** registers, RMC is ready for reception. Detecting a leader initiates reception.

Note: Changing the configurations of the ***[RMCxRCR1]***,***[RMCxRCR2]***,***[RMCxRCR3]*** and ***[RMCxRCR4]*** registers during reception may harm their proper operation. Be careful if you change them during reception.

3.2.5. Stopping Reception

RMC stops reception by clearing the ***[RMCxREN]***<RMCREN> to "0" (reception disabled).
Clearing this bit during reception stops reception immediately and the received data is discarded.

3.2.6. Interrupt

RMC has four kinds of interrupt factors.
Each interrupt factor is summarized in one signal and is output as remote control interrupt (INTRMCx).
About the interrupt factor, please confirm an applicable bit in reception status register (***[RMCxRSTAT]***).

Table 3.3 Interrupt factor and register

interrupt factor	Receive Control Register 2 (***[RMCxRCR2]***)	Receive Status Register (***[RMCxRSTAT]***)
Leader detection interrupt	<RMCLIEN>	<RMCRLIF>
Falling edge interrupt	<RMCEDIEN>	<RMCEDIF>
Maximum data bit cycle interrupt	-	<RMCDMAXIF>
Low width detection interrupt	-	<RMCLOIF>

3.2.6.1. Leader detection interrupt

An interrupt to occur when a leader is detected.
The outbreak of the interrupt can choose permission / prohibition in the receive control register 2 (***[RMCxRCR2]***<RMCLIEN>).
Generating of interruption can be checked by a receive status register (***[RMCxRSTAT]***<RMCLOIF>).

3.2.6.2. Falling edge interrupt

It is interruption which occurs for every falling edge of a data bit after reader detection.
The outbreak of the interrupt can choose permission / prohibition in the receive control register 2 (***[RMCxRCR2]***<RMCLIEN>).
Generating of interruption can be checked by a receive status register (***[RMCxRSTAT]***<RMCLOIF>).

3.2.6.3. Maximum data bit cycle interrupt

It is interruption which will occur if the time more than the threshold (***[RMCxRCR2]***<RMCDMAX [7:0]>) of the maximum data bit cycle set up by the receive control register 2 is detected. Moreover, when ***[RMCxEND1]***, ***[RMCxEND2]***, and ***[RMCxEND2]*** is set up, interruption will be generated if in agreement with the bit number received at the time of generating of the data bit cycle MAX.
Generating of interruption can be checked by a receive status register (***[RMCxRSTAT]***<RMCLOIF>).

3.2.6.4. Low width detection interrupt

It is interruption which will occur if the time more than the Low width set up by the receive control register 2 (***[RMCxRCR2]***<RMCLL [7:0]>) is detected after falling of a data bit. Moreover, when ***[RMCxEND1]***, ***[RMCxEND2]***, and ***[RMCxEND3]*** is set up, interruption will be generated if in agreement with the bit number received at the time of generating of the low width detection.

Generating of interruption can be checked by a receive status register (***[RMCxRSTAT]***<RMCLOIF>).

Please see a remote control wave pattern and the relations of the interrupt in Figure 3.7.

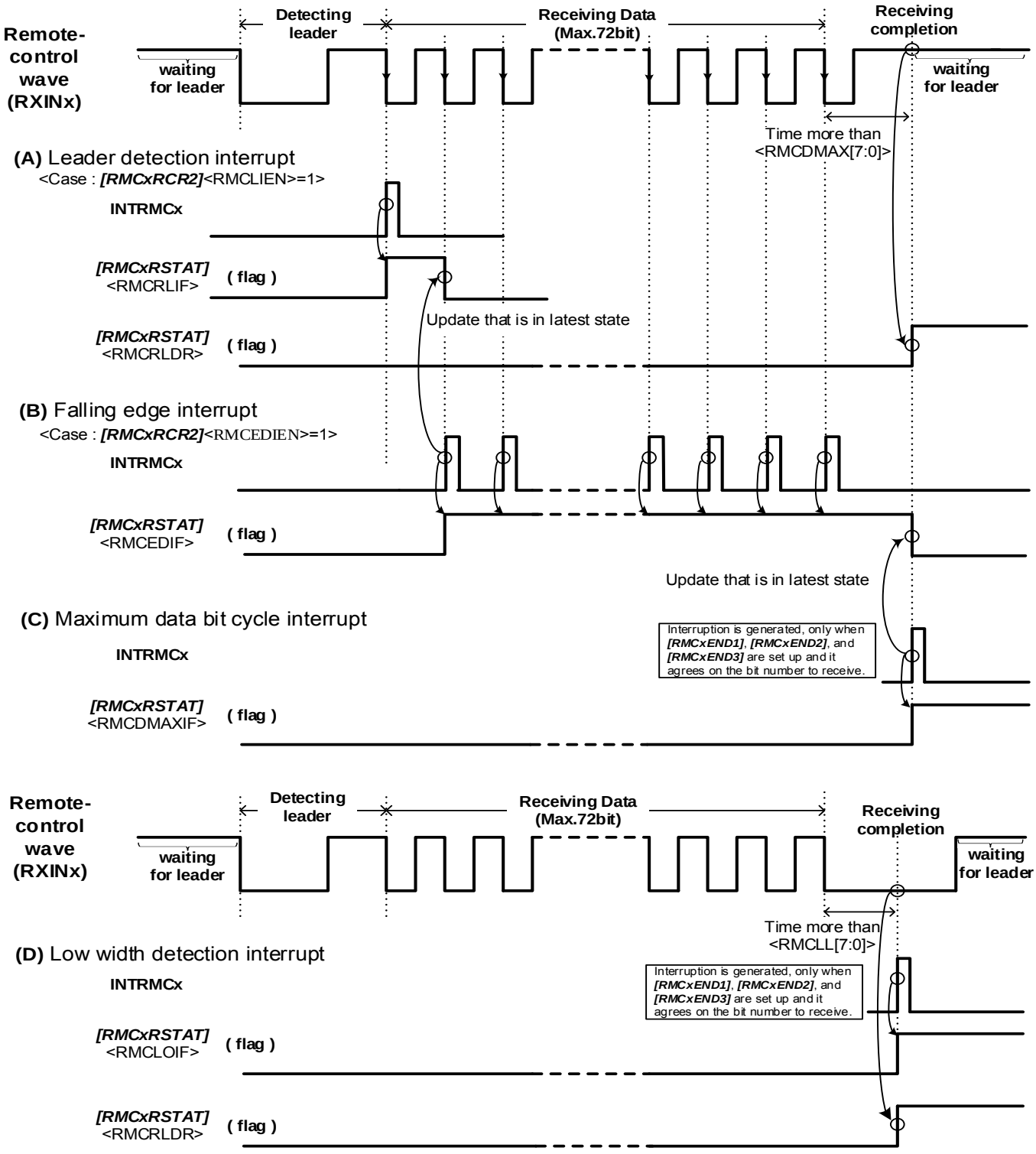

Figure 3.7 A remote control wave pattern and the relations of the interrupt

3.2.7. Receiving Remote Control Signal without Leader in Waiting Leader

Setting ***[RMCxRCR2]***<RMCLD> enables RMC to receive signals with and without a leader.

By setting ***[RMCxRCR2]***<RMCLD>=1, RMC starts receiving data if the signal of which Low width is shorter than the set Low width in the ***[RMCxRCR1]***<RMCLLMIN[7:0]>. RMC keeps receiving data until the final data bit is received.

If ***[RMCxRCR2]***<RMCLD> is enabled, the same settings of error detection, reception completion and data bit determination of 0 or 1 are applied regardless of whether a signal has a leader or not.

Thus receivable remote control signals are limited.

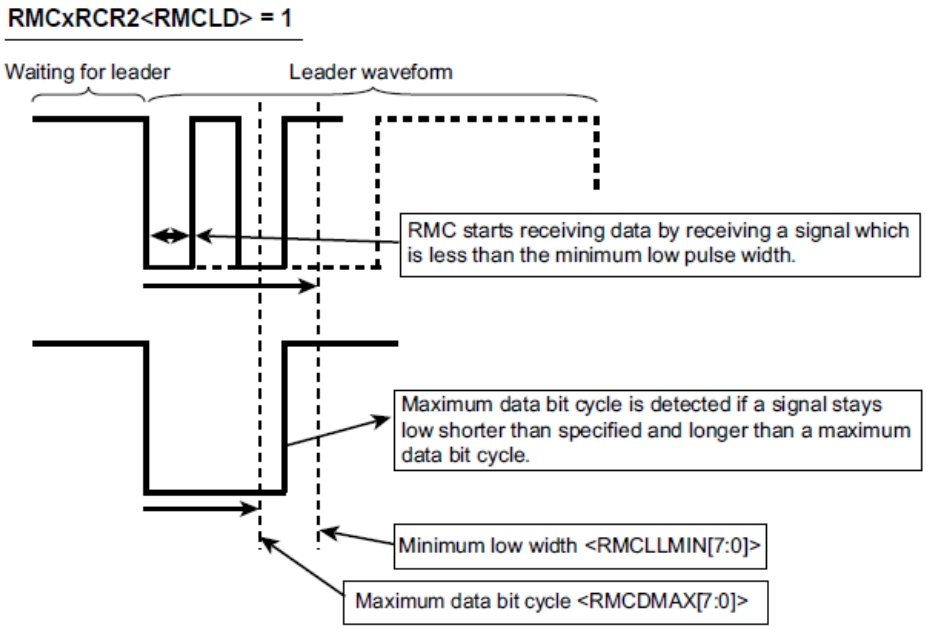

Figure 3.8 Receiving Remote Control Signal without Leader in Waiting Leader (In the case of *[RMCxRCR2]*<RMCLD>=1)

3.2.8. A Leader only with "Low" Width

Figure 3.9 shown below illustrates a remote control signal that starts with a leader of which waveform only has "Low" width.

This signal starts with a leader that only has "Low" width and a data bit cycle starts from the rising edge. To enable the signal, it must be sent after being reversed by setting the ***[RMCxRCR4]***<RMCPO> to "1".

This is because RMC is configured to detect a data bit cycle from the falling edge.

To detect a leader, configure only "Low" pulse width of the leader with the <RMCLLMAX[7:0]>=0x00, <RMCLCMAX[7:0]> > <RMCLCMIN[7:0]>.

In this case, the value of <RMCLLMIN[7:0]> is set as "don't care".
To detect whether data "0" or data "1", configure the threshold of 0/1 detection with the ***[RMCxRCR3]*** <RMCDATL[6:0]>.

To complete data reception, configure the "Low" pulse width detection with <RMCLL[7:0]>.

A reception end / interrupt occurs after confirming the Low period set after the last bit, and the reader waits.

The RMC generates an interrupt and waits for the next leader.

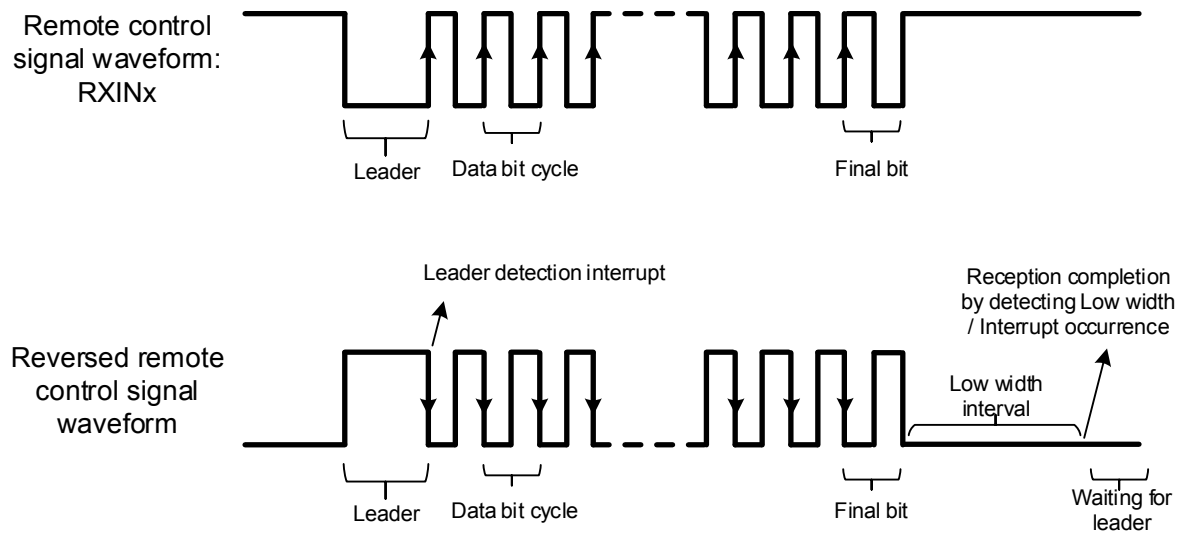

Figure 3.9 A Leader only with "Low" Width

3.2.9. Receiving a Remote Control Signal in a Phase Method

RMC is capable of receiving a remote control signal in a phase method of which signal cycle is fixed.
A signal in the phase method has three waveform patterns (see the figure shown below).

By setting two thresholds a remote control signal pattern is determined. RMC converts the signal into data "0" or "1". On completion of reception, received data "0" and "1" are stored in the ***[RMCxRBUF1]***, ***[RMCxRBUF2]*** and ***[RMCxRBUF3]***.

By setting ***[RMCxRCR2]***<RMCPHM> = 1, RMC enables to receive a remote control signal in the phase method. Each threshold can be configured with the ***[RMCxRCR3]***<RMCDATL[6:0]> and <RMCDATH[6:0]>.

Two thresholds are used to distinguish three waveform patterns. On condition that a cycle between two falling edges is "T", three patterns show cycles of 1T, 1.5T and 2T. Details of the two thresholds are shown in Figure 3.10.

Table 3.4 Threshold and Determined by pattern

	Determined by	Threshold	Register bits to set
Threshold1	Pattern1 & pattern2	1T to 1.5T	***[RMCxRCR3]***<RMCDATL[6:0]>
Threshold2	Pattern2 & pattern3	1.5T to 2T	***[RMCxRCR3]***<RMCDATH[6:0]>

In the discrimination of the stationary fixed-phase remote control signal, three patterns of data change and the data of the immediately preceding period of the judgment pattern are necessary. The phase-type signal should start with data “11”.

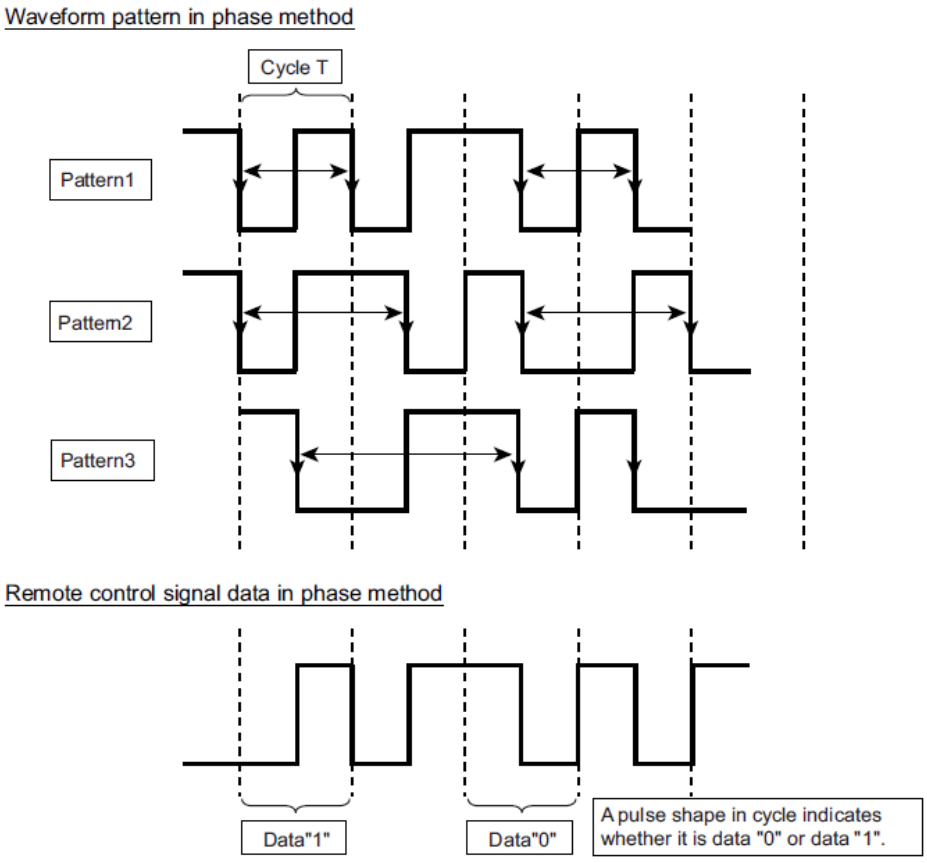

Figure 3.10 Waveform pattern in phase method and the example of data

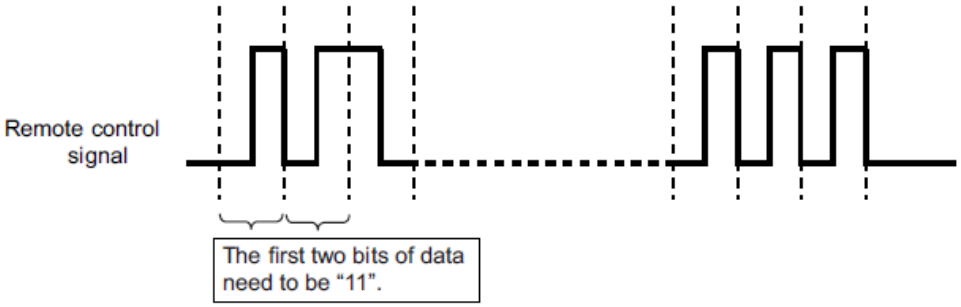

Figure 3.11 The waveform pattern in phase method

4. Registers

4.1. Register List

Addresses and names of RMC control registers are shown below.

Table 4.1 Registers and Address

Peripheral	Function Name	Channel/Unit	Base Address	
			TYPE 1	TYPE 2
Remote Control Signal Preprocessor	RMC	ch 0	0x400E7000	0x400E8100

Note: The Channel/Unit and Base address type are different by products. Please refer to "Product Information" of the reference manual for the details.

Register Name		Address(Base+)
Remote Control Enable Register	***[RMCxEN]***	0x0000
Receive Enable Register	***[RMCxREN]***	0x0004
Receive Data Buffer Register 1	***[RMCxRBUF1]***	0x0008
Receive Data Buffer Register 2	***[RMCxRBUF2]***	0x000C
Receive Data Buffer Register 3	***[RMCxRBUF3]***	0x0010
Receive Control Register 1	***[RMCxRCR1]***	0x0014
Receive Control Register 2	***[RMCxRCR2]***	0x0018
Receive Control Register 3	***[RMCxRCR3]***	0x001C
Receive Control Register 4	***[RMCxRCR4]***	0x0020
Receive Status Register	***[RMCxRSTAT]***	0x0024
Receive End bit Number Register 1	***[RMCxEND1]***	0x0028
Receive End bit Number Register 2	***[RMCxEND2]***	0x002C
Receive End bit Number Register 3	***[RMCxEND3]***	0x0030
Sampling Clock selection Register	***[RMCxFSSEL]***	0x0034

4.2. Details of Registers

4.2.1. *[RMCxEN]* (Remote Control Enable Register)

Bit	Bit Symbol	After reset	Type	Function
31:2	-	0	R	Read as “0”.
1	-	0	R/W	Write as "1".
0	RMCEN	0	R/W	Controls RMC operation. 0: Disabled 1: Enabled Operation of a remote control judging function is controlled. To allow RMC to function, enable the <RMCEN> first. If RMC is enabled and then disabled, the settings in each register remain intact.

4.2.2. *[RMCxREN]* (Receive Enable Register)

Bit	Bit Symbol	After reset	Type	Function
31:1	-	0	R	Read as “0”.
0	RMCREN	0	R/W	Reception 0: Disabled 1: Enabled Controls reception of RMC. Setting this bit to "1" enables reception.

Note: Enable the ***[RMCxREN]***<RMCREN> bit after setting the ***[RMCxRCR1]***, ***[RMCxRCR2]***, ***[RMCxRCR3],***and ***[RMCxRCR4]***.

4.2.3. *[RMCxRBUF1]* (Receive Data Buffer Register 1)

Bit	Bit Symbol	After reset	Type	Function
31:0	RMCRBUF[31:0]	0x00000000	R	Received data (31 to 0 bit) Reads 4 bytes of received data. (31 to 0 bit)

4.2.4. *[RMCxRBUF2]* (Receive Data Buffer Register 2)

Bit	Bit Symbol	After reset	Type	Function
31:0	RMCRBUF[63:32]	0x00000000	R	Received data (63 to 32 bit) Reads 4 bytes of received data. (63 to 32 bit)

4.2.5. *[RMCxRBUF3]* (Receive Data Buffer Register 3)

Bit	Bit Symbol	After reset	Type	Function
31:8	-	0	R	Read as “0”.
7:0	RMCRBUF[71:64]	0x00	R	Received data (71 to 64 bit). Reads 1 byte of received data. (71 to 64 bit).

Note: The received bit is stored in the data buffer register in MSB first order, and the last received bit is stored in the LSB (bit 0). If the remote control signal is received in the LSB first algorithm, the received data is stored in reverse sequence.

4.2.6. *[RMCxRCR1]* (Receive Control Register 1)

Bit	Bit Symbol	After reset	Type	Function
31:24	RMCLCMAX[7:0]	0x00	R/W	Specifies a maximum cycle of leader detection. Calculating formula of the maximum cycle: <RMCLCMAX> × 4/fs [s]. (Note1)
23:16	RMCLCMIN[7:0]	0x00	R/W	Specifies a minimum cycle of leader detection. Calculating formula of the minimum cycle: <RMCLCMIN> × 4/fs [s]. (Note1)
15:8	RMCLLMAX[7:0]	0x00	R/W	Specifies a maximum "Low" width of leader detection. Calculating formula of the maximum "Low" width: <RMCLLMAX> × 4/fs [s] (Note1)
7:0	RMCLLMIN[7:0]	0x00	R/W	Specifies a minimum "Low" width of leader detection. Calculating formula for the minimum "Low" width: <RMCLLMIN> × 4/fs [s] (Note1) When ***[RMCxRCR2]***<RMCLD>=1, a value of the "Low" pulse width is less than the specified value, it is defined as data bit.

Note1: The calculating formula a sampling clock in the case of fs.

In the case of TBxOUT, please replace fs of the calculating formula with a frequency of TBxOUT.

Note2: When you configure the register, you must follow the rule shown below.

Leader	Rules
"Low" width + "High" width	<RMCLCMAX[7:0]> > <RMCLCMIN[7:0]> <RMCLLMAX[7:0]> > <RMCLLMIN[7:0]> <RMCLCMIN[7:0]> > <RMCLLMAX[7:0]>
Only "High" width	<RMCLCMAX[7:0]> > <RMCLCMIN[7:0]> <RMCLLMAX[7:0]> = 0x00 <RMCLLMIN[7:0]> = don't care
No Leader	<RMCLCMAX[7:0]> = 0x00 <RMCLCMIN[7:0]> = don't care <RMCLLMAX[7:0]> = don't care <RMCLLMIN[[7:0]> = don't care

4.2.7. *[RMCxRCR2]* (Receive Control Register 2)

Bit	Bit Symbol	After reset	Type	Function
31	RMCLIEN	0	R/W	Leader detection interrupt 0: Not generated 1: Generated
30	RMCEDIEN	0	R/W	Remote control input falling edge interrupt 0: Not generated 1: Generated
29:26	-	0	R	Read as “0”.
25	RMCLD	0	R/W	Receiving remote control signal with and without a leader 0: Disabled 1: Enabled
24	RMCPHM	0	R/W	Receiving a remote control signal by a phase modulation 0: Not receiving a remote control signal by a phase modulation. (receive by a cycle modulation) 1: Receive remote control signal by a fixed frequency pulse modulation.
23:16	-	0	R	Read as “0”.
15:8	RMCLL[7:0]	0xFF	R/W	Excess "Low" width that triggers reception completion and interrupt generation. 0x00 to 0xFE: Reception completion and interrupt generation at <RMCLL> × 1/fs [s]. (Note1) 0xFF: not to use as the trigger. (Note2)
7:0	RMCDMAX[7:0]	0xFF	R/W	Maximum data bit cycle that triggers reception completion and interrupt generation. 0x00 to 0xFE: Reception completion and interrupt generation at <RMCDMAX> × 1/fs [s]. (Note1) 0xFF: not to use as the trigger. (Note2)

Note1: The calculating formula a sampling clock in the case of fs. In the case of TBxOUT, please replace fs of the calculating formula with a frequency of TBxOUT.

Note2: If ***[RMCxEND1]***<RMCEND1>***[RMCxEND2]***<RMCEND2>***[RMCxEND3]***<RMCEND3> are set, the interrupt is generated only when the reception bit count matches one of the set values.

4.2.8. *[RMCxRCR3]* (Receive Control Register 3)

Bit	Bit Symbol	After reset	Type	Function
31:15	-	0	R	Read as “0”.
14:8	RMCDATH[6:0]	0x00	R/W	Larger threshold to determine a signal pattern in a phase method Calculating formula of the threshold: <RMCDATH> × 1/fs [s] (Note1) (Note2) Specifies a larger threshold (within a range of 1.5T and 2T) to determine a pattern of remote control signal in a phase method. (Note3)
7	-	0	R	Read as “0”.
6:0	RMCDATL[6:0]	0x00	R/W	Threshold to determine 0 or 1 smaller threshold to determine a signal pattern in a phase method. Calculating formula of the threshold: <RMCDATL> × 1/fs [s] (Note1) Specifies two kinds of thresholds: a threshold to determine whether a data bit is 0 or 1; a smaller threshold (within a range of 1T and 1.5T) to determine a pattern of remote control signal in a phase method. (Note4)

Note1: The calculating formula a sampling clock in the case of fs. In the case of TBxOUT, please replace fs of the calculating formula with a frequency of TBxOUT.

Note2: This function is valid only when ***[RMCxRCR2]***<RMCPHM> = 1.

Note3: If the measurement result of the data bit is equal to or larger than the threshold value, the data is judged as “10”. If, less than the threshold, “01”.

Note4: In 0/1 judgment of a data bit, if the data bit is equal or larger than the threshold value, the data is judged as “1”, and if, less than the threshold value, “0”.

In the judgment of 3 kinds of data bit in the phase-type remote control signal, if the data bit is equal to or larger than the threshold value, the data is judged as “01”. If, less than the threshold, “00”.

4.2.9. *[RMCxRCR4]* (Receive Control Register 4)

Bit	Bit Symbol	After reset	Type	Function
31:8	-	0	R	Read as “0”.
7	RMCPO	0	R/W	Remote control input signal selection. 0: Not invert 1: Invert
6:4	-	0	R	Read as “0”.
3:0	RMCNC[3:0]	0x0	R/W	Specifies noise cancellation time. 0x0: No cancellation 0x1 to 0xF: cancellation Calculating formula of noise cancellation time: <RMCNC> × 1/fs [s] (Note1)

Note: The calculating formula a sampling clock in the case of fs.

In the case of TBxOUT, please replace fs of the calculating formula with a frequency of TBxOUT.

4.2.10. *[RMCxRSTAT]* (Receive Status Register)

Bit	Bit Symbol	After reset	Type	Function
31:16	-	0	R	Read as “0”.
15	RMCRLIF	0	R	Interrupt source flag 0: No leader detection interrupt generated. 1: Leader detection interrupt generated.
14	RMCLOIF	0	R	Interrupt source flag 0: No "Low" width detection interrup generated. 1: "Low" width detection interrupt generated.
13	RMCDMAXIF	0	R	Interrupt source flag 0: No maximum data bit cycle interrupt generated. 1: Maximum data bit cycle interrupt generated.
12	RMCEDIF	0	R	Interrupt source flag 0: No falling edge interrupt generated. 1: Falling edge interrupt generated.
11:8	-	0	R	Read as “0”.
7	RMCRLDR	0	R	Leader detection 0: Disable leader detection. 1: Enable leader detection.
6:0	RMCRNUM[6:0]	0x00	R	The number of received data bit 0x00: no data bit (only with leader) 0x01 to 0x48: 1 to 72bit 0x49 to 0xFF: 73bit and more Indicates the number of bits received as remote control signal data. (Note2)

Note1: The fields except <RMCRNUM[6:0]> are updated (set or cleared) by each interrupt factor generation, the leader detection, the repeat code detection, and the reception completion, respectively.

Note2: <RMCRNUM[6:0]> is updated after the reception completion. The received data bit count cannot be monitored during the reception.

4.2.11. *[RMCxEND1]* (Receive End bit Number Register 1)

Bit	Bit Symbol	After reset	Type	Function
31:7	-	0	R	Read as “0”.
6:0	RMCEND1[6:0]	0x00	R/W	Specifies that the number of receive data bit 0x00: No specifically the receive data bit 0x01 to 0x48: Specifies that the number of receive data bit(1 to 72bit) 0x49 to 0xFF: Don’t set the value

4.2.12. *[RMCxEND2]* (Receive End bit Number Register 2)

Bit	Bit Symbol	After reset	Type	Function
31:7	-	0	R	Read as “0”.
6:0	RMCEND2[6:0]	0x00	R/W	Specifies that the number of receive data bit 0x00: No specifically the receive data bit 0x01 to 0x48: Specifies that the number of receive data bit(1 to 72bit) 0x49 to 0xFF: Don’t set the value

4.2.13. *[RMCxEND3]* (Receive End bit Number Register 3)

Bit	Bit Symbol	After reset	Type	Function
31:7	-	0	R	Read as “0”.
6:0	RMCEND3[6:0]	0x00	R/W	Specifies that the number of receive data bit 0x00: No specifically the receive data bit 0x01 to 0x48: Specifies that the number of receive data bit(1 to 72bit) 0x49 to 0xFF: Don’t set the value

Note1: If all of <RMCEND1>,<RMCEND2>,<RMCEND3> are set to “0x00”, an interrupt (the maximum data bit cycle detection and the Low width detection) is generated regardless of the reception bit count.

Note2: An interrupt is generated only when the reception bit count matches one of ***[RMCxEND1], [RMCxEND2],[RMCxEND3]*** at the reception completion. If the register values do not match the count, no interrupt is generated. ***[RMCxEND1]***,***[RMCxEND2]***,***[RMCxEND3]*** can be set to different values, respectively.

4.2.14. *[RMCxFSSEL]* (Sampling Clock selection Register)

Bit	Bit Symbol	After reset	Type	Function
31:1	-	0	R	Read as “0”.
0	RMCCLK	0	R/W	Specifies that Sampling clock of RMC function 0: Low speed Clock (32.768kHz) 1: Timer trigger (TBxOUT) For the Sampling of RMC function, It is able to set the Low speed Clock (32.768kHz) or Timer output (TBxOUT). For the information of TBxOUT use for sampling clock, refer to reference manual "Product Information". The Setting range of Timer output by TBxOUT is from 30 to 34kHz.

Note1: To Change the sampling clock by using the ***[RMCxFSSEL]***, disable the RMC operation first by using the ***[RMCxEN]*** <RMCEN>. Then, enable it again, and set the ***[RMCxFSSEL]*** before setting other RMC registers.

Note2: The RMC can be stopped (disabled) by ***[RMCxEN]***<RMCEN>. Then the circuit is started up (enabled) again. When the sampling clock is changed, it should be checked that the RMC is stopped (disabled). Then, the setting of ***[RMCxFSSEL]*** <RMCCLK> should be done before the other related registers are set.

5. Precautions

- The timer trigger (TBxOUT) for Clock source cannot be selected as the sampling clock in some products. For the details, refer to “Product Information” in reference manual.

6. Revision History

Table 6.1 Revision History

Revision	Date	Description
1.0	2017-09-08	First release
2.0	2018-03-02	1. Outline Corrected: Table 2. Block Diagram Corrected: Figure 2.1 “Source clock selection Register” -->” Sampling clock selection Register” “Received control” -->” Reception control” Corrected: Table 2.1 “Low frequency clock” -->”Low speed clock” “Timer trigger for clock sauce”-->”Timer trigger for clock source” 3.1. Clock supply Corrected: Explanation contents 3.2.1. Sampling clock Corrected: Explanation contents 3.2.2. Basic operation Corrected: Figure 3.1 (Figure title) 3.2.3.1. Settings of Noise Cancelling Time Corrected: Figure 3.2 (Figure title) 3.2.3.2. Settings of Detecting Leader Added: Table 3.2 “Note: For “Low width only”, ***[RMCxRCR4]***<RMCPO> = 1 should be set.” 3.2.3.4. Settings of Reception Completion Corrected: Figure 3.5 (Figure title) 3.2.6.1. Leader detection interrupt Corrected: “An interrupt to occur when a leader is ---------” 3.2.7. Receiving Remote Control Signal without Leader in Waiting Leader Corrected: “By setting ***[RMCxRCR2]***<RMCLD> ----------” 3.2.8. A Leader only with "Low" Width Corrected: “The figure shown”-->” Figure 3.9 shown” Corrected: “<RMCLLMAX[7:0]> = 00000000”-->” <RMCLLMAX[7:0]> = 0x00” Deleted: “The maximum data bit cycle is configured with the <RMCDMAX[7:0]> of the ***[RMCxRCR2]***.” Corrected: “To complete data ----------” Corrected: “A reception end / interrupt occurs after ----------” Corrected: Figure 3.9 3.2.9. Receiving a Remote Control Signal in a Phase Method Corrected: “Details of the two thresholds are shown ----------” Corrected: “To determine a remote control signal ----------” -->” In the discrimination of the stationary ----------” 4.1. Register List Corrected: Register Name “Source Clock selection Register” -->” Sampling Clock selection Register” 4.2.7. ***[RMCxRCR2]*** (Receive Control Register 2) Deleted: Function of Bit Symbol (RMCPHM) “To receive a fixed frequency remote control signal by a pulse modulation, set this bit to "1".” Corrected: Function of Bit Symbol (RMCLL[7:0]) “00000000～11111110:”-->”0x00～0xFE:” “11111111:”-->”0xFF” Added: “(Note2)” Corrected: Function of Bit Symbol (RMCDMAX[7:0]) “00000000～11111110:”-->”0x00～0xFE:” “11111111:”-->”0xFF” Added: “(Note2)” Added: Note2 4.2.8. ***[RMCxRCR3]*** (Receive Control Register 3) Corrected: Function of Bit Symbol (RMCDATH[6:0]) Added: “(Note2)” Deleted: “If the measured cycle ----------” Added: “(Note3)” Corrected: Function of Bit Symbol (RMCDATL[6:0]) Deleted: “As for the determination of ----------” Added: “(Note4)” Corrected: Note2)

		Added: Note3)、Note4) 4.2.9. ***[RMCxRCR4]*** (Receive Control Register 4) Corrected: Function of Bit Symbol (RMCNC[3:0]) “0000:”-->”0x0” “0001～1111:”-->”0x1～0xF:” Corrected: “Note1”-->”Note” 4.2.10. ***[RMCxRSTAT]*** (Receive Status Register) Corrected: Function of Bit Symbol (RMCRNUM[6:0]) “0000000:”-->”0x00” “0000001～1001000:”-->”0x01～0x48:” “1001001～1111111:”-->”0x49～0xFF:” Deleted: “The number cannot be monitored ---------” Added: (Note2) Added: Note1)、Note2) 4.2.11. ***[RMCxEND1]***(Receive End bit Number Register 1) Corrected: Function of Bit Symbol (RMCEND1[6:0]) “0000000:”-->”0x00” “0000001～1001000:”-->”0x01～0x48:” “1001001～1111111:”-->”0x49～0xFF:” 4.2.12. ***[RMCxEND2]***(Receive End bit Number Register 2) Corrected: Function of Bit Symbol (RMCEND2[6:0]) “0000000:”-->”0x00” “0000001～1001000:”-->”0x01～0x48:” “1001001～1111111:”-->”0x49～0xFF:” 4.2.13. ***[RMCxEND3]***(Receive End bit Number Register 3) Corrected: Function of Bit Symbol (RMCEND3[6:0]) “0000000:”-->”0x00” “0000001～1001000:”-->”0x01～0x48:” “1001001～1111111:”-->”0x49～0xFF:” Added: Note1)、Note2) 4.2.14. ***[RMCxFSSEL]*** (Sampling Clock selection Register) Corrected: Chapter “Source Clock selection Register” -->” Sampling Clock selection Register Corrected: Function of Bit Symbol (RMCCLK) Corrected: “Low frequency Clock”-->” Low speed Clock” Corrected: “Timer output”-->”Timer trigger” Added: Note2) ・5. Precautions Corrected: Explanation contents

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