M3H Group(1)
Application Note
CMSIS System &
Clock Configuration

Outlines

This application note explains the operation of the sample programs of Startup and System files.
It is reference material when developing products using M3H Group(1) with each function.
This document helps the user check operation of the product and develop its program.

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1. Preface

This sample program executes the initial settings when an application program is used.
The watchdog timer and the system clock can be set properly.
This sample program assumes that the watchdog timer is set to "disable" immediately after a reset.
For the details, refer to “Clock control and operation mode” and “Clock selective watchdog timer” in Reference manual.

2. Reference Document

- Datasheet
  TMPM3H group (1) datasheet Rev2.0 (Japanese edition)
- Reference manual
  Clock Control and operation mode (CG-M3H(1)-D) Rev2.0 (Japanese edition)
  Clock Selective Watchdog Timer (SIWDT-A) Rev2.1 (Japanese edition)

3. Function to Use

IP	channel	port	Function / operation mode
Watchdog timer	-	-	Watchdog timer disable
Clock control	-	-	External oscillation input and PLL enable

4. Target Device

The target devices of application note are as follows.

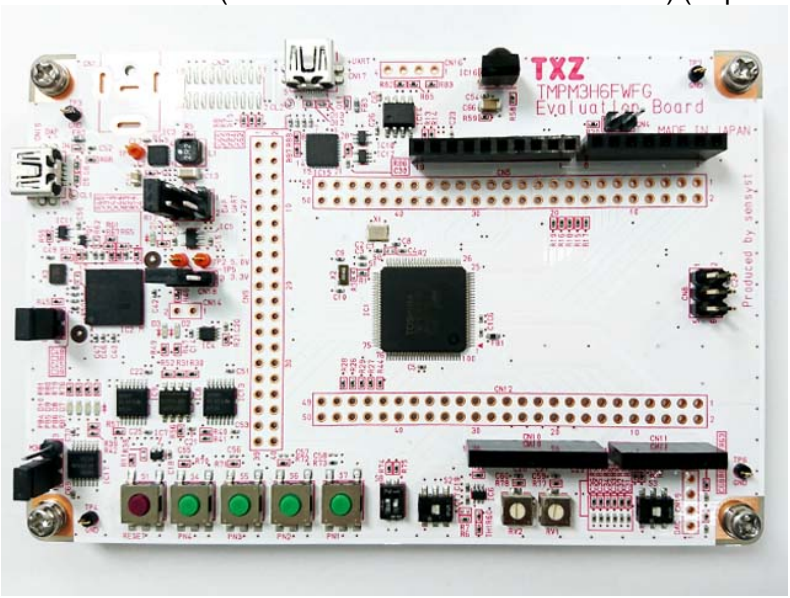
TMPM3H6FWFG	TMPM3H6FUFG	TMPM3H6FSFG
TMPM3H6FWDFG	TMPM3H6FUDFG	TMPM3H6FSDFG
TMPM3H5FWFG	TMPM3H5FUFG	TMPM3H5FSFG
TMPM3H5FWDFG	TMPM3H5FUDFG	TMPM3H5FSDFG
TMPM3H4FWUG	TMPM3H4FUUG	TMPM3H4FSUG
TMPM3H4FWFG	TMPM3H4FUFG	TMPM3H4FSFG
TMPM3H3FWUG	TMPM3H3FUUG	TMPM3H3FSUG
TMPM3H2FWDUG	TMPM3H2FUDUG	TMPM3H2FSDUG
TMPM3H2FWQG	TMPM3H2FUQG	TMPM3H2FSQG
TMPM3H1FWUG	TMPM3H1FUUG	TMPM3H1FSUG
TMPM3H1FPUG	TMPM3H0FSDUG	TMPM3H0FMDUG

* This sample program operates on the evaluation board of TMPM3H6FWFG.
If other function than the TMPM3H6 one is checked, it is necessary that CMSIS Core related files (C startup file and I/O header file) should be changed properly.
The BSP related file is dedicated to the evaluation board (TMPM3H6). If other function than the TMPM3H6 one is checked, the BSP related file should be changed properly.

5. Operation confirmation condition

Used microcontroller TMPM3H6FWFG
Used board TMPM3H6FWFG Evaluation Board (Product of Sensyst)
Unified development environment IAR Embedded Workbench for ARM 8.11.2.13606
Unified development environment µVision MDK Version 5.24.2.0
Sample program V1100

Evaluation board (TMPM3H6FWFG Evaluation Board) (Top view)

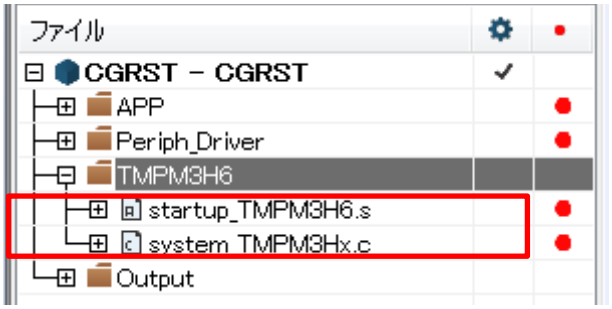


For purchasing the board, refer to the following homepage. (http://www.chip1stop.com/)

6. Function

The settings of the watchdog timer and CG are executed.
After reset, it is run from the startup and proceeds to main processing.
The following files are described in this application note.

startup_TMPM3H6.s
system_TMPM3Hx.c



6.1. Watchdog Timer Setting

Set the watchdog timer.
This sample program does not use this function (Disabled).

6.2. Clock Generator Setting

This sample program switches the system clock between an external clock (f_{EHOSC}) and an internal one (f_{IHOSC1}).
And it also executes the settings of the division ratio of the clock for output control and frequency multiplying ratio of the PLL.

7. Start-up and System File

This sample program is used for the operation of TMPM3H6.

7.1. Operation

This sample program executes the settings of each clock, the watchdog timer, the system core clock, and the PLL.
After the settings are done, the main procedure of an application program executes.

7.2. Watchdog Timer Setting

The watchdog timer switches between Enable and Disable with the SIWD_SET macro of "system_TMPM3Hx.c".
The default is Disable (1U).
SIWD_SETUP (1U) should be changed to 0, then the watchdog timer is set to Enable.
When this sample program is used in the Enable setting, the watchdog timer starts with the initial setting value and the reset is asserted after the watchdog operation is detected.

7.3. Clock Setting

An external clock or an internal clock are selected by switching.
An external oscillation clock has been selected in the sample program.
CLOCK_SETUP (1U)
When switch to internal oscillation, change to "0 U".

The system clock should be set.
SYSCR_Val (0x00000000UL)
This sample program executes to set the initial values.
The prescaler clock and the system clock operate with the setting of fc.
After the warming-up register and the oscillation register are set, the PLL register should be set.

7.4. PLL Setting

The clock multiplying circuit outputs f_{PLL} clock (maximum 40 MHz) which is generated by multiplying suitably the output clock fosc frequency (6 MHz to 12 MHz) of the high speed oscillator.
In this sample program, the external clock frequency is supposed to be 12 MHz.

This sample program operates with the f_{PLL} setting.
This sample program supports the input frequency 6/8/10/12 MHz.
The suitably multiplied frequencies are as follows.
External input frequency * (Multiplying value/Dividing value) = Operating frequency
6 MHz 6.00 MHz * (53.3125/8) = 39.98 MHz
8 MHz 8.00 MHz * (40.0000/8) = 40 MHz
10 MHz 10.00 MHz * (32.0000/8) = 40 MHz
12 MHz 12.00 MHz * (26.6250/8) = 39.94 MHz

In this sample program, the PLL setting value has been selected to 12 MHz and the multiplying ratio has been set to 3.328.
#define PLL0SEL_Ready CG_12M_MUL_3_328_FPLL
If PLL0SEL_Ready is changed to the setting value in system_TMPM3Hx.c, the PLL setting value can be chanted.
CG_6M_MUL_6_664_FPLL 6 MHz selection and the multiplying rate 6.664
CG_8M_MUL_5_FPLL 8 MHz selection and the multiplying rate 5
CG_10M_MUL_4_FPLL 10 MHz selection and the multiplying rate 4
CG_12M_MUL_3_328_FPL 12 MHz selection and the multiplying rate 3.328

7.5. Clock Frequency Switching

The system clock can be divided by the clock gear in ***[CGSYSCR].***
SYSCR_Val (0x00000000UL)
The clock selection and the system clock gear selection can be done if the setting value above is changed.
The sample program operates with the fc setting.

The input of the core clock is the clock divided by SYSCR.
The system core clock is used for the sample program (CGRST, I2C, and others).

8. Precaution

When using the sample program with CPU other than TMPM3H6, please check operation sufficiently.

9. Revision History

Rev	Date	Page	Description
1.0	2018-03-07	-	First release

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