

32-bit RISC Microcontroller

TXZ Family

Reference Manual

Asynchronous Serial Communication

Circuit

(UART-D)

Revision 1.1

2019-07

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

Contents

Preface	5
Related document.....	5
Conventions	6
Terms and Abbreviations	8
1. Outlines	9
2. Configuration.....	10
3. Function and Operation	11
3.1. Clock Supply	11
3.2. Transfer Clock(Baud rate generator)	11
3.3. Data Format	13
3.4. Reception Buffer / Transmission Buffer	14
3.4.1. Reception Buffer.....	15
3.4.2. Transmission Buffer.....	15
3.5. Data Reception	16
3.5.1. Basic Operation.....	16
3.5.2. Reception Error Handling	17
3.5.3. Noise removal of RXD input	19
3.6. Data Transmission	20
3.6.1. Basic Operation.....	20
3.6.2. Transmission of Break Error.....	21
3.7. Handshake Function	22
3.8. Wakeup Function	23
3.9. Half Clock Mode.....	24
3.9.1. Data Reception in Half Clock Mode.....	24
3.9.2. Data Transmission in Half Clock Mode.....	24
3.10. DMA Request.....	25
3.11. Loopback Function(Test function)	26
3.12. Software Reset	26
4. Registers	27
4.1. List of Registers	27
4.2. Details of Registers	28
4.2.1. [UARTxSWRST] (Software Reset Register).....	28
4.2.2. [UARTxCR0] (Control Register0).....	29
4.2.3. [UARTxCR1] (Control Register1).....	31
4.2.4. [UARTxCLK] (Clock Control Register).....	32
4.2.5. [UARTxBRD] (Baud Rate Register).....	32
4.2.6. [UARTxTRANS] (Transfer Enable Register).....	33
4.2.7. [UARTxDR] (Data Register)	33
4.2.8. [UARTxSR] (Status Register)	34
4.2.9. [UARTxFIFOCLR] (FIFO Clear Register)	36

4.2.10. [UARTxERR] (Error Register).....	37
5. Usage Example.....	38
5.1. Baud Rate Setting Value.....	38
6. Precautions	39
7. Revision History	40
RESTRICTIONS ON PRODUCT USE.....	41

List of Figures

Figure 2.1	UART block diagram.....	10
Figure 3.1	Transfer clock generator.....	11
Figure 3.2	Data format	13
Figure 3.3	Data buffer configuration	14
Figure 3.4	Receive timing	16
Figure 3.5	Reception buffer full operation timing.....	17
Figure 3.6	Error flag update timing	18
Figure 3.7	Noise removal operation (when <NF>=101)	19
Figure 3.8	Transmission timing.....	20
Figure 3.9	Serial link of the wakeup function.....	23
Figure 3.10	Reception data in the half clock mode.....	24
Figure 3.11	Data 0 transmission in the half clock mode.....	24
Figure 3.12	Transmission waveform in 1-pin mode.....	24
Figure 3.13	Transmission waveform in 2-pin mode.....	25

List of Tables

Table 2.1	List of Signals.....	10
Table 3.1	Transfer mode.....	13
Table 5.1	Setting example at $\Phi_{Tx} = 40\text{MHz}$, $[UARTxCLK]<PRSEL> = 0000$, and $[UARTxBRD]<KEN> = 1$	38
Table 5.2	Setting example at $\Phi_{Tx} = 80\text{MHz}$, $[UARTxCLK]<PRSEL> = 0000$, and $[UARTxBRD]<KEN> = 1$	38
Table 7.1	Revision history.....	40

Preface

Related document

Document name
Exception
Clock Control and Operation Mode
Product Information
Input/Output Ports

Conventions

- Numeric formats follow the rules as shown below:
 - Hexadecimal: 0xABC
 - Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
 - Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
 - Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by [] defines the register.
 - Example: [ABCD]
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
 - Example: [XYZ1], [XYZ2], [XYZ3] → [XYZn]
- "x" substitutes suffix number or character of units and channels in the Register List.
 - In case of unit, "x" means A, B, and C ...
 - Example: [ADACR0], [ADBCR0], [ADCCR0] → [ADxCR0]
 - In case of channel, "x" means 0, 1, and 2 ...
 - Example: [T32A0RUNA], [T32A1RUNA], [T32A2RUNA] → [T32AxRUNA]
- The bit range of a register is written like as [m: n].
 - Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
 - Example: [ABCD]<EFG> =0x01 (hexadecimal), [XYZn]<VW> =1 (binary)
- Word and Byte represent the following bit length.
 - Byte: 8 bits
 - Half word: 16 bits
 - Word: 32 bits
 - Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
 - R: Read only
 - W: Write only
 - R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of " - " is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is " - ", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value.
 - In the cases that default is " - ", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

Arm, Cortex and Thumb are registered trademarks of Arm Limited (or its subsidiaries) in the US
and/or elsewhere. All rights reserved.



The Flash memory uses the Super Flash® technology under license from Silicon Storage Technology, Inc.
Super Flash® is registered trademark of Silicon Storage Technology, Inc.

All other company names, product names, and service names mentioned herein may be trademarks of their respective companies.

Terms and Abbreviations

Some of abbreviations used in this document are as follows:

ACK	Acknowledgement
CTS	Clear To Send
DMA	Direct Memory Access
FIFO	First-In First-Out
LSB	Least Significant Bit
MSB	Most Significant Bit
RTS	Request To Send
TRGSEL	Trigger Selection circuit
UART	Universal Asynchronous Receiver Transmitter

1. Outlines

The asynchronous serial communication circuit (UART) can operate as a transmission/reception circuit of 1 channel (UTxTXDA / UTxTXDB / UTxRXD) per unit. The following is a list of functions.

Function classification	Function	Operation explanation
Baud rate control	Frequency dividing of prescaler	Selectable from 1/1 to 1/512 of prescaler clock.
	Clock selection	Selectable prescaler dividing clock or timer output
	Baud rate generator	N dividing or $N + (64 - K) / 64$ (N = 1 to 65535 and K = 0 to 63) dividing of the source clock frequency are possible.
Data format	Data length	Selectable 7, 8, or 9-bit.
	Parity	Parity control: Enable or disable selection Parity type: Even or odd parity is selectable
	Stop bit length	Selectable 1-bit or 2-bit.
	Data transfer order	Selectable LSB first or MSB first.
	Data signal inversion	Inversion control of the input and output data signal. Selectable disabled or enabled.
Transmission / reception control	FIFO storage stages	Reception: 8 stages Transmission: 8 stages
	Noise canceling function	Reception: Noise canceling function is enabled or disabled for UTxRXD.
	Error detection	Reception: Parity error, Framing error, Break error, Overrun error Transmission: Trigger transmission error
	Handshake function	Transmission/reception control by handshake with UTxCTS_N / UTxRTS_N signal is possible.
	Wake-up function	Serial link operation using the wakeup function in the 9-bit mode is possible.
Interlocking control	Interrupt	Reception interrupt, Transmission interrupt, and Error interrupt.
	DMA request	Reception DMA request: Burst transfer or Single transfer Transmission DMA request: Burst transfer or Single transfer
Special control	Half clock mode (Transmission / reception)	Transmission and reception with half width of Low width of the normal UART waveform is possible.
	Loopback function (Test function)	The transmission data is connected to the reception data and the loopback test is possible.
	Software reset	Initialization can be done by software.

UTxTXDA can be exchanged for UTxRXD and UTxCTS_N can be exchanged for UTxRTS_N, too. This is done by a port setting. Refer to "Input/Output Ports" of the reference manual.

2. Configuration

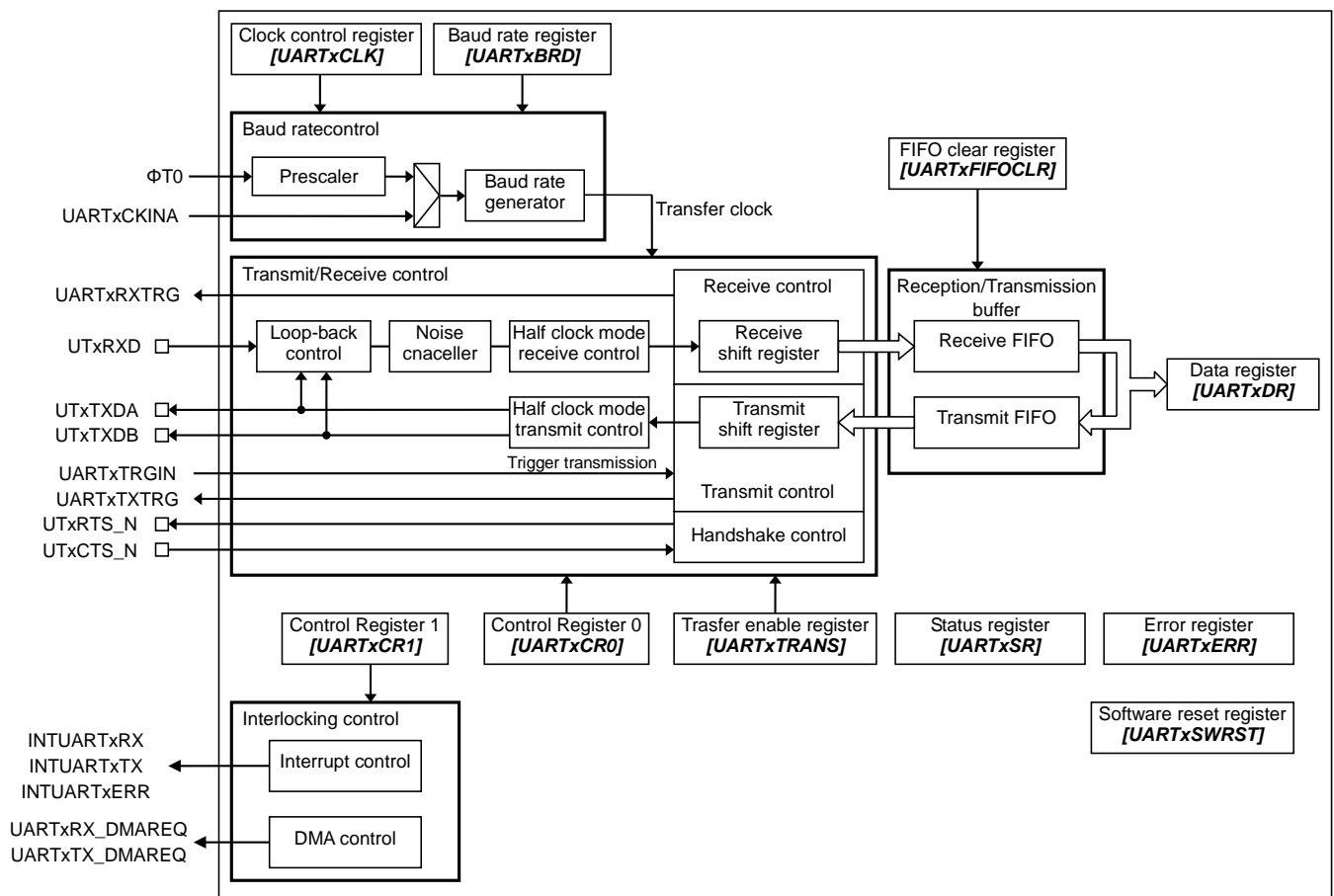


Figure 2.1 UART block diagram

Table 2.1 List of Signals

No	Symbol	Signal name	I/O	Related Reference manual
1	ΦT0	Prescaler clock	Input	Clock Control and Operation Mode
2	UARTxCKINA	Timer output	Input	Product Information
3	UTxRXD	Data input pin	Input	Product Information
4	UTxTXDA	Data output pin A	Output	Product Information
5	UTxTXDB	Data output pin B	Output	Product Information
6	UTxRTS_N	Request to send signal pin	Output	Product Information
7	UTxCTS_N	Clear to send signal pin	Input	Product Information
8	UARTxTRGIN	Trigger transmission signal input pin	Input	Product Information
9	INTUARTxRX	Reception interrupt	Output	Exception
10	INTUARTxTX	Transmission interrupt	Output	Exception
11	INTUARTxERR	Error interrupt	Output	Exception
12	UARTxRXTRG	Reception completion trigger	Output	Product Information
13	UARTxTXTRG	Transmission completion trigger	Output	Product Information
14	UARTxRX_DMAREQ	Reception DMA request	Output	Product Information
15	UARTxTX_DMAREQ	Transmission DMA request	Output	Product Information

3. Function and Operation

3.1. Clock Supply

When you use UART, please set an applicable clock enable bit to "1" (clock supply) in Clock supply and stop register A for fsys (*[CGFSYSENA]*, *[CGFSYSMENA]*), Clock supply and stop register B for fsys (*[CGFSYSENB]*, *[CGFSYSMENB]*), and Clock supply and stop register for fc (*[CGFCEN]*).

An applicable register and the bit position vary according to a product. Therefore, the register may not exist with the product. Please refer to "Clock Control and Operation Mode" of the reference manual for the details.

When attempting to stop supplying the clock, make sure to check whether the UART is stopping. Note that when the MCU enters STOP mode, make sure to check whether the UART is stopping as well.

3.2. Transfer Clock(Baud rate generator)

The following shows the diagram of the transfer clock generator.

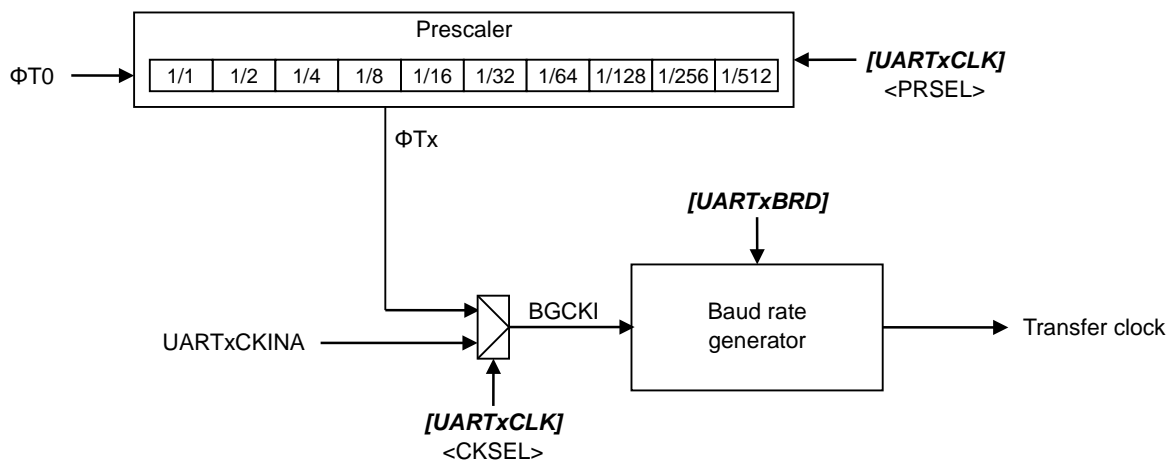


Figure 3.1 Transfer clock generator

The prescaler divides the frequency of the prescaler clock ($\Phi T0$) into 1/1 to 1/512. The dividing value is selected by $[UARTxCLK] \langle PRSEL \rangle$.

The input of baud rate generator is selected from the prescaler dividing clock (ΦTx) or timer output ($UARTxCKINA$) by $[UARTxCLK] \langle CKSEL \rangle$ (Baud rate generator clock selection). (Note)

The baud rate generator generates a transfer clock by dividing the frequency of the clock selected by $\langle CKSEL \rangle$ into N dividing or $N + (64 - K) / 64$ dividing. The setting of the dividing value is done in $[UARTxBRD]$. The transfer clock frequency is 16 times the baud rate.

Note: When the timer output is selected, High width and Low width of the timer output ($UARTxCKINA$) should be more than $\Phi T0$ cycle twice.

The baud rate is calculated as follows:

$$\text{Baud rate} = \frac{\text{BGCKI}}{N + \frac{(64 - K)}{64}} \div 16$$

The baud rate of the N dividing is calculated as follows:

$$\text{Baud rate} = \frac{\text{BGCKI}}{N} \div 16$$

Note: The maximum baud rate is different depending on the product, please refer to the datasheet or "Product Information" of the reference manual.

3.3. Data Format

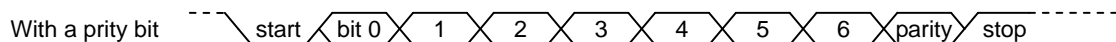
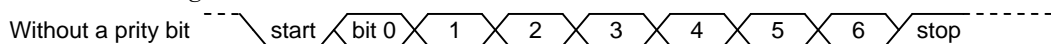
The summary of the data formats is shown in Table 3.1 and Figure 3.2.

A data length, a data transfer order, a parity, a STOP bit length, and a data signal inversion can be selected.

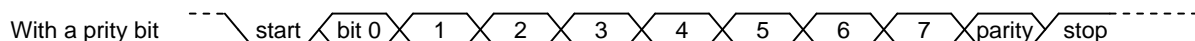
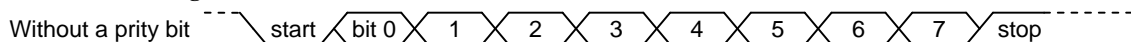
Table 3.1 Transfer mode

Data length	Data transfer order	Parity	STOP bit length (transmission)	Data signal inversion
7-bit	LSB first / MSB first	Presence / absence Even / Odd	1-bit or 2-bit	Performed / Not performed
8-bit				
9-bit				

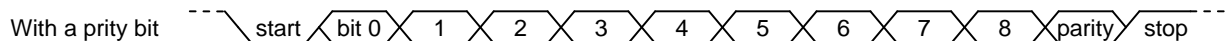
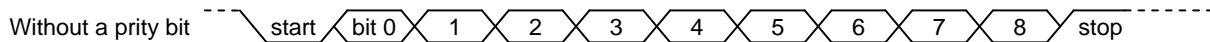
- 7-bit data length / LSB first / No data inversion



- 8-bit data length / LSB first / No data inversion



- 9-bit data length / LSB first / No data inversion



- 9-bit data length / MSB first / Data inversion

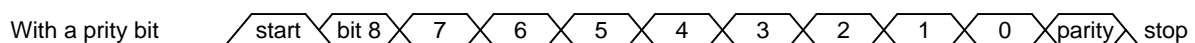
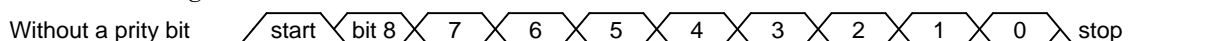


Figure 3.2 Data format

(1) Data length

Selected from among 7, 8, and 9-bit.

(2) Parity control

When $[UARTxCR0]<PE>$ (Parity addition) is set to "1", the parity is enabled. The even or odd parity can be selected by $[UARTxCR0]<EVEN>$ (Even parity selection).

The parity control circuit generates automatically a parity for the data in the transmission buffer at data transmission. The settings of $<PE>$ and $<EVEN>$ should be done before the transmission data is written to $[UARTxDR]<DR>$ (Transmission data).

The parity is automatically generated from the reception data at data reception. The generated parity is compared with the received parity. If they are not identical, the parity error is generated.

(3) STOP bit length

$[UARTxCR0]<SBLEN>$ (STOP bit length select) can set the STOP bit length in the UART transmission mode to 1-bit or 2-bit. At data reception, the STOP bit length is handled as 1 bit regardless of the setting value of this bit.

(4) Transmission signals

In the standard UART communication, the signals are output on the UTxTXDA pin.

In the half clock mode, the signals are output on the UTxTXDA pin and the UTxTXDB pin. For the details, refer to "3.9 Half Clock Mode".

(5) Data signal inversion

The data inversion is set by $[UARTxCR0]<IV>$ (Data signal inversion). When it is set to "1", the input and output data are inverted.

(6) Data exchange

The function of UTxTXDA, UTxRXD, UTxCTS_N, and UTxRTS_N can be exchanged. This is done by a port setting. Refer to "Input/Output Ports" of the reference manual.

3.4. Reception Buffer / Transmission Buffer

Received data / transmitted data is stored in reception buffer/transmission buffer.

Either the reception buffer or the transmission buffer consists of a shift register and a FIFO. The stage count of the receive FIFO and transmit FIFO are "8", respectively.

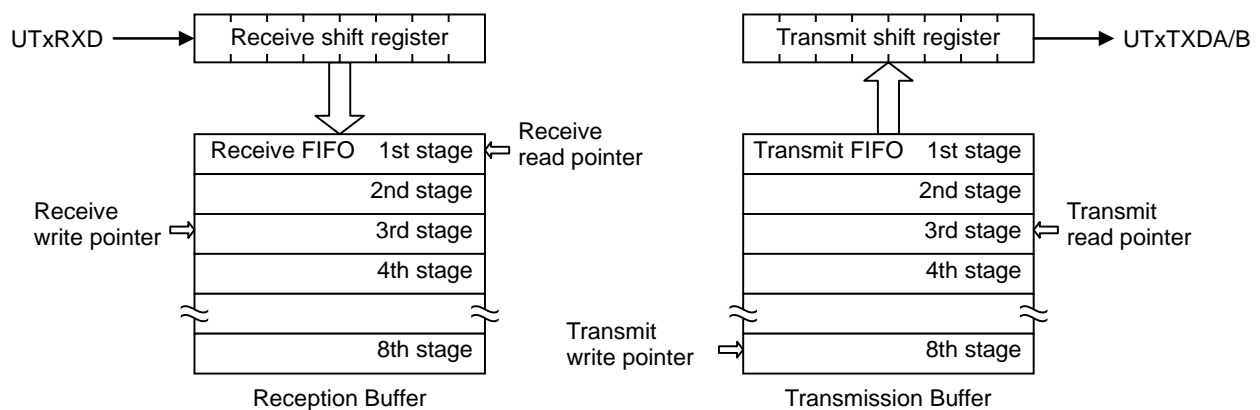


Figure 3.3 Data buffer configuration

3.4.1. Reception Buffer

When all bits (One frame) of data input from UTxRXD are stored in the receive shift register, the data is transferred to the receive FIFO and the receive write pointer is moved to the next stage. When the receive FIFO is read, the receive read pointer moves to the next stage. The data in the receive FIFO is read through *[UARTxDR]*(Data register).

The stage count of the data stored in the receive FIFO is shown in *[UARTxSR]<RLVL>*(Receive FIFO data storage level). The register *[UARTxDR]* should not be read when the receive FIFO is empty.

When the stage count of the data stored in the receive FIFO becomes identical with the count value set in the register *[UARTxCRI]<RIL>*(Reception Fill level setting), *[UARTxSR]<RXFF>*(Receive FIFO flag) is set to "1". Then, a reception interrupt is generated if *[UARTxCRI]<INTRXFE>* is set to "1" to enable a reception interrupt (Note). If receive FIFO interrupt control is enabled. The value of *[UARTxCRI]<RIL>* can be set to "1" to "8".

If *[UARTxFIFOCLR]<RFCLR>*(Reception buffer clear) is set to "1", the read/write pointer of the receive FIFO is initialized.

Note: Do not set the reception complete interrupt control enable (<INTRXWE> =1) and the receive FIFO interrupt control enable (<INTRXFE> =1) at the same time.

3.4.2. Transmission Buffer

The data written to *[UARTxDR]*(Data register) is stored in the transmit FIFO, and the transmit write pointer moves to the next stage. When data transmission is enabled, the data in the transmit FIFO is transferred to the transmission shift register. Then, the data is output on UTxTXDA/B pins. When the transmit FIFO is transferred, the transmit read pointer moves to the next stage.

The stage count of the data in the transmit FIFO is shown in *[UARTxSR]<TLVL>*(Transmit FIFO data storage level).

When the data in the transmit FIFO is transferred to the transmission shift register and the stage count of the data in the transmit FIFO becomes identical with the count value set in *[UARTxCRI]<TIL>*(Transmission Fill level setting), *[UARTxSR]<TXFF>*(Transmit FIFO flag) is set to "1". Then, a transmission interrupt is generated if *[UARTxCRI]<INTTXFE>* is set to "1" to enable a transmission interrupt. The value of *[UARTxCRI]<TIL>* can be set to "0" to "7".

If *[UARTxFIFOCLR]<TFCLR>*(Transmission buffer clear) is set to "1", the read/write pointer of the transmit FIFO is initialized.

3.5. Data Reception

3.5.1. Basic Operation

If $[UARTxTRANS]<RXE>$ (Reception control) is set to "1", the data reception is enabled.

When the START bit is detected, the data reception starts. The data bits and the STOP bit is received. When $[UARTxTRANS]<RXE> = 1$ is set and $UTxRXD$ is "Low", it is regarded immediately as start bit detection.

After one frame data is received completely, the data is transferred from the receive shift register to the receive FIFO. The reception completion flag is set. If the reception completion interrupt control is enabled by $[UARTxCRI]<INTRXWE> = 1$, the reception interrupt is generated.

If the reception FIFO interrupt control is enabled by $[UARTxCRI]<INTRXFE> = 1$, the receive interrupt is generated when the amount of the data in the receive FIFO reaches the Fill level which is set in $[UARTxCRI]<RIL>$ (Reception Fill level setting).

Note: Do not set the reception complete interrupt control enable ($<INTRXWE> = 1$) and the receive FIFO interrupt control enable ($<INTRXFE> = 1$) at the same time.

The followings are examples to generate the reception interrupt.

- When the Fill level is "1" ($[UARTxCRI]<RIL> = 001$):
One frame data is received completely when the receive FIFO is empty. And the received data is transferred from the receive shift register to the receive FIFO. Then, the storage stage count in the receive FIFO becomes "1".
- When the Fill level is "8" ($[UARTxCRI]<RIL> = 000$):
One frame data is received completely when the receive FIFO stores 7-stage data. And the received data is transferred from the receive shift register to the receive FIFO. Then, the storage stage count in the receive FIFO becomes "8".

If $[UARTxTRANS]<RXE>$ is set to "0" during the data reception, the data reception completes and the operation stops.

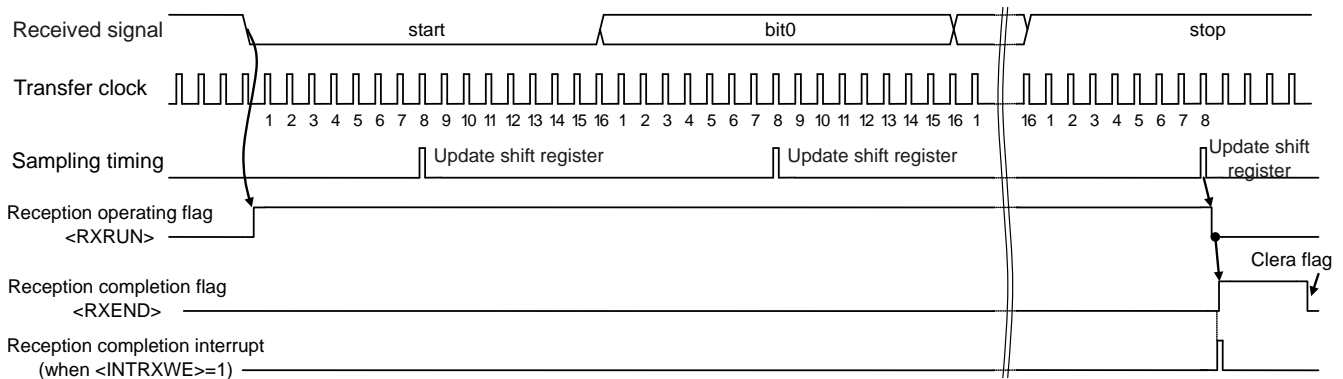


Figure 3.4 Receive timing

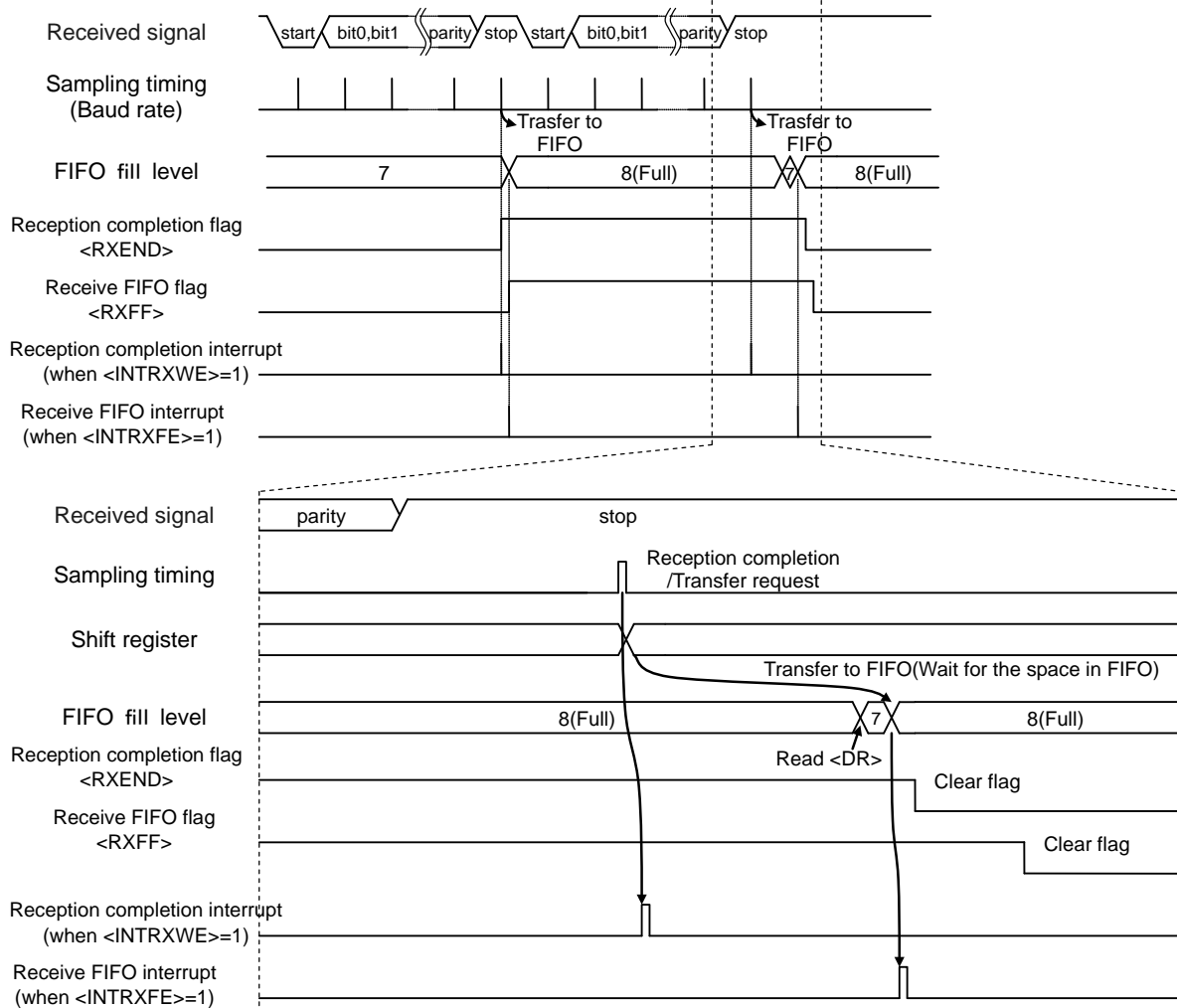


Figure 3.5 Reception buffer full operation timing

3.5.2. Reception Error Handling

If an error is detected, "1" is set to the corresponding error flag bit in $[UARTxERR]$ (Error register) and $[UARTxDR]$ (Data register). When the error occurs, please process appropriately. Also, if error interrupt control is enabled ($[UARTxCRI]<INTERR>=1$), an error interrupt occurs.

Note: If at least one error flag is set, the error interrupt is output. To cancel the error interrupt, clear all error flags with $[UARTxERR]$

The following error detections are done during the data reception.

- Parity error
When the parity addition function is enabled ($[UARTxCRO]<PE>$ (Parity addition) =1), after all bits of the data are received, the parity data generated from the reception data is compared with the received parity bit. If they are not identical, the parity error occurs. This error is masked when a break error occurs.
- Framing error
If the received STOP bit is "0", the framing error occurs. This error is masked when a break error occurs.

- Break error
When all data are "0" between the START bit and the STOP bit, the break error occurs.

- Overrun error
All stages in the receive FIFO store data and the receive shift register has data. Then, if the START bit of the next frame is detected, the overrun error occurs.
Even when the overrun error occurs, the data reception continues. But the received data is discarded. The data in the receive shift register remains. When $[UARTxDR]$ (Data register) is read and some space is generated in the receive FIFO, the data in the receive shift register is transferred to the receive FIFO. While the overrun flag is set, the reception completion interrupt is not generated.

When the overrun error occurs, take the following actions.

- (1) Disable reception control ($[UARTxTRANS]<RXE> = 0$)
- (2) Read received all data $[UARTxDR]$
- (3) Check completion of data reception stop ($[UARTxSR]<RXRUN> = 0$)
- (4) $[UARTxERR]<OVRERR>$ should be cleared.
- (5) Re-enable reception control($[UARTxTRANS]<RXE> = 1$)

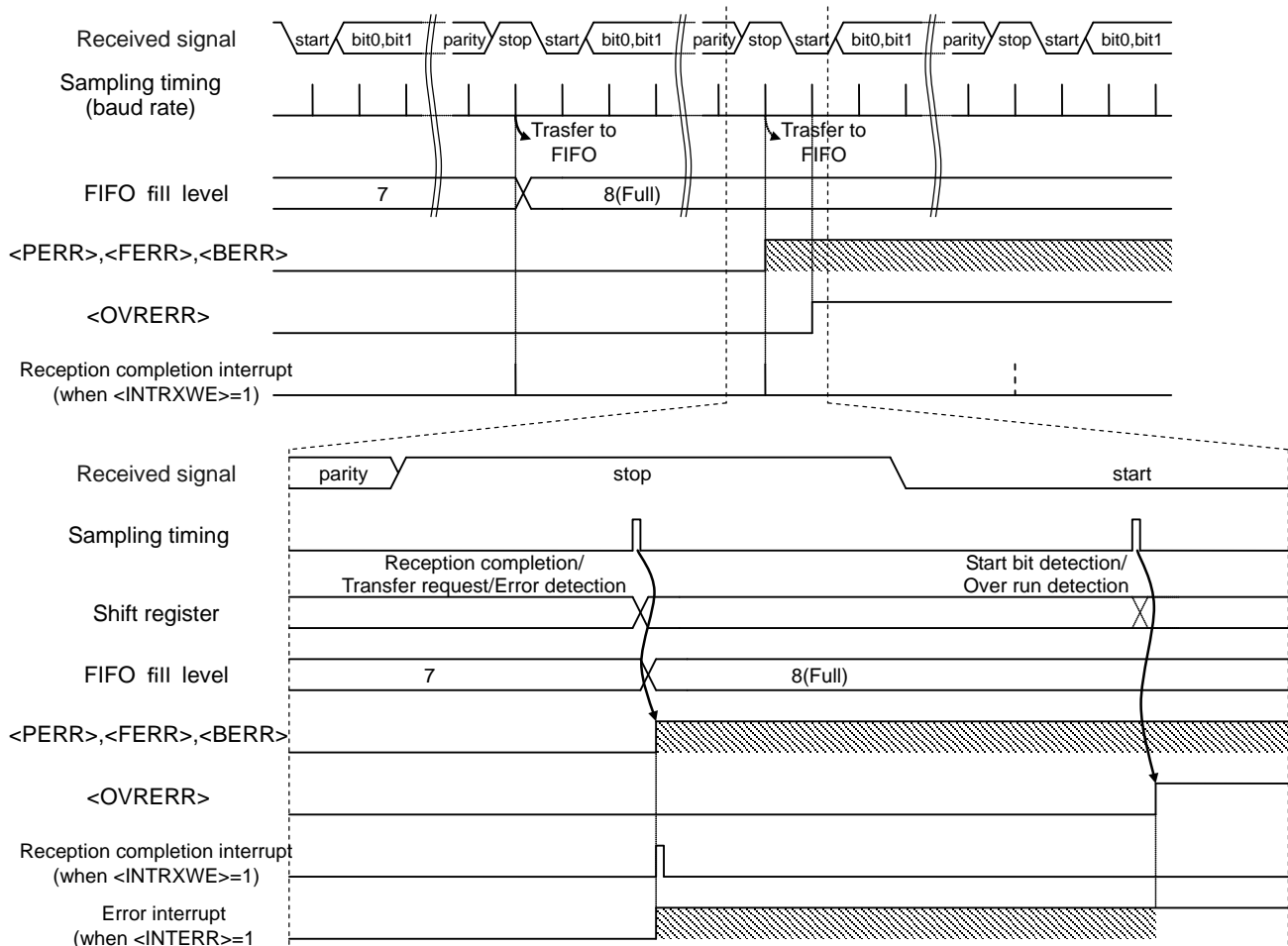


Figure 3.6 Error flag update timing

If the overrun flag is cleared with reception enabled when an overrun error occurs, the latest value of the shift register is stored in the FIFO upon reception of the first STOP bit after clearing the flag, and the receiving operation is continued thereafter. At this time, data stored by reception of the first STOP bit immediately before overrun error occurrence and flag clearing is not guaranteed.

3.5.3. Noise removal of RXD input

UTxRXD input has a noise filter function that operates with $\Phi T0$ clock or transfer clock. The noise removal time should be set with $[UARTxCR0]<NF>$ (UTxRXD noise removal time).

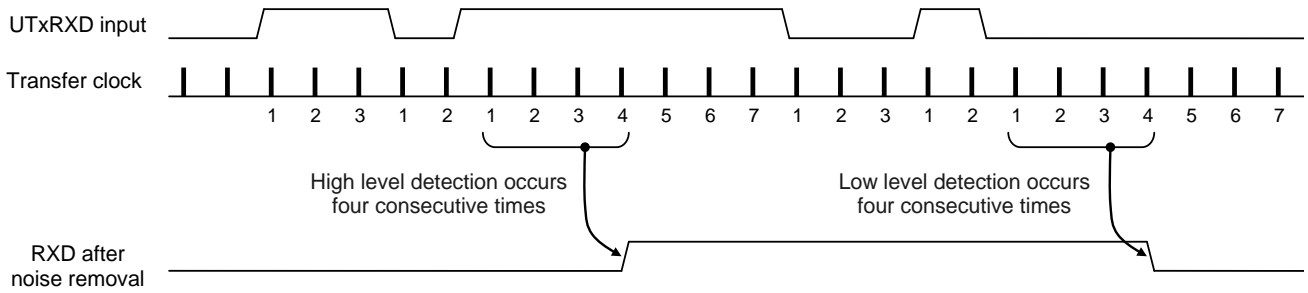


Figure 3.7 Noise removal operation (when $<NF>=101$)

3.6. Data Transmission

3.6.1. Basic Operation

Transmission operation has normal data transmission and data transmission using the trigger function.

- Normal data transmission

$[UARTxTRANS]<TXE>$ should be set to "1" to enable the data transmission. If data exists in the transmit FIFO, the transmission starts. Or, if data is written to the transmit FIFO, the transmission starts. For normal transmission without the trigger function, $[UARTxTRANS]<TXTRG>$ should be set to "0".

At the start of the transmission, data is transferred from the transmit FIFO to the transmission shift register. The START bit, the data, the parity (when the parity is enabled), and the STOP bit are transmitted in this order. When one frame is transmitted completely, the transmission completion flag is set. The transmission interrupt is generated if the interrupt is enabled by $[UARTxCRI]<INTTXWE> = 1$.

The data transmission continues until all data in the transmit FIFO are transmitted.

If the transmission interrupt is enabled by $[UARTxCRI]<INTTXFE> = 1$, the transmit interrupt is generated when the amount of the data in the transmit FIFO reaches the Fill level which is set in $[UARTxCRI]<TIL>$ (Transmission Fill level setting).

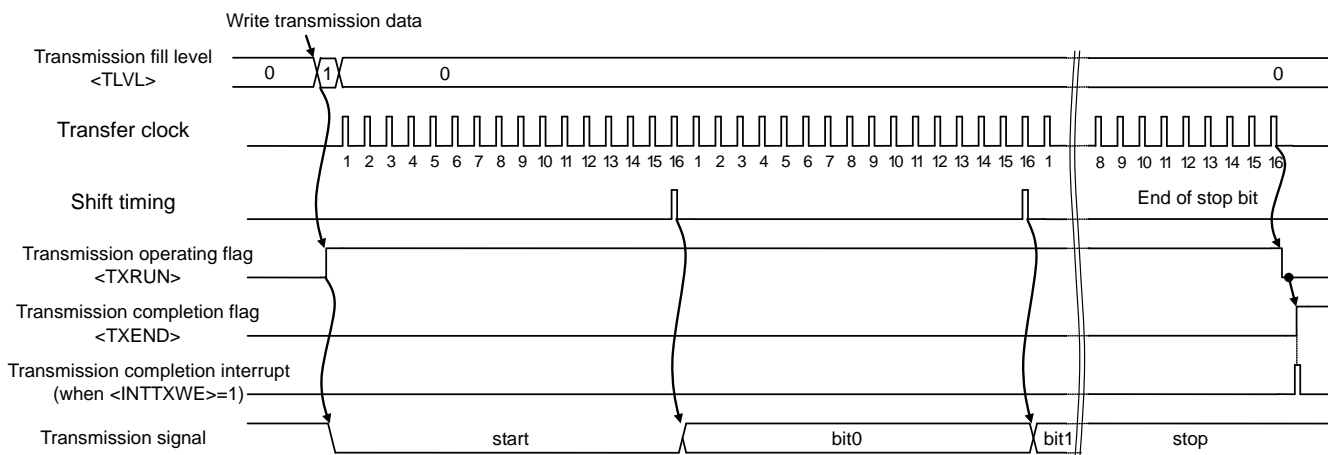


Figure 3.8 Transmission timing

- Data transmission using the trigger function

When $[UARTxTRANS]<TXTRG>$ is "1", $[UARTxTRANS]<TXE>$ should be "0".

When data exists in the transmit FIFO and a trigger is input, $[UARTxTRANS]<TXE>$ becomes "1" automatically and the transmission starts. After the necessary data is transmitted, $[UARTxTRANS]<TXE>$ should be set to "0" to wait for a trigger again. Transmission operation is the same as normal data transmission.

A new trigger is ignored during the data transmission

When no data exists in the transmit FIFO and a trigger is input, the trigger is ignored. Then, the error interrupt is generated and $[UARTxERR]<TRGERR>$ (Trigger transmission error flag) is set. When the error occurs, please process appropriately.

Note: If at least one error flag is set, the error interrupt is output. To cancel the error interrupt, clear all

error flags with *[UARTxERR]*

At the start of the transmission, data is transferred from the transmit FIFO to the transmission shift register. The START bit, the data, the parity (when the parity is enabled), and the STOP bit are transmitted in this order. When one frame is transmitted completely, the transmission completion flag is set. The transmission interrupt is generated if the interrupt is enabled by *[UARTxCRI]<INTTXWE> =1*.

The data transmission continues until all data in the transmit FIFO are transmitted. When *[UARTxTRANS]<TXTRG>* is "1", the transmitter waits for a trigger after all data are transmitted.

If the transmission interrupt is enabled by *[UARTxCRI]<INTTXFE> =1*, the transmit interrupt is generated when the amount of the data in the transmit FIFO reaches the Fill level which is set in *[UARTxCRI]<TIL>* (Transmission Fill level setting).

- The followings are examples to generate the transmission interrupt.
 - When the Fill level is "0" (*[UARTxCRI]<TIL> =000*):
Only one stage data is stored in the transmit FIFO. And the data is transferred from the transmit FIFO to the transmit shift register to transmit the data. The storage stage count in the transmit FIFO becomes "0".
 - When the Fill level is "7" (*[UARTxCRI]<TIL> =111*):
8 stage data is stored in the transmit FIFO. One stage data is transferred from the transmit FIFO to the transmit shift register to transmit the data. The storage stage count becomes "7".

- Disable of transmission control

When *[UARTxTRANS]<TXE>* is set to "0" during the data transmission, the transmitter stops after the current frame data transmission completes. The data in the transmit FIFO is maintained. Also, when re-enabling transmission control, set *[UARTxTRANS]<TXE>* to "1" after confirming transmission completion with *[UARTxSR]<TXRUN>=0*.

3.6.2. Transmission of Break Error

When *[UARTxTRANS]<BK>* (Break transmission) is set to "1", UTxTXDA/B output the Low level regardless of the value in *[UARTxTRANS]<TXE>* (Transmission control) and the enable/disable of the half clock mode. If *[UARTxTRANS]<BK>* is set to "1" during the data transmission, the Low level is output after the current frame is completely transmitted. Also, when the CTS handshake is enabled (*[UARTxCR0]<CTSE> =1*) and the UTxCTS_N pin is "High", the output of "Low" level is started.

[UARTxTRANS]<BK> should be set to "0" to stop the output of the Low level.

3.7. Handshake Function

The CTS/RTS handshake function controls the communication using the UTxCTS_N pin for the data transmission and the UTxRTS_N pin for the data reception. The CTS handshake function is enabled by *[UARTxCR0]<CTSE>* (CTS handshake function), and the RTS function is enabled by *[UARTxCR0]<RTSE>* (RTS handshake function).

When the CTS is enabled, the following operation is done. If the UTxCTS_N pin becomes "High" during the data transmission, the current data transmission completes and then the transmission stops until the UTxCTS_N pin becomes "Low". The transmission interrupt is generated as a normal operation. So, owing to this function, the next transmission data can be written to the transmission buffer and the transmitter can stay in the transmission wait state.

When the RTS is enabled, the UTxRTS_N pin outputs the Low level if the data reception is available, that is, the following conditions are valid:

- *[UARTxTRANS]<RXE>* (Reception control) is "1", which shows the data reception availability.
- The data reception is not operating.
- Receive FIFO has enough space or the receive shift register is empty.

3.8. Wakeup Function

In the 9-bit mode, the wakeup operation of the slave controller is enabled when the wakeup function control bit $[UARTxCR0]<WU>$ (Wake-up function) is set to "1".

A reception interrupt is generated only when the MSB bit of the reception data ($[UARTxDR]<DR[8]>$ (Reception data)) is "1".

Note: The UTxTXDA pins in the slave controllers should be in the open drain output mode.

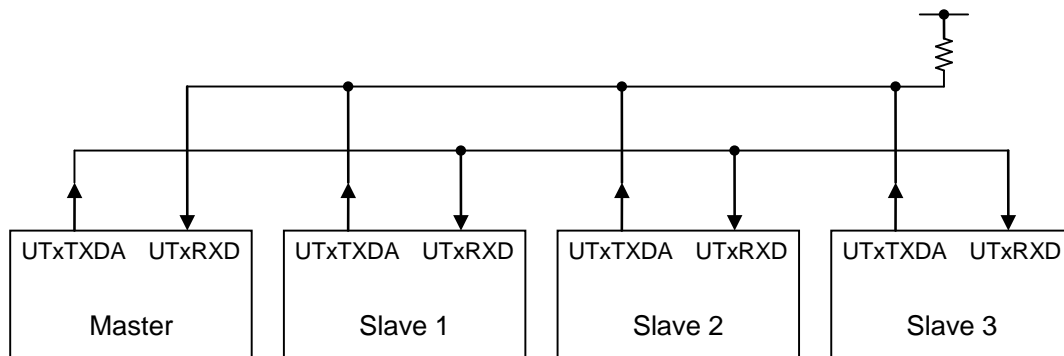


Figure 3.9 Serial link of the wakeup function

The execution procedure of the wakeup function is as follows:

The master and slave controllers should be set to the 9-bit mode ($[UARTxCR0]<SM>$ (Data length) = 10). Each slave controller should set $[UARTxCR0]<WU>$ to "1" to enable the data reception. Prepare the Select code (8 bits) for each slave controller beforehand.

The master controller transmits one frame data which includes the Select code (8 bits) of the slave controller. The MSB bit $[UARTxDR]<DR[8]>$ (Transmission data) should be set to "1".

Each slave controller receives the frame. If a select code of each slave controller is identical with the received one, it clears its own $[UARTxCR0]<WU>$ to "0". Comparison of select code is executed by software.

The master controller transmits data to the specified slave controller (the controller with $[UARTxCR0]<WU> = 0$). At this time, the MSB bit $[UARTxDR]<DR[8]>$ should be set to "0".

The slave controller whose $[UARTxCR0]<WU>$ is "1" ignores the reception data. The reception interrupt is not generated because the MSB bit $[UARTxDR]<DR[8]>$ (Reception data) is "0". The slave controller with $[UARTxCR0]<WU> = 0$ can transmit data to the master controller. So the slave controller can notify the master controller of the completion of reception.

3.9. Half Clock Mode

$[UARTxCR0]<HBSSEN>$ should be set to "1" to enable the half clock mode. In the half clock mode, the width of the data "0" becomes half of the Low width of the normal UART waveform.

3.9.1. Data Reception in Half Clock Mode

The Low level of the input data is detected and an appropriate width of "0" is generated to use a UART reception data (UTxRXD) in the half clock mode.

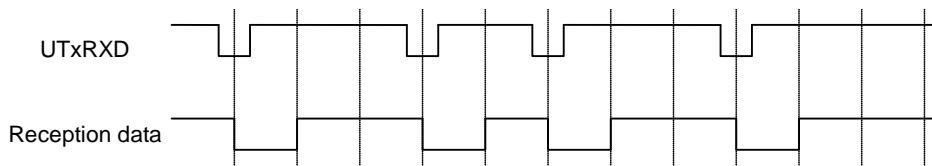


Figure 3.10 Reception data in the half clock mode

3.9.2. Data Transmission in Half Clock Mode

The data "0" width in the half clock mode is half of the width of the normal UART communication as shown in Figure 3.11.

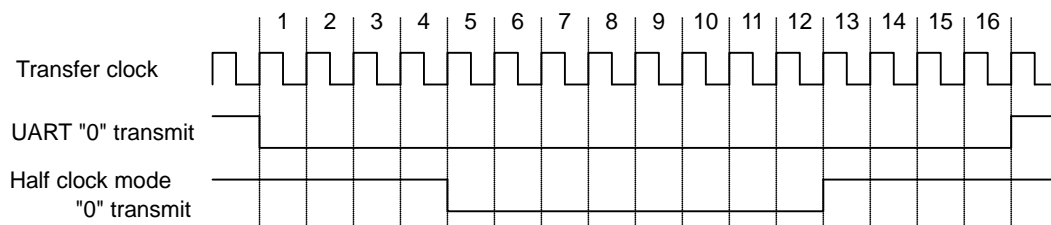


Figure 3.11 Data 0 transmission in the half clock mode

There are two transmission signal pins in the half clock mode. When $[UARTxCR0]<HBSMD>$ (Half clock mode communication output control) is set to "0" (1-pin mode), these two pins output the same signal. When it is set to "1" (2-pin mode), these pins output the data "0" alternately. $[UARTxCR0]<HBSST>$ (Half clock mode communication start control) sets which pin should output the data "0" first.

(1) 1-pin mode

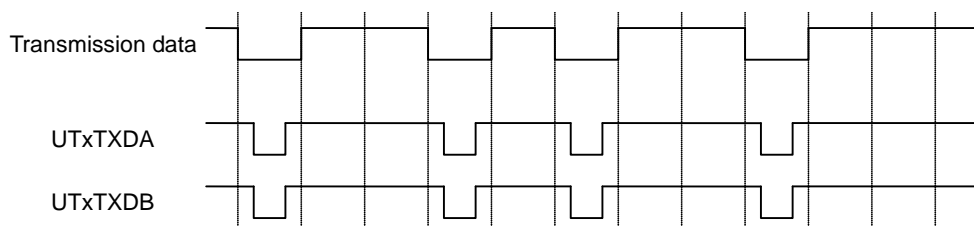


Figure 3.12 Transmission waveform in 1-pin mode

(2) 2-pin mode ($[UARTxCR0]\langle HBSST \rangle = 0$: UTxTXDA outputs "0" first.)

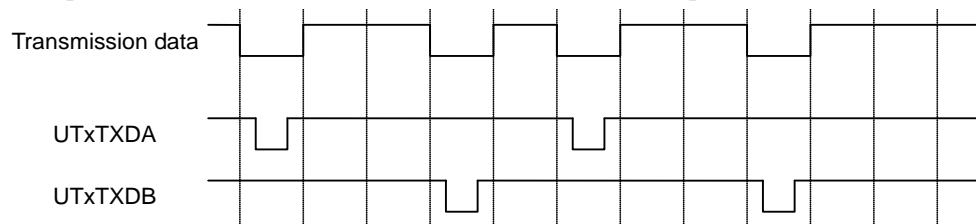


Figure 3.13 Transmission waveform in 2-pin mode

3.10. DMA Request

There are a single request and a burst request in the transmission.

- Reception DMA request

$[UARTxCRI]\langle DMARE \rangle$ (Reception DMA control) should be set to "1" to enable them.

When one data or more exist in the receive FIFO, the single request is generated.

The burst request is generated when the value of $[UARTxSR]\langle RLV L \rangle$ (Receive FIFO data storage level) which shows the stage count of the currently stored data becomes equal to or more than the reception interrupt generation level (Fill level) set in $[UARTxCRI]\langle RIL \rangle$ (Transmission Fill level setting). When the DMA transfer completes, the burst request is generated if the stored data level is equal to or more than the Fill level.

- Transmission DMA request

$[UARTxCRI]\langle DMATE \rangle$ (Transmission DMA control) should be set to "1" to enable them.

When one data stage space or more exist in the transmit FIFO, the single request is generated.

The burst request is generated when the value of $[UARTxSR]\langle TLV L \rangle$ (Transmit FIFO data storage level) which shows the stage count of the currently stored data becomes equal to or less than the transmission interrupt generation level (Fill level) set in $[UARTxCRI]\langle TIL \rangle$ (Transmission Fill level setting). When the DMA transfer completes, a burst request is generated if the stored data level is equal to or less than the Fill level.

3.11. Loopback Function(Test function)

[UARTxCR0]<LPB> (Loopback function) should be set to "1" to enable the loopback function. When the loopback function is enabled, the transmission data is connected to the reception data and the loopback test is possible.

The connection destination changes depending on the half clock mode control setting (*[UARTxCR0]*<HBSEN>(Half clock mode control)).

When the half clock communication is disabled (<HBSEN> =0), UTxTXDA is connected to the reception data.

When the half clock communication is enabled (<HBSEN> =1), the signal of the logical AND of UTxTXDA and UTxTXDB is connected to the reception data.

3.12. Software Reset

The sequence of the write of "10" to *[UARTxSWRST]*<SWRST>(Software reset) and the next write of "01" generates the software reset.

The software reset stops the data transfer and initializes the read/write pointers of the receive/transmit FIFO and the error flags. The registers *[UARTxTRANS]*(Transfer Enable Register), *[UARTxDR]*(Data Register), *[UARTxSR]*(Status Register), and *[UARTxERR]*(Error Register) are initialized.

The data in the registers *[UARTxCR0]*(Control Register 0), *[UARTxCRI]*(Control Register 1), *[UARTxCLK]*(Clock Control Register), and *[UARTxBRD]*(Baud Rate Register) are maintained.

The status of the software reset operation is shown in *[UARTxSWRST]*<SWRSTF>(Software reset flag). If the software reset is asserted, the next operation should be done after <SWRSTF> is checked to be "0".

4. Registers

4.1. List of Registers

The control registers and their addresses are shown as follows:

Function		Channel / Unit	Base address		
			TYPE1	TYPE2	TYPE3
Asynchronous Serial Communication Circuit	UART	ch0	0x400BB000	0x400CE000	0x4006E000
		ch1	0x400BB100	0x400CE400	0x4006E400
		ch2	0x400BB200	0x400CE800	0x4006E800
		ch3	0x400BB300	0x400CEC00	0x4006EC00
		ch4	0x400BBD00	0x400CF000	0x4006F000
		ch5	0x400BBE00	0x400CF400	0x4006F400
		ch6	-	0x400CF800	0x4006F800
		ch7	-	0x400CFC00	0x4006FC00

Note: The channel/unit and base address type are different by products. Please refer to "Product Information" of the reference manual for the details.

Register Name		Address (Base+)
Software Reset Register	[UARTxSWRST]	0x0000
Control Register0	[UARTxCR0]	0x0004
Control Register1	[UARTxCR1]	0x0008
Clock Control Register	[UARTxCLK]	0x000C
Baud Rate Register	[UARTxBRD]	0x0010
Transfer Enable Register	[UARTxTRANS]	0x0014
Data Register	[UARTxDR]	0x0018
Status Register	[UARTxSR]	0x001C
FIFO Clear Register	[UARTxFIFOCLR]	0x0020
Error Register	[UARTxERR]	0x0024

4.2. Details of Registers

4.2.1. [UARTxSWRST] (Software Reset Register)

Bit	Bit Symbol	After Reset	Type	Function
31:8	-	0	R	Reads as "0".
7	SWRSTF	0	R	Software reset flag 0: Software reset is not asserted. 1: Software reset is asserted.
6:2	-	0	R	Reads as "0".
1:0	SWRST[1:0]	00	W	Software reset The sequence of the write of "10" and the next write of "01" generates the software reset. The software reset initializes the registers [UARTxTRANS], [UARTxDR], [UARTxSR], and [UARTxERR]. And, the transmission and reception circuit is also initialized. The read/write pointers of the receive/transmit FIFO are initialized, too. When this field is read, "00" is returned.

4.2.2. [UARTxCR0] (Control Register0)

Bit	Bit Symbol	After Reset	Type	Function
31:19	-	0	R	Reads as "0".
18	HBSST	0	R/W	Half clock mode communication start control 0: Output starts at UTxTXDA pin. 1: Output starts at UTxTXDB pin.
17	HBSMD	0	R/W	Half clock mode communication output control 0: 1-pin mode 1: 2-pin mode
16	HBSEN	0	R/W	Half clock mode control 0: Disabled. 1: Enabled.
15	LPB	0	R/W	Loopback function 0: Disabled. 1: Enabled.
14:12	NF[2:0]	000	R/W	UTxRXD noise removal time 000: None. 001: A signal with 2 cycles or less with $\Phi T0$ clock is removed as noise, and a signal with 3 cycles or more is valid. 010: A signal with 4 cycles or less with $\Phi T0$ clock is removed as noise, and a signal with 5 cycles or more is valid. 011: A signal with 8 cycles or less with $\Phi T0$ clock is removed as noise, and a signal with 9 cycles or more is valid. 100: A signal with 2 cycles or less with transfer clock is removed as noise, and a signal with 3 cycles or more is valid. 101: A signal with 3 cycles or less with transfer clock is removed as noise, and a signal with 4 cycles or more is valid. 110: A signal with 4 cycles or less with transfer clock is removed as noise, and a signal with 5 cycles or more is valid. 111: A signal with 5 cycles or less with transfer clock is removed as noise, and a signal with 6 cycles or more is valid. For the details of the Noise removal, refer to "3.5.3 Noise removal of RXD input".
11	-	0	R	Reads as "0".
10	CTSE	0	R/W	CTS handshake function 0: Disabled. 1: Enabled.
9	RTSE	0	R/W	RTS handshake function 0: Disabled. 1: Enabled.
8	WU	0	R/W	Wake-up function 0: Disabled. 1: Enabled. This setting is available only for the 9-bit mode. It is ignored in the other modes. If it is set to "1" (Enabled) and the 9th bit of the reception data is "1", the corresponding reception interrupt is generated.
7	-	0	R	Reads as "0".
6	IV	0	R/W	Data signal inversion 0: Disabled. 1: Enabled.

Bit	Bit Symbol	After Reset	Type	Function
5	DIR	0	R/W	Data transfer order 0: LSB first 1: MSB first
4	SBLLEN	0	R/W	STOP bit length 0: 1-bit 1: 2-bit
3	EVEN	0	R/W	Even parity selection 0: Odd parity 1: Even parity
2	PE	0	R/W	Parity addition 0: Disabled. 1: Enabled.
1:0	SM[1:0]	00	R/W	Data length 00: 7-bit 01: 8-bit 10: 9-bit 11: Reserved.

Note: This register cannot be rewritten during the data transmission and the data reception. This register is rewritable if *[UARTxSR] <SUE>* (Setting enable status flag) =0 (Setting is enabled).

4.2.3. [UARTxCR1](Control Register1)

Bit	Bit Symbol	After Reset	Type	Function
31:15	-	0	R	Reads as "0".
14:12	TIL[2:0]	000	R/W	Transmission Fill level setting 000: 0 stages 001: 1 stage 111: 7 stages This sets the Fill level where the transmission interrupt is generated.
11	-	0	R	Reads as "0".
10:8	RIL[2:0]	001	R/W	Reception Fill level setting 000: 8 stages 001: 1 stage 111: 7 stages This sets the Fill level where the reception interrupt is generated.
7	INTTXFE	0	R/W	Transmit FIFO interrupt control 0: Disabled. 1: Enabled.
6	INTTXWE	0	R/W	Transmission completion interrupt control 0: Disabled. 1: Enabled.
5	INTRXFE	0	R/W	Receive FIFO interrupt control(Note 1) 0: Disabled. 1: Enabled.
4	INTRXWE	0	R/W	Reception completion interrupt control(Note 1) 0: Disabled. 1: Enabled.
3	-	0	R	Reads as "0".
2	INTERR	0	R/W	Error interrupt control 0: Disabled. 1: Enabled.
1	DMATE	0	R/W	Transmission DMA control 0: Disabled. 1: Enabled.
0	DMARE	0	R/W	Reception DMA control 0: Disabled. 1: Enabled.

Note 1: Please do not enable <INTRXWE> and <INTRXFE> at the same time.

Note 2: This register cannot be rewritten during the data transmission and the data reception. This register is rewritable if [UARTxSR] <SUE>(Setting enable status flag) =0 (Setting is enabled).

4.2.4. [UARTxCLK] (Clock Control Register)

Bit	Bit Symbol	After Reset	Type	Function
31:8	-	0	R	Reads as "0".
7:4	PRSEL[3:0]	0000	R/W	Prescaler dividing ratio selection 0000: 1/1 0110: 1/64 0001: 1/2 0111: 1/128 0010: 1/4 1000: 1/256 0011: 1/8 1001: 1/512 0100: 1/16 1010 to 1111: Inhibited setting. 0101: 1/32
3:2	-	0	R	Reads as "0".
1:0	CKSEL[1:0]	00	R/W	Clock selection of baud rate generator 00: Prescaler dividing clock (Φ_{Tx}) 01: Timer output (UARTxCKINA) 10: Reserved 11: Reserved

Note: This register cannot be rewritten during the data transmission and the data reception. This register is rewritable if [UARTxSR] <SUE>(Setting enable status flag) =0 (Setting is enabled).

4.2.5. [UARTxBRD] (Baud Rate Register)

Bit	Bit Symbol	After Reset	Type	Function
31:24	-	0	R	Reads as "0".
23	KEN	0	R/W	$N + (64 - K) / 64$ dividing control 0: Disabled. 1: Enabled.
22	-	0	R	Reads as "0".
21:16	BRK[5:0]	000000	R/W	K value setting of the $N + (64 - K) / 64$ dividing 000000: K =0 000001: K =1 000010: K =2 111111: K =63
15:0	BRN[15:0]	0x0000	R/W	N value setting of the $N + (64 - K) / 64$ dividing or N dividing. 0x0000: Inhibited setting. 0x0001: N =1 0x0002: N =2 0xFFFF: N =65535

Note: This register cannot be rewritten during the data transmission and the data reception. This register is rewritable if [UARTxSR] <SUE>(Setting enable status flag) =0 (Setting is enabled).

4.2.6. [UARTxTRANS] (Transfer Enable Register)

Bit	Bit Symbol	After Reset	Type	Function
31:4	-	0	R	Reads as "0".
3	BK	0	R/W	Break transmission 0: No transmission is done. 1: Transmission is done. When this bit is set to "1", the Low level is output. When this bit is set to "0", the transmission stops. If [UARTxCRO]<IV>(Data signal inversion) is "1" to invert the data, the High level is output.
2	TXTRG	0	R/W	Trigger transmission control 0: Disabled. 1: Enabled. Do not change <TXTRG> during transmission. Set <TXE> to "0" and check [UARTxSR] <TXRUN> =0 (operation stop) and then change. For the selection of the trigger input, refer to "Product Information" of the reference manual.
1	TXE	0	R/W	Transmission control 0: Disabled. 1: Enabled.
0	RXE	0	R/W	Reception control 0: Disabled. 1: Enabled.

4.2.7. [UARTxDR] (Data Register)

Bit	Bit Symbol	After Reset	Type	Function
31:19	-	0	R	Reads as "0".
18	PERR	0	R	Parity error(Note) 0: No errors. 1: Error occurs. The write to this bit is ignored.
17	FERR	0	R	Framing error(Note) 0: No errors. 1: Error occurs. The write to this bit is ignored.
16	BERR	0	R	Break error flag 0: No errors. 1: Error occurs. The write of this bit is ignored.
15:9	-	0	R	Reads as "0".
8:0	DR[8:0]	Undefined.	R	Reception data read. This field should not read when no reception data is present.
			W	Transmission data write.

Note: <PERR>,<FERR> is masked when a break error occurs.

4.2.8. [UARTxSR] (Status Register)

Bit	Bit Symbol	After Reset	Type	Function											
31	SUE	0	R	<p>Setting enable status flag</p> <p>0: Setting is enabled. 1: Setting is disabled.</p> <p>When <SUE> is "0", the UART does neither data transmission nor data reception. The registers can be updated.</p> <p>Note: Target registers are following. [UARTxCR0], [UARTxCR1], [UARTxCLK], [UARTxBRD], and [UARTxFIFOCLR].</p> <p><SUE> becomes "0" when the followings occur.</p> <ol style="list-style-type: none"> 1. Reset is input. 2. Software reset is asserted. 3. The data transmission and the data reception complete after [UARTxTRANS]<TXE> and <RXE> are set to "0", respectively. 											
30:16	-	0	R	Reads as "0".											
15	TXRUN	0	R	<p>Transmission operating flag</p> <p>0: Stop 1: Operating</p> <p>This bit is the status flag which shows the transmission is operating. The following status is set by the combination of <TXRUN> and <TLVL> bits.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th><TXRUN></th> <th><TLVL></th> <th>Status</th> </tr> </thead> <tbody> <tr> <td rowspan="2" style="text-align: center;">0</td> <td style="text-align: center;">Other than 0000</td> <td>Stop or Wait for the next transmission</td> </tr> <tr> <td style="text-align: center;">0000</td> <td>Transmission completes and the transmit FIFO is empty.</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">-</td> <td>Transmission is operating.</td> </tr> </tbody> </table> <p><TXRUN> is set when data is present in the transmission shift register even though the transmit FIFO is empty.</p>	<TXRUN>	<TLVL>	Status	0	Other than 0000	Stop or Wait for the next transmission	0000	Transmission completes and the transmit FIFO is empty.	1	-	Transmission is operating.
<TXRUN>	<TLVL>	Status													
0	Other than 0000	Stop or Wait for the next transmission													
	0000	Transmission completes and the transmit FIFO is empty.													
1	-	Transmission is operating.													
14	TXEND	0	R	<p>Transmission completion flag</p> <p>0: - 1: Transmission completion</p> <p>This flag is set when one frame transmission completes.</p>											
			W	<p>Flag clear</p> <p>0: - 1: Flag clear.</p> <p>Write of "1" clears this bit.</p>											
13	TXFF	0	R	<p>Transmit FIFO flag</p> <p>0: - 1: Data count reaches the set transmission Fill level.</p> <p>This bit is set when the stage count of the stored data becomes the set value of Fill level (the [UARTxCR1]<TIL> value) from <TIL>+1.</p>											
			W	<p>Flag clear</p> <p>0: - 1: Flag clear.</p> <p>Write of "1" clears this bit.</p>											
12	-	0	R	Reads as "0".											
11:8	TLVL[3:0]	0000	R	<p>Transmit FIFO data storage level</p> <p>This field shows the current stage count of the data stored in the transmit FIFO.</p>											

Bit	Bit Symbol	After Reset	Type	Function		
7	RXRUN	0	R	Reception operating flag 0: Stop 1: Operating The status flag which shows the reception is operating. The following status is set by the combination of <RXRUN> and <RLVL> bits.		
				<RXRUN>	<RLVL>	Status
				0	Other than 1000	Stop or Wait for the next reception
				1	1000	Receive FIFO is full and the reception completes.
1	-	Reception is operating.				
6	RXEND	0	R	Reception completion flag 0: - 1: Reception completion This flag is set to "1" when one frame reception completes.		
			W	Flag clear 0: - 1: Flag clear. Write of "1" clears this bit.		
5	RXFF	0	R	Receive FIFO flag 0: - 1: Data count reaches the set reception Fill level. This bit is set when the stage count of the stored data stage becomes the [UARTxCR1]<RIL> value (the set value of Fill level) from <RIL>-1.		
			W	Flag clear 0: - 1: Flag clear. Write of "1" clears this bit.		
4	-	0	R	Reads as "0".		
3:0	RLVL[3:0]	0000	R	Receive FIFO data storage level This bit shows the current stage count of the data stored in the receive FIFO.		

4.2.9. [UARTx FIFOCLR] (FIFO Clear Register)

Bit	Bit Symbol	After Reset	Type	Function
31:2	-	0	R	Reads as "0".
1	TFCLR	0	W	Transmission buffer clear 0: - 1: Clear When this bit is written to "1", the read/write pointer of the transmit FIFO are initialized. When it is read, "0" is returned.
0	RFCLR	0	W	Reception buffer clear 0: - 1: Clear When this bit is written to "1", the read/write pointer of the receive FIFO are initialized. When it is read, "0" is returned.

Note: This register cannot be rewritten during the data transmission and the data reception. This register is rewritable if [UARTxSR]<SUE> =0 (Setting is enabled).

4.2.10. [UARTxERR] (Error Register)

Bit	Bit Symbol	After Reset	Type	Function
31:5	-	0	R	Reads as "0".
4	TRGERR	0	R	Trigger transmission error flag 0: No errors. 1: Error occurs. This is set to "1" when the data transmission cannot be started by the trigger because of no data in the transmit FIFO.
			W	Flag clear 0: - 1: Flag clear. Write of "1" clears this bit.
3	OVRERR	0	R	Overrun error flag 0: No errors. 1: Error occurs. This is set to "1" when an overrun error occurs.
			W	Flag clear 0: - 1: Flag clear. Write of "1" clears this bit. (Note3)
2	PERR	0	R	Parity error flag(Note 1) 0: No errors. 1: Error occurs. This is set to "1" when a parity error occurs.
			W	Flag clear 0: - 1: Flag clear. Write of "1" clears this bit.
1	FERR	0	R	Framing error flag(Note 1) 0: No errors. 1: Error occurs. This is set to "1" when a framing error occurs.
			W	Flag clear 0: - 1: Flag clear. Write of "1" clears this bit.
0	BERR	0	R	Break error flag 0: No errors. 1: Error occurs. This is set to "1" when a break error occurs.
			W	Flag clear 0: - 1: Flag clear. Write of "1" clears this bit.

Note 1: <PERR>, <FERR> is masked when a break error occurs.

Note 2: If error occurrence and flag clearing are simultaneous, clearing takes precedence.

Note 3: For the procedure for clearing the overrun flag, refer to "3.5.2 Reception Error Handling".

5. Usage Example

5.1. Baud Rate Setting Value

The following shows samples of the baud rate setting values using the clock frequency Φ_{Tx} . The deviation of Φ_{Tx} is not included.

Table 5.1 Setting example at $\Phi_{Tx} = 40\text{MHz}$, $[UARTxCLK]\langle PRSEL \rangle = 0000$, and $[UARTxBRD]\langle KEN \rangle = 1$

Baud Rate (bps)	Setting K value $\langle BRK \rangle$	Setting N value $\langle BRN \rangle$	Calculated Value (bps)
9600	0x25	0x104	9600
	0x26		
19200	0x32	0x082	19198
	0x33		19201
38400	0x39	0x041	38397
	0x3A		38406
57600	0x26	0x02B	57595
	0x27		57616
62500	0x00	0x027	62500
76800	0x1C	0x020	76775
	0x1D		76812
115200	0x13	0x015	115191
	0x14		115274
128000	0x1E	0x013	128000

Table 5.2 Setting example at $\Phi_{Tx} = 80\text{MHz}$, $[UARTxCLK]\langle PRSEL \rangle = 0000$, and $[UARTxBRD]\langle KEN \rangle = 1$

Baud Rate (bps)	Setting K value $\langle BRK \rangle$	Setting N value $\langle BRN \rangle$	Calculated Value (bps)
9600	0x0A	0x208	9600
	0x0B		
19200	0x25	0x104	19200
38400	0x32	0x082	38397
	0x33		38402
57600	0x0C	0x056	57595
	0x0D		57606
62500	0x00	0x04F	62500
76800	0x39	0x041	76794
	0x3A		76812
115200	0x26	0x02B	115191
	0x27		115232
128000	0x3C	0x027	128000

6. Precautions

- In some products, the UTxRTS_N pin or the UTxCTS_N pin may not be assigned. The corresponding functions should not be used in those products.
- The registers which are not assigned should not be accessed.
- The trigger input depends on the product when the trigger transmission control is used. Refer to "Product Information" of the reference manual.

7. Revision History

Table 7.1 Revision history

Revision	Date	Description
1.0	2018-09-20	First release
1.1	2019-07-26	- 3.5.2 modified the contents of procedure when the overrun error occurs. - 4.2.8 modified the "0" writing operation of bit 14/13/6/5 (Don't care → -) - 4.2.9 modified the "0" writing operation of bit 1/0 (Don't care → -) - 4.2.10 modified the "0" writing operation of bit 4/3/2/1/0 (Don't care → -)

RESTRICTIONS ON PRODUCT USE

Toshiba Corporation and its subsidiaries and affiliates are collectively referred to as "TOSHIBA". Hardware, software and systems described in this document are collectively referred to as "Product".

- TOSHIBA reserves the right to make changes to the information in this document and related Product without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, lifesaving and/or life supporting medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, and devices related to power plant. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative or contact us via our website.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**