CMOS Digital Integrated Circuit Silicon Monolithic

TMPM4K Group(2)

LQFP144 20x20mm, 0.5mm pitch
LQFP100 14x14mm, 0.5mm pitch
LQFP80 14x14mm, 0.65mm pitch
LQFP80 12x12mm, 0.5mm pitch
LQFP64 12x12mm, 0.65mm pitch
LQFP64 10x10mm, 0.5mm pitch

LQFP128 14x20mm, 0.5mm pitch
QFP100 14x20mm, 0.65mm pitch

General Description

- Arm® Cortex®-M4 processor with FPU
  Operation frequency: 1 to 160 MHz, Operation voltage: 2.7 to 5.5 V
- Code flash: 128 to 512 KB, Data flash: 32KB
- Package: 64-pin to 144-pin. 8 types of packages are available.
- Hardware IPs such as A-VE+, 12-bit ADC, and A-PMD are provided for implementation of vector control and PFC control

Applications

Motors, major appliances using motors, and industrial equipment.

Features

- Arm Cortex-M4 processor with FPU
  - Operation frequency: 1 to 160 MHz
  - Memory Protection Unit (MPU)
- Low-power consumption mode
  - Operation voltage: 2.7 to 5.5 V
  - Low-power consumption operation: IDLE, STOP1
- Operation temperature: -40 to +105°C
- Internal memory
  - Code flash: 128 to 512 KB, rewritable up to 10,000 times
  - Data flash: 32KB rewritable up to 100,000 times
  - Data flash is rewritable in parallel with instruction execution
  - RAM: 24KB, with parity
- Clock
  - External high speed oscillator: 6 to 12 MHz(Ceramic, Crystal)
  - External high speed clock input: 6 to 10 MHz
  - Internal high speed oscillator (IHOSC1): 10 MHz, user trimming function
  - PLL: 160 MHz output(System clock)
- Oscillation frequency detection (OFD): Abnormal system clock detection
- Voltage Detection (LVD): 8 level, Generate interrupts and reset outputs
- Interruption
  - External: 15 to 22 factors, with DNF
  - Internal: 95 to 105factors
- I/O ports: 51 to 131 (Input:2, Output:1)
  - 5V-tolerant, open-drain, pull-up/-down
- On-chip debug (JTAG/SW), NBDIF(RAM monitor)
- Trigger Selector (TRGSEL)
  - Expand Trigger request for DMAC, Timer, others
- DMA controller (DMAC): 1 unit
  - DMA requests: 30 to 32 factors, internal/external triggers
- CRC Calculation Circuit (CRC): CRC32, CRC16
- Asynchronous Serial Interface (UART): 3 to 4 channels
  - 5Mbps(Max), FIFO(Transmitter 8-stage, Receive 8-stage)
- Serial Peripheral Interface (TSPI): 2 channels
  - SIO/SPI mode, 10Mbps(MAX), FIFO(Transmitter: 16bitx8, Receive: 16bitx8)
- I^2C Interface (I^2C): 2 channels, Multi Master
- CAN controller (CAN): 0 to 1 channel
  - Version2.0B Active, 32 mailbox, MAX 1Mbps
- 12-bit Analog to Digital Converter (ADC): 14 to 32 inputs in 3 units
  - Conversion time: 1.0 μs at ADCLK=160MHz
  - Self-diagnosis support function
- Operational Amplifier (OPAMP): 3 channels
  - Gain selectable
- Advanced programmable motor control circuit (A-PMD): 3 channels
  - 3-phase complementary PWM output, Synchronized with ADC
  - PFC control: support 3-phase interleaved PFC
  - Emergency stop function by external inputs (EMG pin, OVV pin)
- Advanced vector engine plus (A-VE+): 1 channel
  - Vector control coprocessor cooperates with ADC/A-PMD
  - 1-shunt current detection area can be enlarged
  - Dead time compensation control, non-interference control
- Advanced Encoder input circuit (32-bit) (A-ENC32): 1 to 3 channels
  - Encoder/sensor (3 types)/Timer /Phase counter mode

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Start of commercial production
2019-05

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- 32-bit Timer Event Counter (T32A)
  - 6 channels as 32-bit Timers, 12 channels as 16-bit Timers
  - Interval Timer, event counter, input capture, phase difference input, PPG output, Sync Start, Trigger start
- Watchdog timer (SIWDT): 1 channel
  - Clock system other than the system clock can be selected
  - Clear window, interrupts and reset output

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Products Lists Categorized by Functions

The product under development is contained in this table.
For the newest status of each product, Please contact your sales representative.

Table.1 Products Lists

Built-in Functions		TMPM4KQFDFG TMPM4KQFYFG TMPM4KQFWFG	TMPM4KPFDDFG TMPM4KPFYDFG TMPM4KPFWDFG	TMPM4KNFDDFG TMPM4KNFYDFG TMPM4KNFWDFG	TMPM4KMFDDFG TMPM4KMFYDFG TMPM4KMFWDFG	TMPM4KLFDUG TMPM4KLFYUG TMPM4KLFWUG
				TMPM4KNFDFG TMPM4KNFYFG TMPM4KNFWFG	TMPM4KMFDFG TMPM4KMFYFG TMPM4KMFWFG	TMPM4KLFDFG TMPM4KLFYFG TMPM4KLFWFG
Memory	Code Flash (KB)	512 256 128	512 256 128	512 256 128	512 256 128	512 256 128
	Data Flash (KB)	32	32	32	32	32
	RAM (KB)	24	24	24	24	24
I/O port	PORT(pin)	131	115	87	67	51
External interrupt	INT (pin)	22	21	20	18	15
DMA	DMAC (ch)	32	32	32	32	30
Timer function	T32A (ch)	6	6	6	6	6
Serial communication function	UART (ch)	4	4	4	4	3
	I^2C (ch)	2	2	2	2	2
	TSPI(SIO) (ch)	2	2	2	2	2
	CAN (ch)	1	1	1	N/A	N/A
Analog function	12-bit ADC Unit A/B/C (AIN ch)	16/8/8	16/8/8	11/5/6	8/5/4	8/3/3
	OPAMP (Unit)	3	3	3	3	3
Motor control peripherals	A-VE+ (ch)	1	1	1	1	1
	A-PMD (ch)	3	3	3	3	3
	A-ENC32 (ch)	3	3	3	2	1
Other peripherals	CRC (ch)	1	1	1	1	1
	RAMP (ch)	2	2	2	2	2
System function	LVD	1	1	1	1	1
	WDT (ch)	1	1	1	1	1
	OFD	1	1	1	1	1
	POR	1	1	1	1	1
Debug interface	Debug	JTAG/SW TRACE(4bits) NBDIF	JTAG/SW TRACE(4bits) NBDIF	JTAG/SW TRACE(4bits) NBDIF	SW	SW
Package	Package type	LQFP144 (20 mm x 20 mm, 0.5 mm pitch)	LQFP128 (14 mm x 20 mm, 0.5 mm pitch)	QFP100 (14 mm x 20 mm, 0.65 mm pitch)	LQFP80 (14 mm x 14 mm, 0.65 mm pitch)	LQFP64 (10 mm x 10 mm, 0.5 mm pitch)
				LQFP100 (14 mm x 14 mm, 0.5 mm pitch)	LQFP80 (12 mm x 12 mm, 0.5 mm pitch)	LQFP64 (12 mm x 12 mm, 0.65 mm pitch)

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Contents

General Description 1
Applications 1
Features 1
Products Lists Categorized by Functions 3
Contents 4
List of Figures 8
List of Tables 9
Preface 10
Conventions 10
Terms and Abbreviations 12
1. Block Diagram 13
2. Pin Assignment 14
2.1. LQFP144 14
2.2. LQFP128 15
2.3. QFP100 16
2.4. LQFP100 17
2.5. LQFP80 18
2.6. LQFP64 19
3. Memory Map 20
3.1. List of Memory Sizes 21
4. Pin Description 22
4.1. Functional Pin Name and Functions 22
4.1.1. Function Pins of Peripheral 22
4.1.2. Debug Pins 24
4.1.3. Control Pins 25
4.1.4. Power Supply Pins 25
4.1.5. Capacitors between power supply pins 26
4.2. Functional Pin and Ports Assignment (Pin Number) 27
4.3. Ports 35
4.3.1. Port Specification Table 36
5. Functional Description and Operation Description 41
5.1. Reference Manuals 41
5.2. Processor Core 42
5.2.1. Core Information 42
5.2.2. Configurable Options 42
5.3. Clock Control and Operation Mode (CG) 43
5.4. Flash Memory (Code FLASH, Data FLASH) 43
5.5. Oscillator 44

Not Recommended for New Design

5.6. Trimming Circuit (TRM) 44
5.7. Oscillation Frequency Detection Circuit (OFD) 44
5.8. Voltage Detection Circuit (LVD) 45
5.9. Digital Noise Filter circuit(DNF) 45
5.10. Debug Interface (DEBUG) 46
5.10.1. Non Break Debug Interface (NBDIF) 46
5.11. DMA Controller (DMAC) 47
5.12. Asynchronous Serial Communication Circuit (UART) 47
5.13. Serial Peripheral Interface (TSPI) 48
5.14. I2C Interface (I2C) 48
5.15. CAN controller (CAN) 48
5.16. 12-bit Analog to Digital Converter (ADC) 49
5.17. Operational Amplifier (OPAMP) 49
5.18. Advanced Programmable Motor Control Circuit (A-PMD) 50
5.19. Advanced Encoder Input Circuit (32-bit) (A-ENC32) 50
5.20. Advanced Vector Engine Plus (A-VE+) 51
5.21. 32-bit Timer Event Counter (T32A) 51
5.22. Clock Selective Watchdog Timer (SIWDT) 52
5.23. CRC Calculation Circuit (CRC) 52
5.24. RAM Parity (RAMP) 52
6. Equivalent Circuit 53
6.1. Port 53
6.2. Analog Reference pin 56
6.3. Control Pin 57
6.4. Clock control 57
7. Electrical Characteristics 58
7.1. Absolute Maximum Ratings 58
7.2. DC Electrical Characteristics (1/2) 60
7.3. DC Electrical Characteristics (2/2) 64
7.4. 12-bit AD Converter Characteristics 66
7.5. Operational Amplifier (OPAMP) Characteristics 67
7.6. Characteristics of Internal processing at RESET 68
7.7. Characteristics of Power on Reset 68
7.8. Characteristics of Voltage Detection Circuit 69
7.9. AC Electrical Characteristics 70
7.9.1. Serial Peripheral Interface (TSPI) 70
7.9.1.1. AC Measurement Conditions 70
7.9.1.2. AC Electrical Characteristics 70
7.9.2. I2C Interface (I2C) 77
7.9.2.1. AC Measurement Conditions 77
7.9.2.2. AC Electrical Characteristics 77

Not Recommended for New Design

7.9.3. 32-bit Timer Event Counter (T32A) 79
7.9.3.1. AC Measurement Conditions 79
7.9.3.2. AC Electrical Characteristics 79
7.9.4. External Interrupt 80
7.9.4.1. AC Measurement Conditions 80
7.9.4.2. AC Electrical Characteristics 80
7.9.5. Trigger Input (TRGINx) 81
7.9.5.1. AC Measurement Conditions 81
7.9.5.2. AC Electrical Characteristics 81
7.9.6. Debug Communication 82
7.9.6.1. AC Measurement Conditions 82
7.9.6.2. SW Interface 82
7.9.6.3. JTAG Interface 83
7.9.6.4. ETM Trace 84
7.9.6.5. Non Break Debug Interface (NBDIF) 85
7.9.7. Noise Filter Characteristics 86
7.9.8. External Clock Input 86
7.9.8.1. AC Measurement Conditions 86
7.9.8.2. AC Electrical Characteristics 86
7.10. Flash Memory Characteristics 87
7.10.1. Code Flash 87
7.10.2. Data Flash 87
7.10.3. Chip Erase 87
7.11. Regulator 88
7.12. Oscillation Circuit 89
7.12.1. Internal Oscillation 89
7.12.2. External Oscillator 89
7.12.3. Oscillation Circuit 89
7.12.4. Ceramic Oscillator 90
7.12.5. Crystal Oscillator 90
7.12.6. Precautions for designing printed circuit board 90
8. Package Dimensions 91
8.1. P-LQFP144-2020-0.50-002 91
8.2. P-LQFP128-1420-0.50-001 92
8.3. P-LQFP100-1414-0.50-002 93
8.4. P-QFP100-1420-0.65-001 94
8.5. P-LQFP80-1414-0.65-001 95
8.6. P-LQFP80-1212-0.50-003 96
8.7. P-LQFP64-1010-0.50-003 97
8.8. P-LQFP64-1212-0.65-001 98
9. Precautions 99
10. Revision History 100
Appendix 101

Not Recommended for New Design

List of All pins..... 101
Part Naming Conventions..... 104
RESTRICTIONS ON PRODUCT USE..... 105

Not Recommended for New Design

List of Figures

Figure 1.1 Block diagram of the TMPM4K Group(2) products 13
Figure 3.1 Example of the TMPM4KxFD 20
Figure 4.1 Capacitors for power supply pins connection circuit 26
Figure 7.1 Through rate 67
Figure 7.2 1st clock edge sampling (Master) 75
Figure 7.3 2nd clock edge sampling (Master) 75
Figure 7.4 2nd clock edge sampling (Slave) 76
Figure 7.5 AC timing of I2C 78
Figure 7.6 Count Pulse input 80
Figure 7.7 JTAG/SW waveform 83
Figure 7.8 Trace signal waveform 84
Figure 7.9 AC timing of NBDIF 85
Figure 7.10 External clock input waveform 86
Figure 7.11 Oscillation circuit sample 89

Not Recommended for New Design

List of Tables

Table.1 Products Lists ... 3
Table 3.1 Memory sizes and addresses ... 21
Table 4.1 Pin names and functions of peripheral pins ... 22
Table 4.2 Debug pin names and their function ... 24
Table 4.3 Control pin names and their function ... 25
Table 4.4 Power supply pin names and their function ... 25
Table 4.5 Signal connection List (1/8) ... 27
Table 4.6 Signal connection List (2/8) ... 28
Table 4.7 Signal connection List (3/8) ... 29
Table 4.8 Signal connection List (4/8) ... 30
Table 4.9 Signal connection List (5/8) ... 31
Table 4.10 Signal connection List (6/8) ... 32
Table 4.11 Signal connection List (7/8) ... 33
Table 4.12 Signal connection List (8/8) ... 34
Table 4.13 Pin numbers, and specifications of Port A, B, C, D ... 36
Table 4.14 Pin numbers, and specifications of Port E, F, G, H ... 37
Table 4.15 Pin numbers, and specifications of Port J, K, L ... 38
Table 4.16 Pin numbers, and specifications of Port M, N, P, R ... 39
Table 4.17 Pin numbers, and specifications of Port T, U, V, W ... 40
Table 5.1 Reference Manuals for TMPM4K Group(2) ... 41
Table 5.2 Core revision ... 42
Table 5.3 Configurable options and their implementations ... 42
Table 5.4 Built-in Oscillator ... 44
Table 5.5 Built-in TRM ... 44
Table 5.6 Built-in OFD ... 44
Table 5.7 Built-in LVD ... 45
Table 5.8 Number of External Interrupt (Built-in DNF) ... 45
Table 5.9 Built-in Debug Interface ... 46
Table 5.10 Built-in DMAC ... 47
Table 5.11 Built-in UART ... 47
Table 5.12 Built-in TSPI ... 48
Table 5.13 Built-in I^2C ... 48
Table 5.14 Built-in CAN ... 48
Table 5.15 Built-in ADC channel list ... 49
Table 5.16 Built-in OPAMP ... 49
Table 5.17 Built-in A-PMD ... 50
Table 5.18 Built-in A-ENC ... 50
Table 5.19 Built-in A-VE+ ... 51
Table 5.20 Built-in T32A ... 51
Table 5.21 Built-in SIWDT ... 52
Table 5.22 Built-in CRC ... 52
Table 5.23 Built-in RAMP ... 52
Table 7.1 Absolute maximum ratings ... 58
Table 7.2 Thermal resistance of IC package and maximum allowable power table ... 59
Table 7.3 I_{DD} measurement condition (Pin setting, Oscillation Circuit) ... 64
Table 7.4 I_{DD} measurement condition (CPU, Peripheral) ... 65
Table 10.1 Revision History ... 100

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Preface

Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1]***, ***[XYZ2]***, ***[XYZ3]*** → ***[XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, "x" means A, B, and C ...
  Example: ***[ADACR0]***, ***[ADBCR0]***, ***[ADCCR0]*** → ***[ADxCR0]***
  In case of channel, "x" means 0, 1, and 2 ...
  Example: ***[T32A0RUNA]***, ***[T32A1RUNA]***, ***[T32A2RUNA]*** → ***[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> =0x01 (hexadecimal), ***[XYZn]***<VW> =1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value.
  In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

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Terms and Abbreviations

Some of abbreviations used in this document are as follows:

ADC	Analog to Digital Converter
A-ENC32	Advanced Encoder Input Circuit (32-bit)
A-PMD	Advanced Programmable Motor Control Circuit
A-VE+	Advanced Vector Engine Plus
CAN	Controller Area Network
CRC	Cyclic Redundancy Check
DMAC	Direct Memory Access Controller
DNF	Digital Noise Filter
EHOSC	External High speed Oscillator
IHOSC	Internal High speed Oscillator
INT	Interrupt
I^2C	Inter-Integrated Circuit
LVD	Voltage Detection Circuit
NBDIF	Non Break Debug Interface
NMI	Non-Maskable Interrupt
OFD	Oscillation Frequency Detector
OPAMP	Operational Amplifier
POR	Power On Reset Circuit
RAMP	RAM parity
SIWDT	Clock Selective Watchdog timer
TRGSEL	Trigger Selection circuit
TRM	Trimming circuit
TSPI	Serial Peripheral Interface
T32A	32-bit Timer Event Counter
UART	Universal Asynchronous Receiver Transmitter

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1. Block Diagram

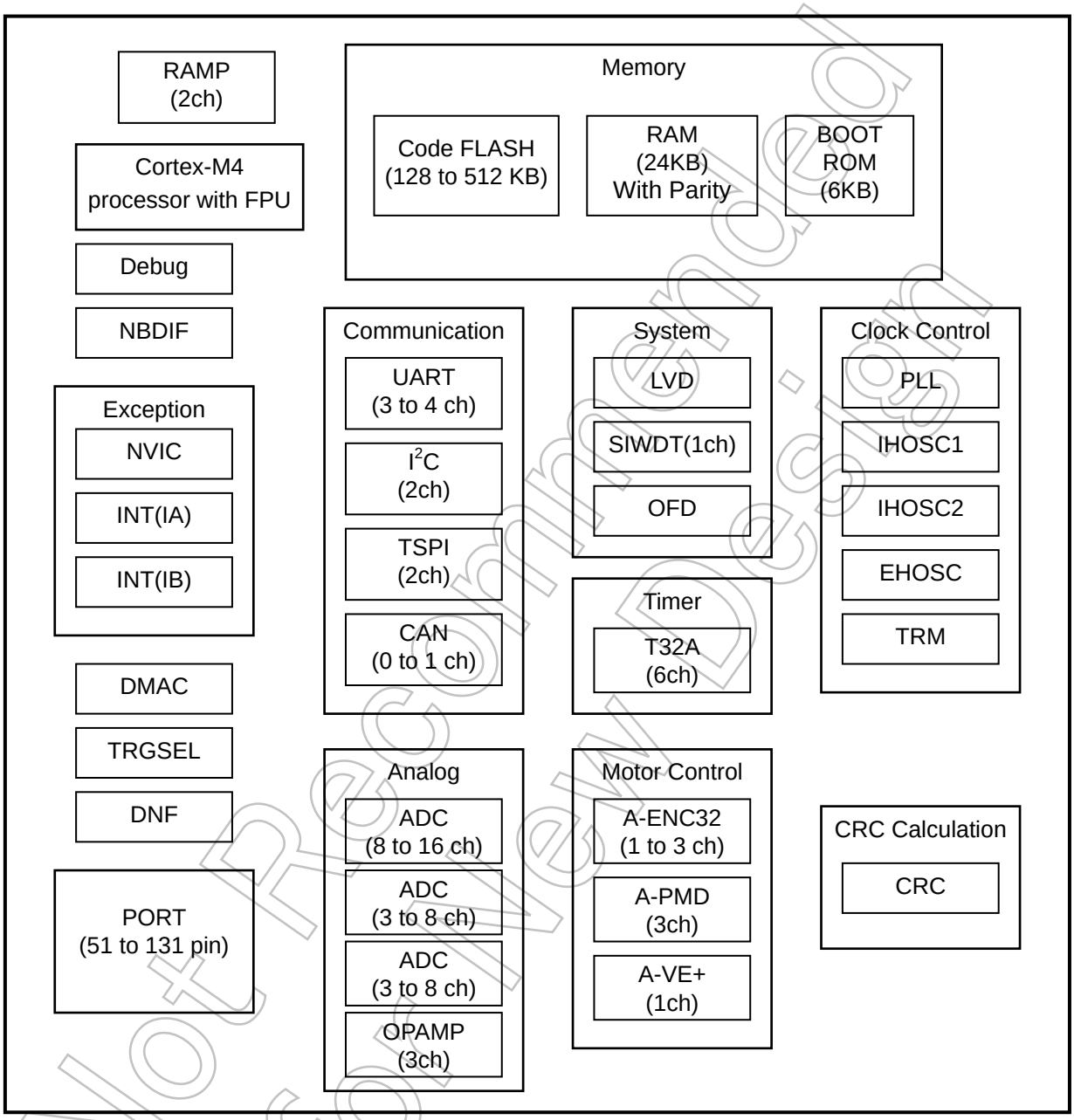

Figure 1.1 Block diagram of the TMPM4K Group(2) products

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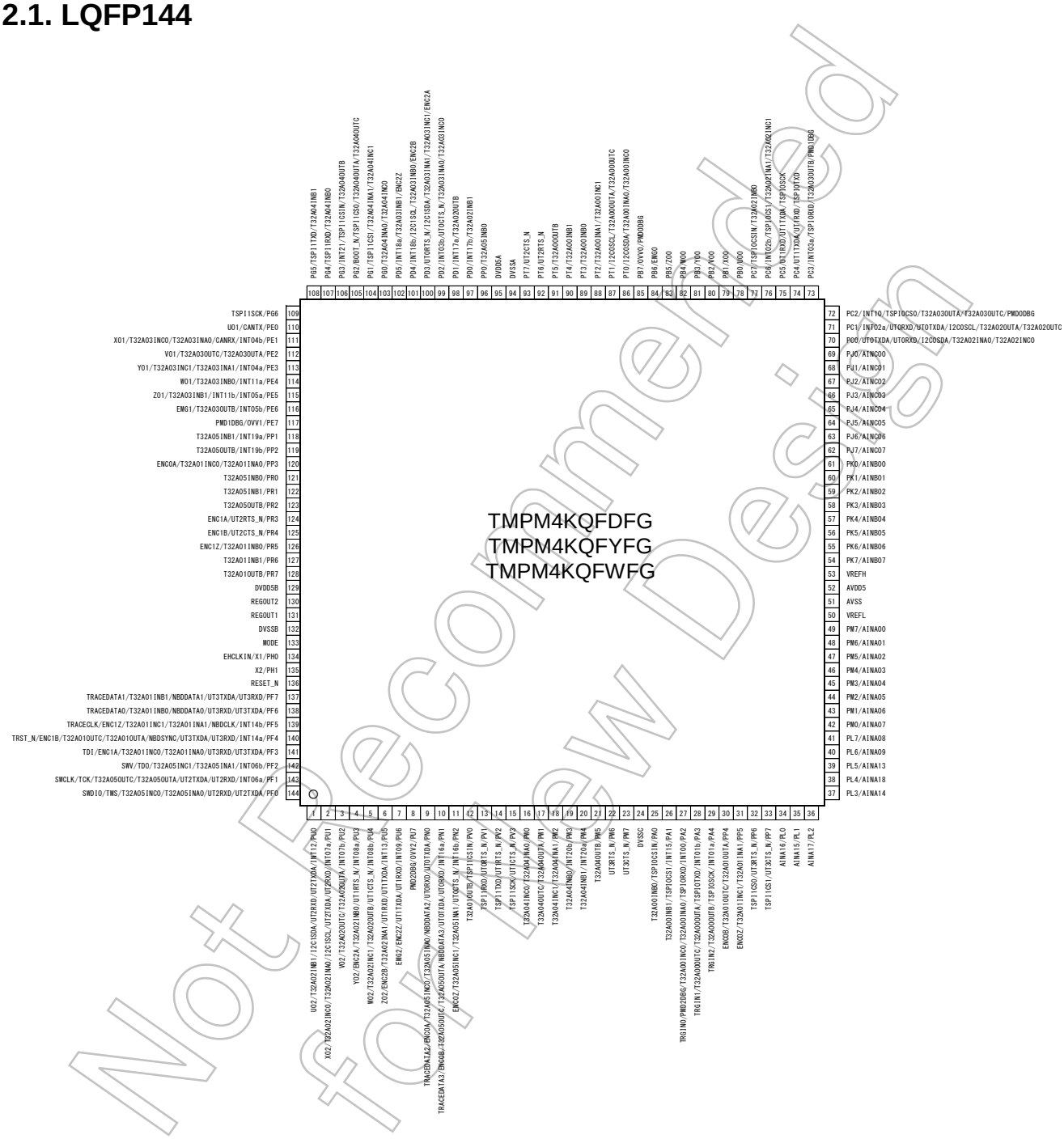
2. Pin Assignment

2.1. LQFP144



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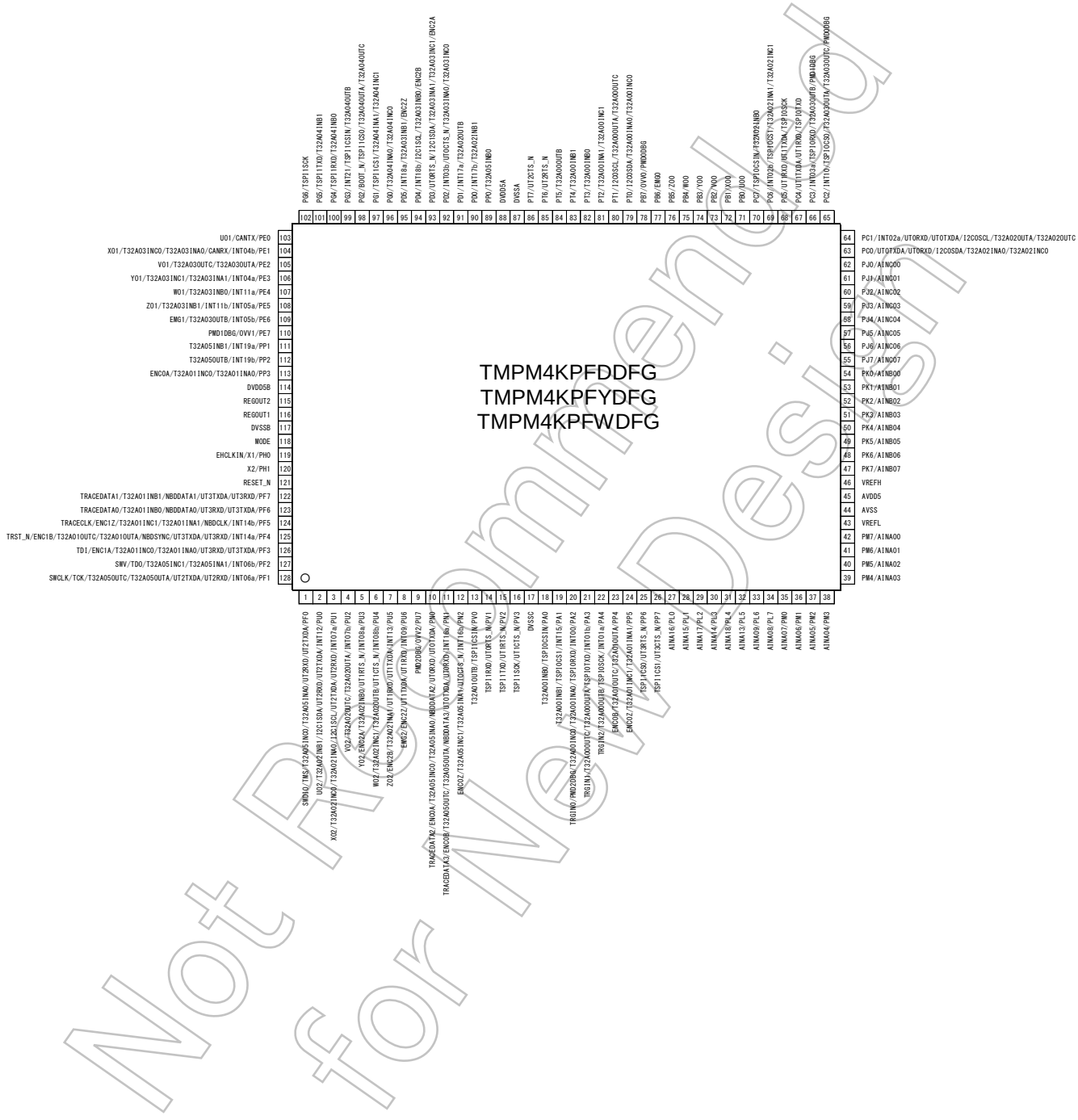
2.2. LQFP128



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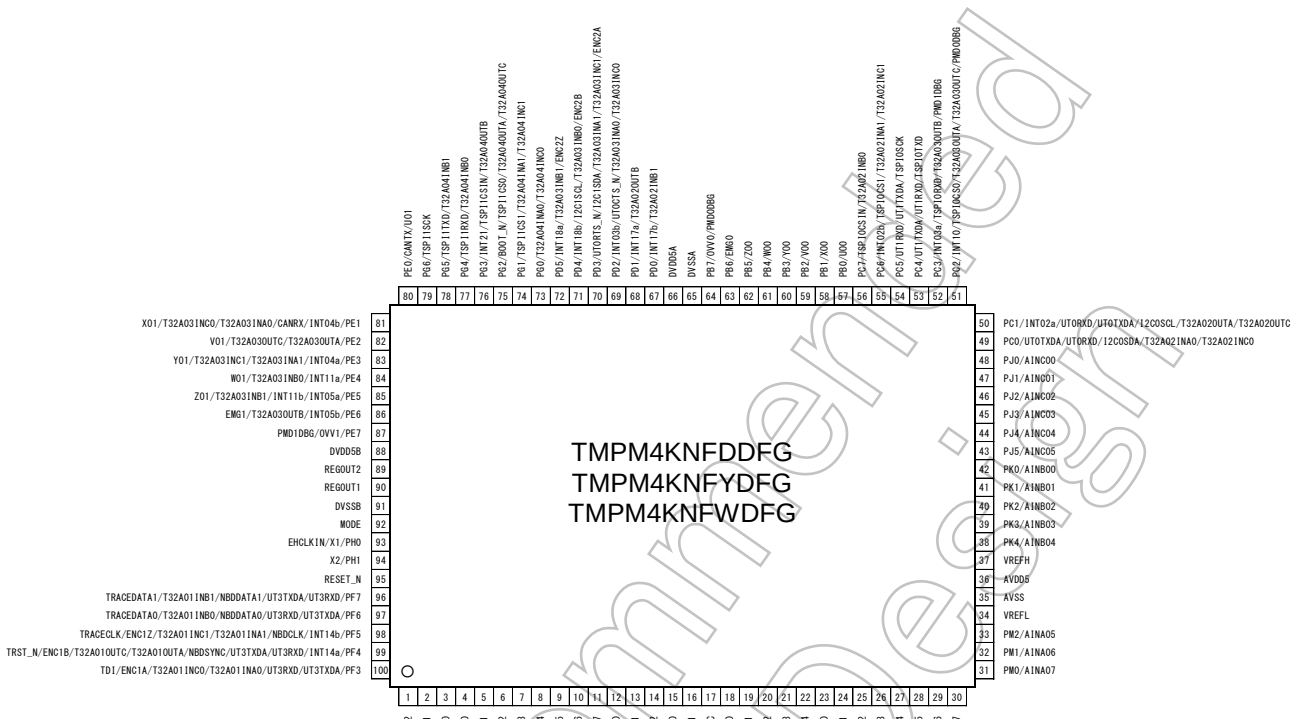
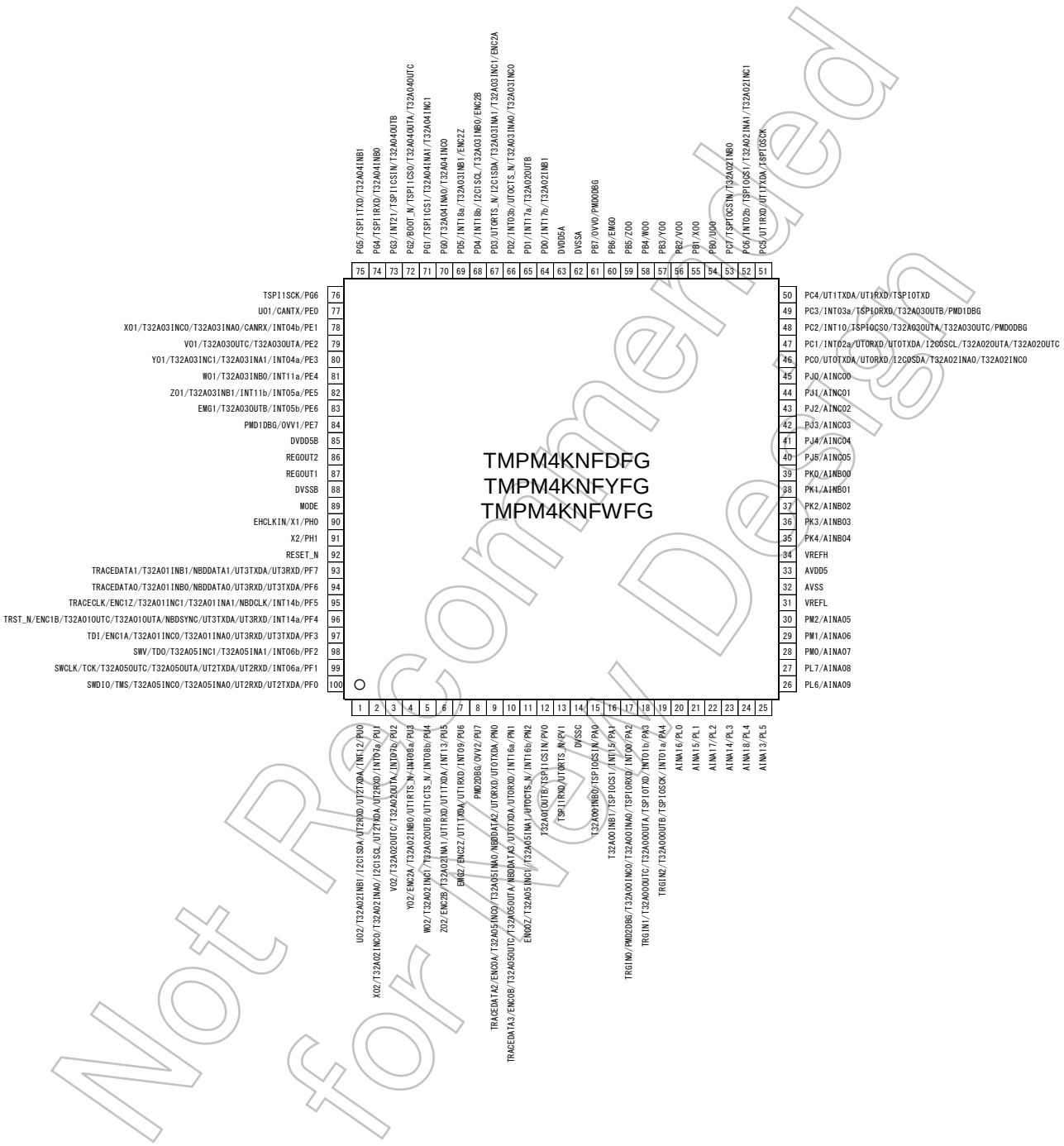
2.3. QFP100



Not Recommended for New Design

2.4. LQFP100



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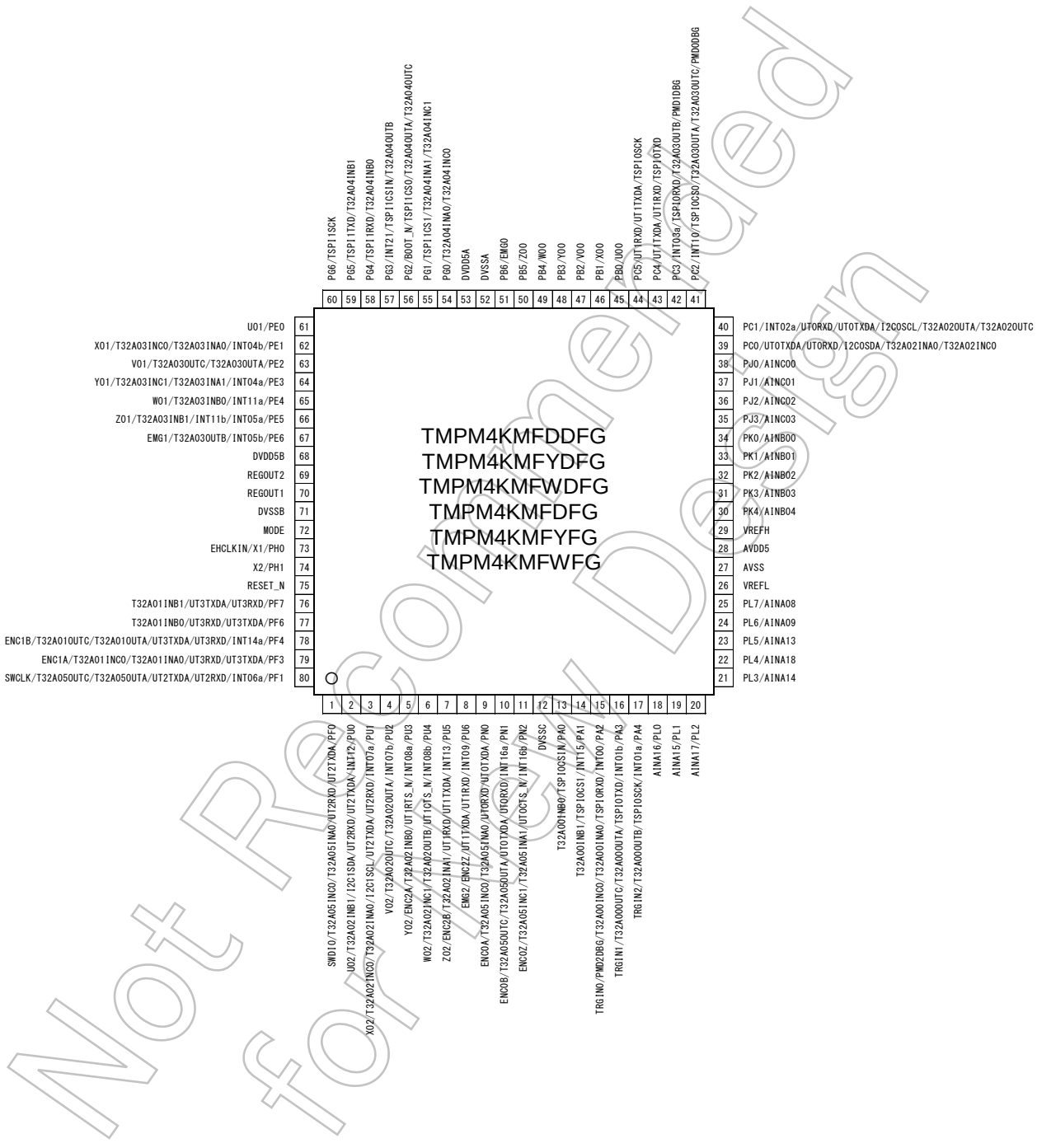
2.5. LQFP80



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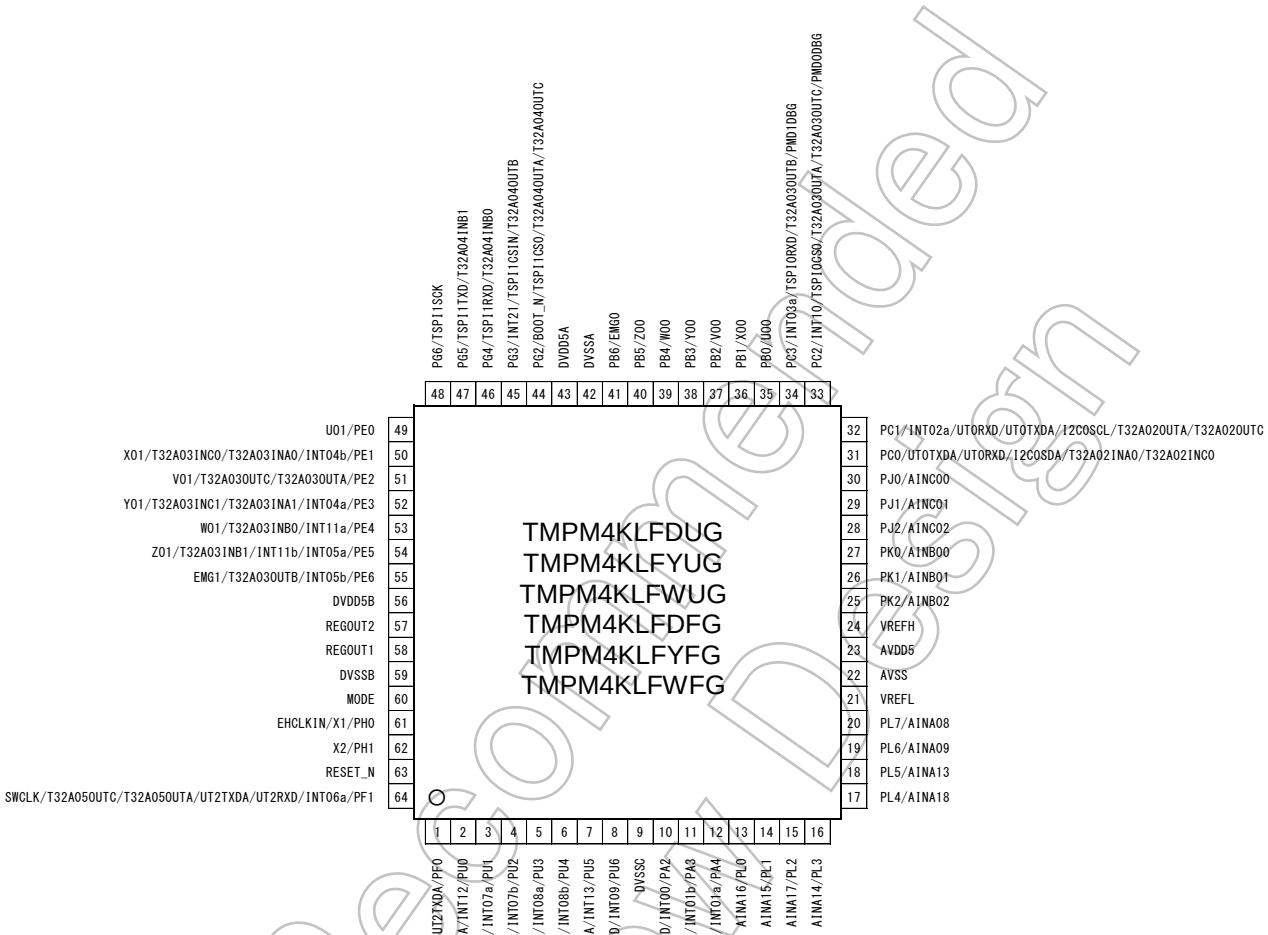
2.6. LQFP64



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3. Memory Map

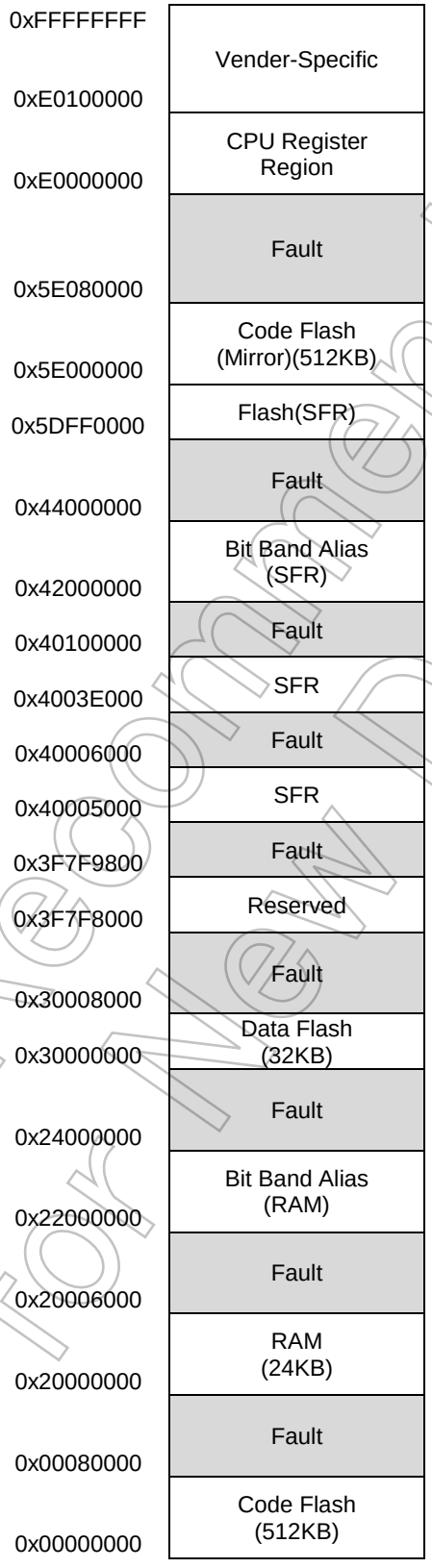

Figure 3.1 Example of the TMPM4KxFD

Note: Fault, Reserved: Please do not access their region.

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3.1. List of Memory Sizes

Table 3.1 Memory sizes and addresses

Products			TMPM4KQFDFG TMPM4KPFDDFG TMPM4KNFDDFG TMPM4KNFDFG TMPM4KMFDDFG TMPM4KMFDFG TMPM4KLFDUG TMPM4KLFDFG	TMPM4KQFYFG TMPM4KPFYDFG TMPM4KNFYDFG TMPM4KNFYFG TMPM4KMFYDFG TMPM4KMFYFG TMPM4KLFYUG TMPM4KLFYFG	TMPM4KQFWFG TMPM4KPFWDFG TMPM4KNFWDFG TMPM4KNFWFG TMPM4KMFWDFG TMPM4KMFWFG TMPM4KLFWUG TMPM4KLFWFG
Peripheral region	Code Flash (Mirror)	Size	512KB	256KB	128KB
		START	0x5E000000	0x5E000000	0x5E000000
		END	0x5E07FFFF	0x5E03FFFF	0x5E01FFFF
SRAM region	Data Flash	Size	32KB		
		START	0x30000000		
		END	0x30007FFF		
	RAM	Size	24KB		
		START	0x20000000		
		END	0x20005FFF		
Code region	Code Flash	Size	512KB	256KB	128KB
		START	0x00000000	0x00000000	0x00000000
		END	0x0007FFFF	0x00003FFF	0x00001FFF

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4. Pin Description

4.1. Functional Pin Name and Functions

4.1.1. Function Pins of Peripheral

Table 4.1 Pin names and functions of peripheral pins

Peripheral function	Pin name	Input or Output	Function
Interrupt control (IA/IB)	INTx	Input	External interrupt input pin External input pin provides the noise filter (filter width: Typ. 30 ns).
32-bit Timer event counter (T32A)	T32AxINA0	Input	16-bit timer A input capture input pin 0
	T32AxINA1	Input	16-bit timer A input capture input pin 1
	T32AxOUTA	Output	16-bit timer A output pin
	T32AxINB0	Input	16-bit timer B input capture input pin 0
	T32AxINB1	Input	16-bit timer B input capture input pin 1
	T32AxOUTB	Output	16-bit timer B output pin
	T32AxINC0	Input	32-bit timer input capture input pin 0
	T32AxINC1	Input	32-bit timer input capture input pin 1
	T32AxOUTC	Output	32-bit timer output pin
Serial peripheral interface (TSPI)	TSPIxCSIN	Input	Chip select input pin
	TSPIxCS0	Output	Chip select output pin 0
	TSPIxCS1	Output	Chip select output pin 1
	TSPIxRXD	Input	Data input pin
	TSPIxTXD	Output	Data output pin
	TSPIxSCK	I/O	Clock input/output pin
Asynchronous serial communication circuit (UART)	UTxRXD	Input	Data input pin
	UTxTXDA	Output	Data output pin A
	UTxCTS_N	Input	Transmission control input pin
	UTxRTS_N	Output	Transmission request output pin
I^2C interface (I^2C)	I2CxSDA	I/O	Data input/output pin
	I2CxSCL	I/O	Clock input/output pin
CAN Controller (CAN)	CANTX	Output	CAN data output pin
	CANRX	Input	CAN data input pin
Advanced Programmable Motor Control Circuit (A-PMD)	EMGx	Input	Emergency state detection input pin
	OVVx	Input	Overvoltage detection input pin
	UOx	Output	U-phase output pin
	VOx	Output	V-phase output pin
	WOx	Output	W-phase output pin
	XOx	Output	X-phase output pin
	YOx	Output	Y-phase output pin
	ZOx	Output	Z-phase output pin
	PMDxDBG	Output	Debug output pin for motor control

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Peripheral function	Pin name	Input or Output	Function
Advanced Encoder Input Circuit (32-bit) (A-ENC32)	ENCxA	Input	Encoder input pin A
	ENCxB	Input	Encoder input pin B
	ENCxZ	Input	Encoder input pin Z
Analog to Digital Converter (ADC)	AINAx, AINBx, AINCx	Input	Analog input pin
Trigger input (TRGSEL)	TRGINx	Input	External trigger input pin

Note: "x" means channel number or unit number or interrupt number.

Not Recommended for New Design

4.1.2. Debug Pins

Table 4.2 Debug pin names and their function

Debug PORT	Pin name	Input or Output	Function
JTAG	TMS	Input	JTAG test mode selection input pin
	TCK	Input	JTAG serial clock input pin
	TDO	Output	JTAG serial data output pin
	TDI	Input	JTAG serial data input pin
	TRST_N	Input	JTAG test reset input pin
SW	SWDIO	I/O	Serial wire data input/output pin
	SWCLK	Input	Serial wire clock input pin
	SWV	Output	Serial wire viewer output pin
TRACE	TRACECLK	Output	Trace clock output pin
	TRACEDATA0	Output	Trace data output pin 0
	TRACEDATA1	Output	Trace data output pin 1
	TRACEDATA2	Output	Trace data output pin 2
	TRACEDATA3	Output	Trace data output pin 3
NBDIF	NBDSYNC	Input	Non break debug synchronous input pin
	NBDCLK	Input	Non break debug clock input pin
	NBDDATA0	I/O	Non break debug data output pin 0
	NBDDATA1	I/O	Non break debug data output pin 1
	NBDDATA2	I/O	Non break debug data output pin 2
	NBDDATA3	I/O	Non break debug data output pin 3

Not Recommended for New Design

4.1.3. Control Pins

Table 4.3 Control pin names and their function

	Pin name	Input or Output	Function
Control Pin	X1	Input	High speed oscillator connection pin
	X2	Output	High speed oscillator connection pin
	EHCLKIN	Input	External Clock signal input pin
	BOOT_N	Input	BOOT mode control pin The BOOT mode control pin is sampled on the rising edge of the RESET_N input. It's not sampled by internal Reset factor. If the BOOT mode control pin is "Low" level, the MCU enters single-boot mode. If it is "High", the MCU enters single-chip mode. For details, refer to "Flash Memory" of Reference Manual.
	RESET_N	Input	Reset signal input pin
	MODE	Input	Mode Pin This pin must be fixed to "Low" level.

4.1.4. Power Supply Pins

Table 4.4 Power supply pin names and their function

	Pin name	Function
Power Supply	DVDD5A (Note1) DVDD5B (Note1)	Power supply pin for digital DVDD5A/B supplies the power to the following pins: PA to PH, PN, PP, PR, PT to PW, MODE, RESET_N, BOOT_N A power supply is supplied to an oscillating circuit from a built-in regulator. X1, X2
	DVSSA (Note2) DVSSB (Note2) DVSSC (Note2)	GND pin for digital
	REGOUT1 (Note3)	Capacitor for a regulator connection pin (Note4)
	REGOUT2 (Note3)	Capacitor for a regulator connection pin (Note4)
	AVDD5 VREFH	Power supply pin for analog and reference power pin for analog (VREFH). AVDD5 supplies the power to the following pins: PL, PM, PK, PJ
	AVSS VREFL	GND pin for analog and reference GND pin for analog (VREFL)

Note1: Apply the voltage to DVDD5A and DVDD5B at the same potential except the case that the pins are not provided.

Note2: Apply the external voltage to DVSSA, DVSSB, and DVSSC at the same potential except the case that the pins are not provided.

Note3: For REGOUT1 and REGOUT2, do not cause a short circuit with DVDD5A, DVDD5B, or DVSSA, DVSSB, or DVSSC.

Note4: For the capacitor value, refer to the "7.Electrical Characteristics"

Not Recommended for New Design

4.1.5. Capacitors between power supply pins

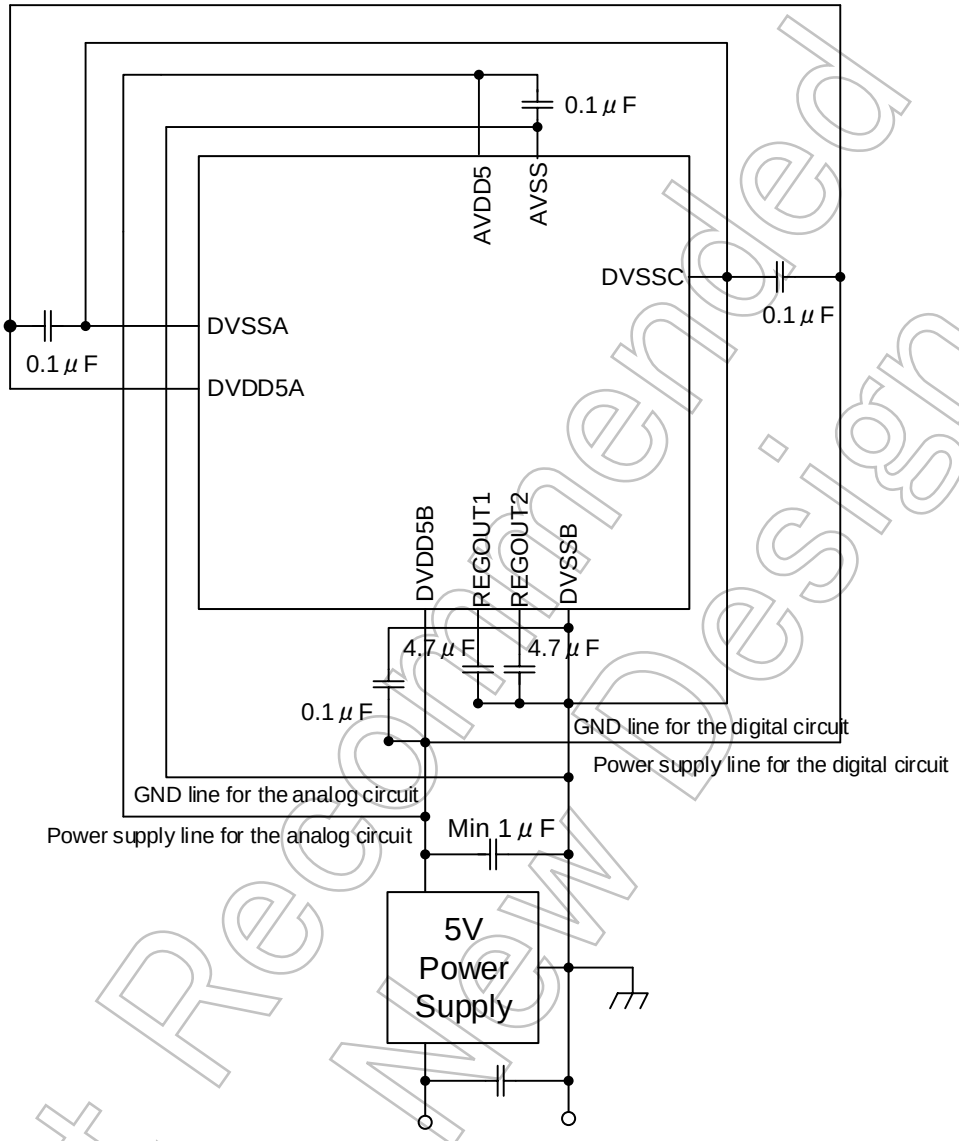


Figure 4.1 Capacitors for power supply pins connection circuit

Note1: 5V power supply output capacitor (min 1 µF) must be placed on the shortest distance from the DVDD5B, DVSSB.

Note2: 5V power supply and GND lines must be separated for the analog circuit and the digital circuit in near 5V power supply output capacitor (min 1 µF) between this capacitor and DVDD5B, DVSSB.

Note3: Power supply and GND lines must be bring close and be wired. When they are away, a power supply loop makes for power supply and GND lines through the capacitor of a power supply circuit, and they will be the antenna received high frequency noise.

Note4: Capacitors of REGOUT1 and REGOUT2 for regulators must be same capacity, and they must be placed on the shortest distance from DVSSB.

Note5: Use multilayer ceramic capacitors for the power supply output capacitor (1 µF or more) and regulator capacitors (4.7 µF).

Not Recommended for New Design

4.2. Functional Pin and Ports Assignment (Pin Number)

Following table shows a pin number of the port assignment and each product which were seen from the functional pin.

"-" means that it not have a pin or there is no assignment of a function.

Table 4.5 Signal connection List (1/8)

Function	Combination functional pin name	Port name	M4KQ (LQFP144)	M4KP (LQFP128)	M4KN (QFP100)	M4KN (LQFP100)	M4KM (LQFP80)	M4KL (LQFP64)
UART ch0	UT0RXD	PC0	70	63	49	46	39	31
		PC1	71	64	50	47	40	32
		PN0	9	10	12	9	9	-
		PN1	10	11	13	10	10	-
	UT0TXDA	PC1	71	64	50	47	40	32
		PC0	70	63	49	46	39	31
		PN1	10	11	13	10	10	-
		PN0	9	10	12	9	9	-
	UT0CTS_N	PD2	99	92	69	66	-	-
		PN2	11	12	14	11	11	-
	UT0RTS_N	PD3	100	93	70	67	-	-
		PV1	13	14	16	13	-	-
UART ch1	UT1RXD	PC4	74	67	53	50	43	-
		PC5	75	68	54	51	44	-
		PU5	6	7	9	6	7	7
		PU6	7	8	10	7	8	8
	UT1TXDA	PC5	75	68	54	51	44	-
		PC4	74	67	53	50	43	-
		PU6	7	8	10	7	8	8
		PU5	6	7	9	6	7	7
	UT1CTS_N	PU4	5	6	8	5	6	6
		PV3	15	16	-	-	-	-
	UT1RTS_N	PU3	4	5	7	4	5	5
		PV2	14	15	-	-	-	-
UART ch2	UT2RXD	PF0	144	1	3	100	1	1
		PF1	143	128	2	99	80	64
		PU0	1	2	4	1	2	2
		PU1	2	3	5	2	3	3
	UT2TXDA	PF1	143	128	2	99	80	64
		PF0	144	1	3	100	1	1
		PU1	2	3	5	2	3	3
		PU0	1	2	4	1	2	2
	UT2CTS_N	PR4	125	-	-	-	-	-
		PT7	93	86	-	-	-	-
	UT2RTS_N	PR3	124	-	-	-	-	-
		PT6	92	85	-	-	-	-
UART ch3	UT3RXD	PF3	141	126	100	97	79	-
		PF4	140	125	99	96	78	-
		PF6	138	123	97	94	77	-
		PF7	137	122	96	93	76	-
	UT3TXDA	PF4	140	125	99	96	78	-
		PF3	141	126	100	97	79	-
		PF7	137	122	96	93	76	-
		PF6	138	123	97	94	77	-
	UT3CTS_N	PP7	33	26	-	-	-	-
		PW7	23	-	-	-	-	-
	UT3RTS_N	PP6	32	25	-	-	-	-
		PW6	22	-	-	-	-	-

Not Recommended for New Design

Table 4.6 Signal connection List (2/8)

Function	Combination functional pin name	Port name	M4KQ (LQFP144)	M4KP (LQFP128)	M4KN (QFP100)	M4KN (LQFP100)	M4KM (LQFP80)	M4KL (LQFP64)
I²C ch0	I2C0SDA	PC0	70	63	49	46	39	31
		PT0	86	79	-	-	-	-
	I2C0SCL	PC1	71	64	50	47	40	32
		PT1	87	80	-	-	-	-
I²C ch1	I2C1SDA	PD3	100	93	70	67	-	-
		PU0	1	2	4	1	2	2
	I2C1SCL	PD4	101	94	71	68	-	-
		PU1	2	3	5	2	3	3
TSPI ch0	TSPI0RXD	PA2	27	20	20	17	15	10
		PC3	73	66	52	49	42	34
	TSPI0TXD	PA3	28	21	21	18	16	11
		PC4	74	67	53	50	43	-
	TSPI0SCK	PA4	29	22	22	19	17	12
		PC5	75	68	54	51	44	-
	TSPI0CSIN	PA0	25	18	18	15	13	-
		PC7	77	70	56	53	-	-
	TSPI0CS0	PC2	72	65	51	48	41	33
	TSPI0CS1	PA1	26	19	19	16	14	-
		PC6	76	69	55	52	-	-
TSPI ch1	TSPI1RXD	PG4	107	100	77	74	58	46
		PV1	13	14	16	13	-	-
	TSPI1TXD	PG5	108	101	78	75	59	47
		PV2	14	15	-	-	-	-
	TSPI1SCK	PG6	109	102	79	76	60	48
		PV3	15	16	-	-	-	-
	TSPI1CSIN	PG3	106	99	76	73	57	45
		PV0	12	13	15	12	-	-
	TSPI1CS0	PG2	105	98	75	72	56	44
		PP6	32	25	-	-	-	-
	TSPI1CS1	PG1	104	97	74	71	55	-
		PP7	33	26	-	-	-	-
CAN	CANRX	PE1	111	104	81	78	-	-
	CANTX	PE0	110	103	80	77	-	-

Not Recommended for New Design

Table 4.7 Signal connection List (3/8)

Function	Combination functional pin name	Port name	M4KQ (LQFP144)	M4KP (LQFP128)	M4KN (QFP100)	M4KN (LQFP100)	M4KM (LQFP80)	M4KL (LQFP64)
T32A ch0	T32A00INA0	PA2	27	20	20	17	15	10
		PT0	86	79	-	-	-	-
	T32A00INA1	PT2	88	81	-	-	-	-
	T32A00OUTA	PA3	28	21	21	18	16	11
		PT1	87	80	-	-	-	-
	T32A00INB0	PA0	25	18	18	15	13	-
		PT3	89	82	-	-	-	-
	T32A00INB1	PA1	26	19	19	16	14	-
		PT4	90	83	-	-	-	-
	T32A00OUTB	PA4	29	22	22	19	17	12
		PT5	91	84	-	-	-	-
	T32A00INC0	PA2	27	20	20	17	15	10
		PT0	86	79	-	-	-	-
	T32A00INC1	PT2	88	81	-	-	-	-
	T32A00OUTC	PA3	28	21	21	18	16	11
		PT1	87	80	-	-	-	-
T32A ch1	T32A01INA0	PF3	141	126	100	97	79	-
		PP3	120	113	-	-	-	-
	T32A01INA1	PF5	139	124	98	95	-	-
		PP5	31	24	-	-	-	-
	T32A01OUTA	PF4	140	125	99	96	78	-
		PP4	30	23	-	-	-	-
	T32A01INB0	PF6	138	123	97	94	77	-
		PR5	126	-	-	-	-	-
	T32A01INB1	PF7	137	122	96	93	76	-
		PR6	127	-	-	-	-	-
	T32A01OUTB	PR7	128	-	-	-	-	-
		PV0	12	13	15	12	-	-
	T32A01INC0	PF3	141	126	100	97	79	-
		PP3	120	113	-	-	-	-
	T32A01INC1	PF5	139	124	98	95	-	-
		PP5	31	24	-	-	-	-
	T32A01OUTC	PF4	140	125	99	96	78	-
		PP4	30	23	-	-	-	-
T32A ch2	T32A02INA0	PC0	70	63	49	46	39	31
		PU1	2	3	5	2	3	3
	T32A02INA1	PC6	76	69	55	52	-	-
		PU5	6	7	9	6	7	7
	T32A02OUTA	PC1	71	64	50	47	40	32
		PU2	3	4	6	3	4	4
	T32A02INB0	PC7	77	70	56	53	-	-
		PU3	4	5	7	4	5	5
	T32A02INB1	PD0	97	90	67	64	-	-
		PU0	1	2	4	1	2	2
	T32A02OUTB	PD1	98	91	68	65	-	-
		PU4	5	6	8	5	6	6
	T32A02INC0	PC0	70	63	49	46	39	31
		PU1	2	3	5	2	3	3
	T32A02INC1	PC6	76	69	55	52	-	-
		PU4	5	6	8	5	6	6
	T32A02OUTC	PC1	71	64	50	47	40	32
		PU2	3	4	6	3	4	4

Not Recommended for New Design

Table 4.8 Signal connection List (4/8)

Function	Combination functional pin name	Port name	M4KQ (LQFP144)	M4KP (LQFP128)	M4KN (QFP100)	M4KN (LQFP100)	M4KM (LQFP80)	M4KL (LQFP64)
T32A ch3	T32A03INA0	PD2	99	92	69	66	-	-
		PE1	111	104	81	78	62	50
	T32A03INA1	PD3	100	93	70	67	-	-
		PE3	113	106	83	80	64	52
	T32A03OUTA	PC2	72	65	51	48	41	33
		PE2	112	105	82	79	63	51
	T32A03INB0	PD4	101	94	71	68	-	-
		PE4	114	107	84	81	65	53
	T32A03INB1	PD5	102	95	72	69	-	-
		PE5	115	108	85	82	66	54
	T32A03OUTB	PC3	73	66	52	49	42	34
		PE6	116	109	86	83	67	55
	T32A03INC0	PD2	99	92	69	66	-	-
		PE1	111	104	81	78	62	50
	T32A03INC1	PD3	100	93	70	67	-	-
		PE3	113	106	83	80	64	52
	T32A03OUTC	PC2	72	65	51	48	41	33
		PE2	112	105	82	79	63	51
T32A ch4	T32A04INA0	PG0	103	96	73	70	54	-
		PW0	16	-	-	-	-	-
	T32A04INA1	PG1	104	97	74	71	55	-
		PW2	18	-	-	-	-	-
	T32A04OUTA	PG2	105	98	75	72	56	44
		PW1	17	-	-	-	-	-
	T32A04INB0	PG4	107	100	77	74	58	46
		PW3	19	-	-	-	-	-
	T32A04INB1	PG5	108	101	78	75	59	47
		PW4	20	-	-	-	-	-
	T32A04OUTB	PG3	106	99	76	73	57	45
		PW5	21	-	-	-	-	-
	T32A04INC0	PG0	103	96	73	70	54	-
		PW0	16	-	-	-	-	-
	T32A04INC1	PG1	104	97	74	71	55	-
		PW2	18	-	-	-	-	-
	T32A04OUTC	PG2	105	98	75	72	56	44
		PW1	17	-	-	-	-	-
T32A ch5	T32A05INA0	PF0	144	1	3	100	1	1
		PN0	9	10	12	9	9	-
	T32A05INA1	PF2	142	127	1	98	-	-
		PN2	11	12	14	11	11	-
	T32A05OUTA	PF1	143	128	2	99	80	64
		PN1	10	11	13	10	10	-
	T32A05INB0	PP0	96	89	-	-	-	-
		PR0	121	-	-	-	-	-
	T32A05INB1	PP1	118	111	-	-	-	-
		PR1	122	-	-	-	-	-
	T32A05OUTB	PP2	119	112	-	-	-	-
		PR2	123	-	-	-	-	-
	T32A05INC0	PF0	144	1	3	100	1	1
		PN0	9	10	12	9	9	-
	T32A05INC1	PF2	142	127	1	98	-	-
		PN2	11	12	14	11	11	-
	T32A05OUTC	PF1	143	128	2	99	80	64
		PN1	10	11	13	10	10	-

Not Recommended for New Design

Table 4.9 Signal connection List (5/8)

Function	Combination functional pin name	Port name	M4KQ (LQFP144)	M4KP (LQFP128)	M4KN (QFP100)	M4KN (LQFP100)	M4KM (LQFP80)	M4KL (LQFP64)
ADC unit A	AINA00	PM7	49	42	-	-	-	-
	AINA01	PM6	48	41	-	-	-	-
	AINA02	PM5	47	40	-	-	-	-
	AINA03	PM4	46	39	-	-	-	-
	AINA04	PM3	45	38	-	-	-	-
	AINA05	PM2	44	37	33	30	-	-
	AINA06	PM1	43	36	32	29	-	-
	AINA07	PM0	42	35	31	28	-	-
	AINA08	PL7	41	34	30	27	25	20
	AINA09	PL6	40	33	29	26	24	19
	AINA13	PL5	39	32	28	25	23	18
	AINA14	PL3	37	30	26	23	21	16
	AINA15	PL1	35	28	24	21	19	14
	AINA16	PL0	34	27	23	20	18	13
	AINA17	PL2	36	29	25	22	20	15
	AINA18	PL4	38	31	27	24	22	17
ADC unit B	AINB00	PK0	61	54	42	39	34	27
	AINB01	PK1	60	53	41	38	33	26
	AINB02	PK2	59	52	40	37	32	25
	AINB03	PK3	58	51	39	36	31	-
	AINB04	PK4	57	50	38	35	30	-
	AINB05	PK5	56	49	-	-	-	-
	AINB06	PK6	55	48	-	-	-	-
	AINB07	PK7	54	47	-	-	-	-
ADC unit C	AINC00	PJ0	69	62	48	45	38	30
	AINC01	PJ1	68	61	47	44	37	29
	AINC02	PJ2	67	60	46	43	36	28
	AINC03	PJ3	66	59	45	42	35	-
	AINC04	PJ4	65	58	44	41	-	-
	AINC05	PJ5	64	57	43	40	-	-
	AINC06	PJ6	63	56	-	-	-	-
	AINC07	PJ7	62	55	-	-	-	-

Not Recommended for New Design

Table 4.10 Signal connection List (6/8)

Function	Combination functional pin name	Port name	M4KQ (LQFP144)	M4KP (LQFP128)	M4KN (QFP100)	M4KN (LQFP100)	M4KM (LQFP80)	M4KL (LQFP64)
IA/IB	INT00	PA2	27	20	20	17	15	10
	INT01b	PA3	28	21	21	18	16	11
	INT01a	PA4	29	22	22	19	17	12
	INT02a	PC1	71	64	50	47	40	32
	INT02b	PC6	76	69	55	52	-	-
	INT03a	PC3	73	66	52	49	42	34
	INT03b	PD2	99	92	69	66	-	-
	INT04b	PE1	111	104	81	78	62	50
	INT04a	PE3	113	106	83	80	64	52
	INT05a	PE5	115	108	85	82	66	54
	INT05b	PE6	116	109	86	83	67	55
	INT06a	PF1	143	128	2	99	80	64
	INT06b	PF2	142	127	1	98	-	-
	INT07a	PU1	2	3	5	2	3	3
	INT07b	PU2	3	4	6	3	4	4
	INT08a	PU3	4	5	7	4	5	5
	INT08b	PU4	5	6	8	5	6	6
	INT09	PU6	7	8	10	7	8	8
	INT10	PC2	72	65	51	48	41	33
	INT11a	PE4	114	107	84	81	65	53
	INT11b	PE5	115	108	85	82	66	54
	INT12	PU0	1	2	4	1	2	2
	INT13	PU5	6	7	9	6	7	7
	INT14a	PF4	140	125	99	96	78	-
	INT14b	PF5	139	124	98	95	-	-
	INT15	PA1	26	19	19	16	14	-
	INT16a	PN1	10	11	13	10	10	-
	INT16b	PN2	11	12	14	11	11	-
	INT17b	PD0	97	90	67	64	-	-
	INT17a	PD1	98	91	68	65	-	-
	INT18b	PD4	101	94	71	68	-	-
	INT18a	PD5	102	95	72	69	-	-
	INT19a	PP1	118	111	-	-	-	-
	INT19b	PP2	119	112	-	-	-	-
	INT20b	PW3	19	-	-	-	-	-
	INT20a	PW4	20	-	-	-	-	-
	INT21	PG3	106	99	76	73	57	45

Not Recommended for New Design

Table 4.11 Signal connection List (7/8)

Function	Combination functional pin name	Port name	M4KQ (LQFP144)	M4KP (LQFP128)	M4KN (QFP100)	M4KN (LQFP100)	M4KM (LQFP80)	M4KL (LQFP64)
A-PMD ch0	EMG0	PB6	84	77	63	60	51	41
	OVV0	PB7	85	78	64	61	-	-
	UO0	PB0	78	71	57	54	45	35
	VO0	PB2	80	73	59	56	47	37
	WO0	PB4	82	75	61	58	49	39
	XO0	PB1	79	72	58	55	46	36
	YO0	PB3	81	74	60	57	48	38
	ZO0	PB5	83	76	62	59	50	40
	PMD0DBG	PB7	85	78	64	61	-	-
		PC2	72	65	51	48	41	33
A-PMD ch1	EMG1	PE6	116	109	86	83	67	55
	OVV1	PE7	117	110	87	84	-	-
	UO1	PE0	110	103	80	77	61	49
	VO1	PE2	112	105	82	79	63	51
	WO1	PE4	114	107	84	81	65	53
	XO1	PE1	111	104	81	78	62	50
	YO1	PE3	113	106	83	80	64	52
	ZO1	PE5	115	108	85	82	66	54
	PMD1DBG	PC3	73	66	52	49	42	34
		PE7	117	110	87	84	-	-
A-PMD ch2	EMG2	PU6	7	8	10	7	8	8
	OVV2	PU7	8	9	11	8	-	-
	UO2	PU0	1	2	4	1	2	2
	VO2	PU2	3	4	6	3	4	4
	WO2	PU4	5	6	8	5	6	6
	XO2	PU1	2	3	5	2	3	3
	YO2	PU3	4	5	7	4	5	5
	ZO2	PU5	6	7	9	6	7	7
	PMD2DBG	PA2	27	20	20	17	15	10
		PU7	8	9	11	8	-	-
A-ENC32 ch0	ENC0A	PN0	9	10	12	9	9	-
		PP3	120	113	-	-	-	-
	ENC0B	PN1	10	11	13	10	10	-
		PP4	30	23	-	-	-	-
	ENC0Z	PN2	11	12	14	11	11	-
		PP5	31	24	-	-	-	-
A-ENC32 ch1	ENC1A	PF3	141	126	100	97	79	-
		PR3	124	-	-	-	-	-
	ENC1B	PF4	140	125	99	96	78	-
		PR4	125	-	-	-	-	-
	ENC1Z	PF5	139	124	98	95	-	-
		PR5	126	-	-	-	-	-
A-ENC32 ch2	ENC2A	PD3	100	93	70	67	-	-
		PU3	4	5	7	4	5	5
	ENC2B	PD4	101	94	71	68	-	-
		PU5	6	7	9	6	7	7
	ENC2Z	PD5	102	95	72	69	-	-
		PU6	7	8	10	7	8	8

Not Recommended for New Design

Table 4.12 Signal connection List (8/8)

Function	Combination functional pin name	Port name	M4KQ (LQFP144)	M4KP (LQFP128)	M4KN (QFP100)	M4KN (LQFP100)	M4KM (LQFP80)	M4KL (LQFP64)
TRGSEL	TRGIN0	PA2	27	20	20	17	15	10
	TRGIN1	PA3	28	21	21	18	16	11
	TRGIN2	PA4	29	22	22	19	17	12
JTAG	TMS	PF0	144	1	3	100	-	-
	TCK	PF1	143	128	2	99	-	-
	TDO	PF2	142	127	1	98	-	-
	TDI	PF3	141	126	100	97	-	-
	TRST_N	PF4	140	125	99	96	-	-
SW	SWDIO	PF0	144	1	3	100	1	1
	SWCLK	PF1	143	128	2	99	80	64
	SWV	PF2	142	127	1	98	-	-
TRACE	TRACECLK	PF5	139	124	98	95	-	-
	TRACEDATA0	PF6	138	123	97	94	-	-
	TRACEDATA1	PF7	137	122	96	93	-	-
	TRACEDATA2	PN0	9	10	12	9	-	-
	TRACEDATA3	PN1	10	11	13	10	-	-
NBDIF	NBDSYNC	PF4	140	125	99	96	-	-
	NBDCLK	PF5	139	124	98	95	-	-
	NBDDATA0	PF6	138	123	97	94	-	-
	NBDDATA1	PF7	137	122	96	93	-	-
	NBDDATA2	PN0	9	10	12	9	-	-
	NBDDATA3	PN1	10	11	13	10	-	-
Control pin	X1	PH0	134	119	93	90	73	61
	X2	PH1	135	120	94	91	74	62
	EHCLKIN	PH0	134	119	93	90	73	61
	BOOT_N	PG2	105	98	75	72	56	44
	RESET_N		136	121	95	92	75	63
	MODE		133	118	92	89	72	60

Not Recommended for New Design

4.3. Ports

The symbols of each table of the port have the following meanings.

- Input/Output: Input or/and Output of Port
  Input: Input port
  Output: Output port
  I/O: Input/Output port

- PU/PD: Programmable pull-up/pull-down
  PU: Programmable pull-up is selectable
  PD: Programmable pull-down is selectable

- OD: Programmable open-drain output
  Yes: Support
  No: Non support

- 5V_T: 5V-tolerant
  Yes: Support
  N/A: Not available

- SMT/CMOS: Input gate
  SMT: Schmitt trigger input
  CMOS: CMOS input

- State under Reset: Port state under Reset
  Hi-z: High impedance
  PU: Pull-up
  PD: Pull-down

- State after Reset: Port state after Reset
  Hi-z: High impedance
  PU: Pull-up
  PD: Pull-down

Not Recommended for New Design

4.3.1. Port Specification Table

Table 4.13 Pin numbers, and specifications of Port A, B, C, D

Port Name	Input/Output	PU/PD	OD	5V_T	SMT/ CMOS	Under Reset	After Reset
PA0	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PA1	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PA2	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PA3	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PA4	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PB0	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PB1	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PB2	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PB3	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PB4	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PB5	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PB6	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PB7	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PC0	I/O	PU/PD	YES	YES	SMT	Hi-z	Hi-z
PC1	I/O	PU/PD	YES	YES	SMT	Hi-z	Hi-z
PC2	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PC3	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PC4	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PC5	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PC6	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PC7	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PD0	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PD1	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PD2	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PD3	I/O	PU/PD	YES	YES	SMT	Hi-z	Hi-z
PD4	I/O	PU/PD	YES	YES	SMT	Hi-z	Hi-z
PD5	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z

Not Recommended for New Design

Table 4.14 Pin numbers, and specifications of Port E, F, G, H

Port Name	Input/Output	PU/PD	OD	5V_T	SMT/ CMOS	Under Reset	After Reset
PE0	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PE1	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PE2	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PE3	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PE4	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PE5	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PE6	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PE7	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PF0	I/O	PU/PD	YES	N/A	SMT	PU(Note2)	PU(Note2)
PF1	I/O	PU/PD	YES	N/A	SMT	PD(Note2)	PD(Note2)
PF2	I/O	PU/PD	YES	N/A	SMT	Hi-z (Note2)	Hi-z (Note2)
PF3	I/O	PU/PD	YES	N/A	SMT	PU(Note2)	PU(Note2)
PF4	I/O	PU/PD	YES	N/A	SMT	PU(Note2)	PU(Note2)
PF5	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PF6	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PF7	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PG0	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PG1	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PG2	Output	PU/PD (Note1)	YES	N/A	SMT	Hi-z (Note1)	Hi-z
PG3	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PG4	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PG5	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PG6	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PH0	Input	PD	NO	N/A	SMT	Hi-z	Hi-z
PH1	Input	PD	NO	N/A	SMT	Hi-z	Hi-z

Note1: Combination with BOOT_N. When RESET_N=0, Pull-up resistor is enabled.
When RESET_N=1, the pin state is Hi-z with internal reset.

Note2: It is assigned to a debugging pin in the state of the initial stage. (PF3: TDI, PF2: TDO/SWV, PF0: TMS/SWDIO, PF1: TCK/SWCLK, PF4: TRST_N)
When receiving the command from TOOL, PF2: TDO/SWV becomes output.

Not Recommended for New Design

Table 4.15 Pin numbers, and specifications of Port J, K, L

Port Name	Input/Output	PU/PD	OD	5V_T	SMT/ CMOS	Under Reset	After Reset
PJ0	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PJ1	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PJ2	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PJ3	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PJ4	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PJ5	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PJ6	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PJ7	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PK0	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PK1	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PK2	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PK3	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PK4	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PK5	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PK6	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PK7	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PL0	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PL1	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PL2	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PL3	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PL4	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PL5	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PL6	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PL7	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z

Not Recommended for New Design

Table 4.16 Pin numbers, and specifications of Port M, N, P, R

Port Name	Input/Output	PU/PD	OD	5V_T	SMT/ CMOS	Under Reset	After Reset
PM0	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PM1	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PM2	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PM3	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PM4	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PM5	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PM6	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PM7	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PN0	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PN1	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PN2	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PP0	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PP1	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PP2	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PP3	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PP4	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PP5	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PP6	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PP7	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PR0	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PR1	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PR2	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PR3	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PR4	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PR5	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PR6	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PR7	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z

Not Recommended for New Design

Table 4.17 Pin numbers, and specifications of Port T, U, V, W

Port Name	Input/Output	PU/PD	OD	5V_T	SMT/ CMOS	Under Reset	After Reset
PT0	I/O	PU/PD	YES	YES	SMT	Hi-z	Hi-z
PT1	I/O	PU/PD	YES	YES	SMT	Hi-z	Hi-z
PT2	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PT3	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PT4	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PT5	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PT6	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PT7	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PU0	I/O	PU/PD	YES	YES	SMT	Hi-z	Hi-z
PU1	I/O	PU/PD	YES	YES	SMT	Hi-z	Hi-z
PU2	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PU3	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PU4	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PU5	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PU6	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PU7	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PV0	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PV1	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PV2	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PV3	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PW0	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PW1	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PW2	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PW3	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PW4	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PW5	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PW6	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PW7	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z

Not Recommended for New Design

5. Functional Description and Operation Description

5.1. Reference Manuals

For more information on product of TMPM4K Group(2), please refer to Reference Manuals below;

Table 5.1 Reference Manuals for TMPM4K Group(2)

Reference Manual	IP Symbol	Category
Input/Output Ports (TMPM4K Group(2))	PORT-M4K(2)	System
Memory Map (TMPM4K Group(2))	MMAP-M4K(2)	System
Exception (TMPM4K Group(2))	EXCEPT-M4K(2)	System
Clock Control and Operation Mode (TMPM4K Group(2))	CG-M4K(2)-E	System
Product Information (TMPM4K Group(2))	PINFO-M4K(2)	System
Power supply and Reset operation (TMPM4K Group(2))	RESET-M4K(2)	System
Flash Memory	FLASH512HD32-B	Peripheral
Trimming Circuit	TRM-A	Peripheral
Oscillation Frequency Detector	OFD-A	Peripheral
Voltage Detection Circuit	LVD-B	Peripheral
Digital Noise Filter Circuit	DNF-A	Peripheral
Debug Interface	DEBUG-A	Peripheral
Non Break Debug Interface	NBDIF-A	Peripheral
DMA Controller	DMAC-B	Peripheral
Asynchronous Serial Communication Circuit	UART-C	Peripheral
Serial Peripheral Interface	TSPI-B	Peripheral
I^2C Interface	I2C-B	Peripheral
CAN Controller	CAN-A	Peripheral
12-bit Analog to Digital Converter	ADC-D	Peripheral
Operational Amplifier	OPAMP-A	Peripheral
Advanced Programmable Motor Control Circuit	A-PMD-A	Peripheral
Advanced Encoder Input Circuit (32-bit)	A-ENC32-A	Peripheral
Advanced Vector Engine Plus	A-VE+-B	Peripheral
32-bit Timer Event Counter	T32A-B	Peripheral
Clock Selective Watchdog Timer	SIWDT-A	Peripheral
CRC Calculation Circuit	CRC-A	Peripheral
RAM Parity	RAMP-B	Peripheral

Not Recommended for New Design

5.2. Processor Core

The TMPM4K Group(2) incorporates a high-performance 32-bit processor core (Arm Cortex-M4 processor with FPU).

For the operation of the processor core, refer to the Arm documentation set for "Cortex-M series processors". This section explains the product-specific information.

5.2.1. Core Information

The Cortex-M4 processor with FPU revision used in the TMPM4K Group(2) is shown as below:

For details of the CPU core and the architecture, refer to the documentation of the Arm in the following URL:

http://infocenter.arm.com/help/index.jsp

Table 5.2 Core revision

Group name	Core revision
TMPM4K Group(2)	r0p1

5.2.2. Configurable Options

In the Cortex-M4 processor with FPU, some blocks can be selected to implement. The following table shows the configurations of the TMPM4K Group(2).

Table 5.3 Configurable options and their implementations

Configurable option	Implementation
FWB	Literal comparator: 2 Instruction comparator: 6
DWT	Comparator: 4
ITM	Available
MPU	Available
ETM	Available
AHB-AP	Available
AHB trace macro cell interface	Not available
TPIU	Available
WIC	Not available
Debug port	JTAG/Serial wire
Bit band	Available
Sequential control of AHB	Not available

Not Recommended for New Design

5.3. Clock Control and Operation Mode (CG)

The CG selects a clock gear ratio and the prescaler clock, or warm up time of the oscillator.

There are NORMAL mode and low-power consumption mode as operation modes. Power consumption can be decreased by mode transition.

The system clock consists of "High speed system clock" and "Middle speed system clock". The former is a high speed oscillation clock and the latter is generated by dividing High speed system clock.

The outline of the clock/mode control circuit is as follows:

- Internal high speed oscillator: 10MHz
- Selectable from the external high speed oscillator or internal high speed oscillator.
- PLL (Clock Multiplication Circuit)

  For System clock, Capable of 160 MHz output by changing the multiplication ratio according to the frequency of the high speed oscillation circuit.
- Clock gear:

  The high speed clock can be divided by 1/1, 1/2, 1/4, 1/8, or 1/16 and the clock is used as the system clock (fsys).
- Low-power consumption mode:

  IDLE: Only the CPU is stopped in this mode. Each peripheral circuit can enable or disable operation in the IDLE mode.

  STOP1: The system clock is stopped in this mode.

5.4. Flash Memory (Code FLASH, Data FLASH)

TMPM4K Group(2) has 512KB/256KB/128KB of Code flash and 32KB of Data flash.

The code flash stores instruction code, and CPU reads instruction code and executes. The data flash stores data, and even if a power supply is off, data can be kept.

It has the dual mode that possible to write and erase data flash while executing an order by a code flash. And it's also possible to continue executing an application program during writing or erasing data flash memory.

It has protection function which prohibits write or erase by the block unit and it has the security function which prohibits the reading of the program code by the 3rd person.

Not Recommended for New Design

5.5. Oscillator

External High Speed Oscillator (EHOSC):

Connect crystal resonator or ceramic resonator to terminals. Use clock source for System clock.

Internal High Speed Oscillator 1 (IHOSC1):

The oscillation frequency is 10MHz. Use clock source for System clock.

Internal High Speed Oscillator 2 (IHOSC2):

The oscillation frequency is 10MHz. Use clock source for OFD and SIWDT.

Table 5.4 Built-in Oscillator

	M4KQ	M4KP	M4KN	M4KM	M4KL
EHOSC	✓	✓	✓	✓	✓
IHOSC1	✓	✓	✓	✓	✓
IHOSC2	✓	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.6. Trimming Circuit (TRM)

The TRM can adjust oscillation frequency of the internal high speed oscillator (IHOSC1).

Table 5.5 Built-in TRM

	M4KQ	M4KP	M4KN	M4KM	M4KL
TRM	✓	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.7. Oscillation Frequency Detection Circuit (OFD)

The OFD is a function that detects an abnormal state of the clock. It measures the external high speed oscillation (f_{EHOSC}) or high speed clock (fc) based on the internal reference clock (f_{IHOSC2}). If an oscillation or clock frequency is out of the specified range, a reset signal occurs.

The upper limit and the lower limit of detection frequency ranges can be specified respectively.

Table 5.6 Built-in OFD

	M4KQ	M4KP	M4KN	M4KM	M4KL
OFD	✓	✓	✓	✓	✓

Note: ✓: Available, -: N/A

Not Recommended for New Design

5.8. Voltage Detection Circuit (LVD)

The LVD is a peripheral function that detects whether a power supply voltage is lower or higher than the preset voltage. When a low voltage or higher voltage than the preset voltage is detected, the LVD generates an interrupt request or reset the MCU.

Setting voltage can be chosen from eight kinds. LVD is set to enable from the Reset state at the Power on.

Table 5.7 Built-in LVD

	M4KQ	M4KP	M4KN	M4KM	M4KL
LVD	✓	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.9. Digital Noise Filter circuit(DNF)

The DNF can eliminate the noise of input signals from external interrupt pins at the certain range. The noise of the High level / Low level input of the external interrupt signal INTx is removed.

Table 5.8 Number of External Interrupt (Built-in DNF)

	M4KQ	M4KP	M4KN	M4KM	M4KL
Number of External Interrupt	22	21	20	18	15

Not Recommended for New Design

5.10. Debug Interface (DEBUG)

TMPM4K Group(2) contain Interface for connecting debug tool, which is the Serial Wire Debug Port (SWCLK, SWDIO) and the JTAG Debug Port (TDI, TDO, TMS, TCK, TRST_N). These are connected with the Debug tool and used for program development. And also it contains the trace clock(TRACECLK) and data output (TRACEDATA0to3) to reduce the Debug Process.

TMPM4K Group(2) products support serial wire debug ports, JTAG debug ports, trace outputs, and NBDIF.

Table 5.9 Built-in Debug Interface

Debug function	Pin Name	PORT	M4KQ	M4KP	M4KN	M4KM	M4KL
SW	SWDIO	PF0	✓	✓	✓	✓	✓
	SWCLK	PF1	✓	✓	✓	✓	✓
	SWV	PF2	✓	✓	✓	-	-
JTAG	TMS	PF0	✓	✓	✓	-	-
	TCK	PF1	✓	✓	✓	-	-
	TDO	PF2	✓	✓	✓	-	-
	TDI	PF3	✓	✓	✓	-	-
	TRST_N	PF4	✓	✓	✓	-	-
TRACE	TRACECLK	PF5	✓	✓	✓	-	-
	TRACEDATA0	PF6	✓	✓	✓	-	-
	TRACEDATA1	PF7	✓	✓	✓	-	-
	TRACEDATA2	PN0	✓	✓	✓	-	-
	TRACEDATA3	PN1	✓	✓	✓	-	-
NBDIF	NBDSYNC	PF4	✓	✓	✓	-	-
	NBDCLK	PF5	✓	✓	✓	-	-
	NBDDATA0	PF6	✓	✓	✓	-	-
	NBDDATA1	PF7	✓	✓	✓	-	-
	NBDDATA2	PN0	✓	✓	✓	-	-
	NBDDATA3	PN1	✓	✓	✓	-	-

Note: ✓: Available, -: N/A

5.10.1. Non Break Debug Interface (NBDIF)

Connecting debug tools supporting NBDIF can provide RAM monitor function.
NBDIF support vary depending on the product. Please refer to "Table 5.9 Built-in Debug Interface".

Not Recommended for New Design

5.11. DMA Controller (DMAC)

The DMAC is the peripheral function to move the data between peripheral functions and the memory, or between memories. These operations are performed separately from the CPU control; thus, the CPU load can greatly be reduced by using the DMA.

TMPM4K Group(2) product has one DMA controller (DMAC) unit, and there are up to 32 channels of activation factors per unit.

Table 5.10 Built-in DMAC

DMAC	M4KQ	M4KP	M4KN	M4KM	M4KL
Unit A	✓	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.12. Asynchronous Serial Communication Circuit (UART)

The UART is asynchronous serial communication function. It can choose the data length of 7, 8 or 9bits, parity existence, and a STOP bit length function. Moreover, selection of the MSB first / LSB first and reversal of data polarity can be performed and Terminal exchanged of TXD/RXD can be performed in a Port setting.

The FIFO buffer supports data communication on 8-stage at transmission; and on 8-stage at reception. The telecommunication control by CTS/RTS is supported.

Table 5.11 Built-in UART

Channel	M4KQ	M4KP	M4KN	M4KM	M4KL
Channel 0	✓	✓	✓	✓	✓
Channel 1	✓	✓	✓	✓	✓
Channel 2	✓	✓	✓	✓	✓
Channel 3	✓	✓	✓	✓	-

Note1: ✓: Available, -: N/A

Note2: External pins vary depending on the product. Please refer to section "2. Pin Assignment".

Not Recommended for New Design

5.13. Serial Peripheral Interface (TSPI)

The TSPI supports two communication methods and enables to perform serial communication between other devices at high speed. The SPI bus type, which uses a CS (Chip Select) signal at communications, and SIO bus type, which does not use a CS signal at communications can be selected.

The data length can be changed from 7 bits (with a parity bit) to 32 bits (without a parity bit) in the unit of one bit. There is an 8-stage 16-bit FIFO for reception and transmission, each. The TSPI supports the master and slave communications.

Table 5.12 Built-in TSPI

Channel	M4KQ	M4KP	M4KN	M4KM	M4KL
Channel 0	✓	✓	✓	✓	✓
Channel 1	✓	✓	✓	✓	✓

Note1: ✓: Available, -: N/A

Note2: External pins vary depending on the product. Please refer to section "2. Pin Assignment".

5.14. I^2C Interface (I^2C)

I^2C is two-wire bi-directional serial communications between Master and Slave device. The mode in which two or more masters can exist on the same bus called a multi-master is supported. It supports Standard mode (Max 100kbps), Fast mode (Max 400kbps).

Table 5.13 Built-in I^2C

Channel	M4KQ	M4KP	M4KN	M4KM	M4KL
Channel 0	✓	✓	✓	✓	✓
Channel 1	✓	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.15. CAN controller (CAN)

The CAN is a system that can mutually communicate without a host computer. It conforms to CAN version 2.0 B active and supports the standard and extended format. It has 32 mailbox and maximum transfer rate is 1Mbps.

Table 5.14 Built-in CAN

Channel	M4KQ	M4KP	M4KN	M4KM	M4KL
Channel 0	✓	✓	✓	-	-

Note1: ✓: Available, -: N/A

Note2: External pins vary depending on the product. Please refer to section "2. Pin Assignment".

Not Recommended for New Design

5.16. 12-bit Analog to Digital Converter (ADC)

The ADC is a 12-bit successive-approximation analog-to-digital converter. The combination of a conversion result register and analog input can be programmed in each startup trigger of AD conversion. A startup trigger for analog to digital conversion can be selected from software or peripheral functions (A-PMD trigger outputs, timer/event counter outputs, port inputs). A motor is easily controllable by cooperating especially with A-PMD.

The monitor function of conversion result is also available and it can generate an interrupt when the compare conditions are matched.

This ADC incorporates a selector to connect VREFH/VREFL with reference power supply. Controlling by software can support self-diagnosis function.

Table 5.15 Built-in ADC channel list

ADC	M4KQ	M4KP	M4KN	M4KM	M4KL
Unit A Analog Inputs Pin count	16	16	11	8	8
Unit B Analog Inputs Pin count	8	8	5	5	3
Unit C Analog Inputs Pin count	8	8	6	4	3

5.17. Operational Amplifier (OPAMP)

This MCU incorporates an OPAMP to amplify weak analog signals inputting to the ADC. The input gain is selectable.

Table 5.16 Built-in OPAMP

Unit	M4KQ	M4KP	M4KN	M4KM	M4KL
Unit A	✓	✓	✓	✓	✓
Unit B	✓	✓	✓	✓	✓
Unit C	✓	✓	✓	✓	✓

Note: ✓: Available, -: N/A

Not Recommended for New Design

5.18. Advanced Programmable Motor Control Circuit (A-PMD)

The A-PMD enables users to control brushless DC motors easily. It incorporates the pulse modulation circuit and dead-time circuit, and easily generates signals for motor control that makes 3-phase complementary PWM output and ADC cooperate.

It also provides the over-voltage detection input and abnormal detection input to support safety measures.

Furthermore, 3-phase interleaved PFC control for power-factor improvement can be provided.

Table 5.17 Built-in A-PMD

Channel	M4KQ	M4KP	M4KN	M4KM	M4KL
Channel 0	✓	✓	✓	✓	✓
Channel 1	✓	✓	✓	✓	✓
Channel 2	✓	✓	✓	✓	✓

Note1: ✓: Available, -: N/A

5.19. Advanced Encoder Input Circuit (32-bit) (A-ENC32)

The A-ENC32 supports an incremental encoder to acquire the motor position easily. The noise canceller is installed in the input pins, so that the signals from an incremental encoder or Hall sensor can be input directly.

The A-ENC32 provides six operation modes: encoder mode, sensor modes (3 kinds), timer mode, and phase counter mode.

Table 5.18 Built-in A-ENC

Channel	M4KQ	M4KP	M4KN	M4KM	M4KL
Channel 0	✓	✓	✓	✓	-
Channel 1	✓	✓	✓	-	-
Channel 2	✓	✓	✓	✓	✓

Note1: ✓: Available, -: N/A

Note2: External pins vary depending on the product. Please refer to section "2. Pin Assignment".

Not Recommended for New Design

5.20. Advanced Vector Engine Plus (A-VE+)

The advanced vector engine plus executes vector control by hardware. In this vector operation, the ADC and A-PMD operate in a coordinated fashion without software involvement.

Also, it provides 1-shunt current detection area enlargement process, dead time compensation control, and non-interfere control.

Table 5.19 Built-in A-VE+

Channel	M4KQ	M4KP	M4KN	M4KM	M4KL
Channel 0	✓	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.21. 32-bit Timer Event Counter (T32A)

The T32A is a timer event counter that can operate as a 32-bit timer or two 16-bit timers. 16-bit Timer or 32-bit Timer can be selected. In 16-bit Timer, the T32A is comprised of Timer A and Timer B incorporating a 16-bit counter respectively. In 32-bit Timer, the T32A operates as Timer C incorporating a 32-bit counter.

The T32A have an interval timer, event counter, input capture, 2-phase counter input, PPG output, Synchronous Start, and Trigger start/stop functions.

Table 5.20 Built-in T32A

Channel	M4KQ	M4KP	M4KN	M4KM	M4KL
Channel 0	✓	✓	✓	✓	✓
Channel 1	✓	✓	✓	✓	✓
Channel 2	✓	✓	✓	✓	✓
Channel 3	✓	✓	✓	✓	✓
Channel 4	✓	✓	✓	✓	✓
Channel 5	✓	✓	✓	✓	✓

Note1: ✓: Available, -: N/A

Note2: External pins vary depending on the product. Please refer to section "2. Pin Assignment".

Not Recommended for New Design

5.22. Clock Selective Watchdog Timer (SIWDT)

The SIWDT is a peripheral function that detects an overflow of the binary counter and generates an interrupt request or resets the MCU. This state occurs when a binary counter cannot be cleared within the preset detection time.

The count clock can be selected from three clocks: system clock (fsys/4), internal oscillator (f_{IHOSC1}), or internal oscillator2 (f_{IHOSC2}).

It also provides the count-clear window function that can clear the count only for the specified period.

Moreover, change of a register can be forbidden by setting to protected mode.(the count-clear function is possible)

Table 5.21 Built-in SIWDT

Channel	M4KQ	M4KP	M4KN	M4KM	M4KL
Channel 0	✓	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.23. CRC Calculation Circuit (CRC)

The CRC Calculation Circuit has the hardware calculation circuit for CRC32 and CRC16.

It can be used for detecting a memory and communication data error.

Table 5.22 Built-in CRC

	M4KQ	M4KP	M4KN	M4KM	M4KL
CRC	✓	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.24. RAM Parity (RAMP)

The RAM parity function generates and (8-bit unit) stores even parity data when writing to RAM, and performs a parity judging when reading from RAM.

An interrupt is generated when it becomes an error by judgment. The Status and Address which the error generated are known.

Table 5.23 Built-in RAMP

Channel	M4KQ	M4KP	M4KN	M4KM	M4KL
Channel 0	✓	✓	✓	✓	✓
Channel 1	✓	✓	✓	✓	✓

Note: ✓: Available, -: N/A

Not Recommended for New Design

6. Equivalent Circuit

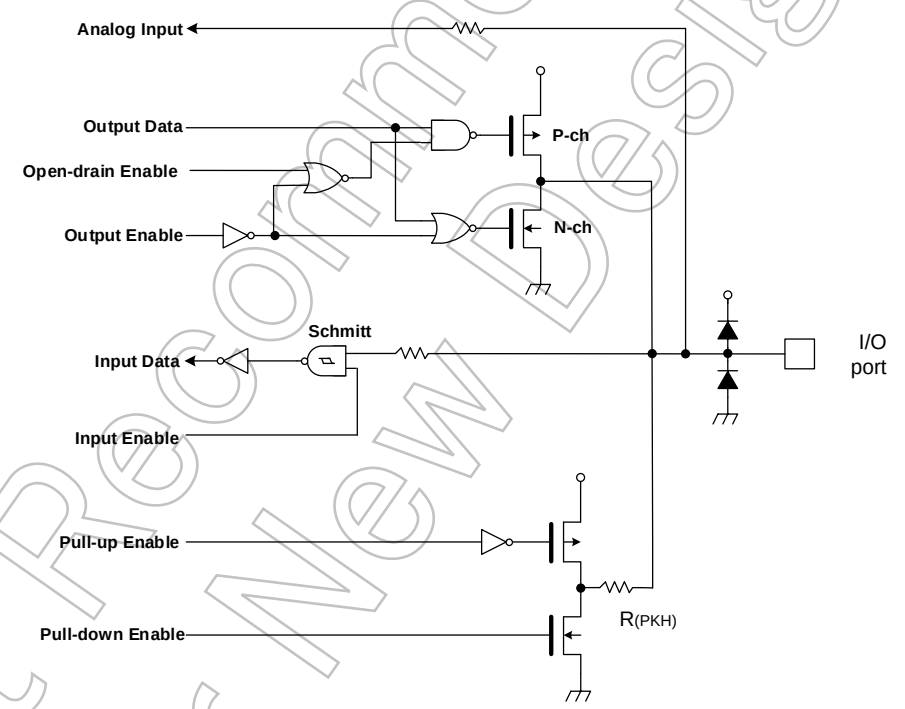
Basically, the gate symbols written are the same as those used for the standard CMOS logic IC [74HCxx] series.

The input protection resistance ranges from several tens of Ω to several hundred Ω. Feedback resistor and Damping resistor are shown with a typical value.

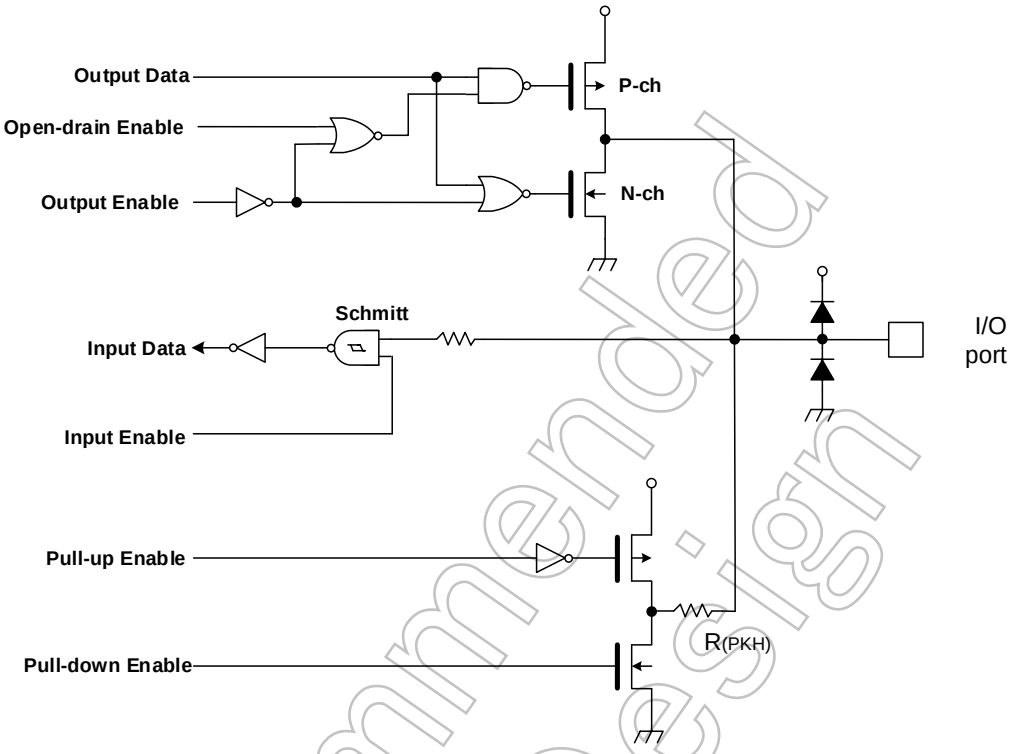
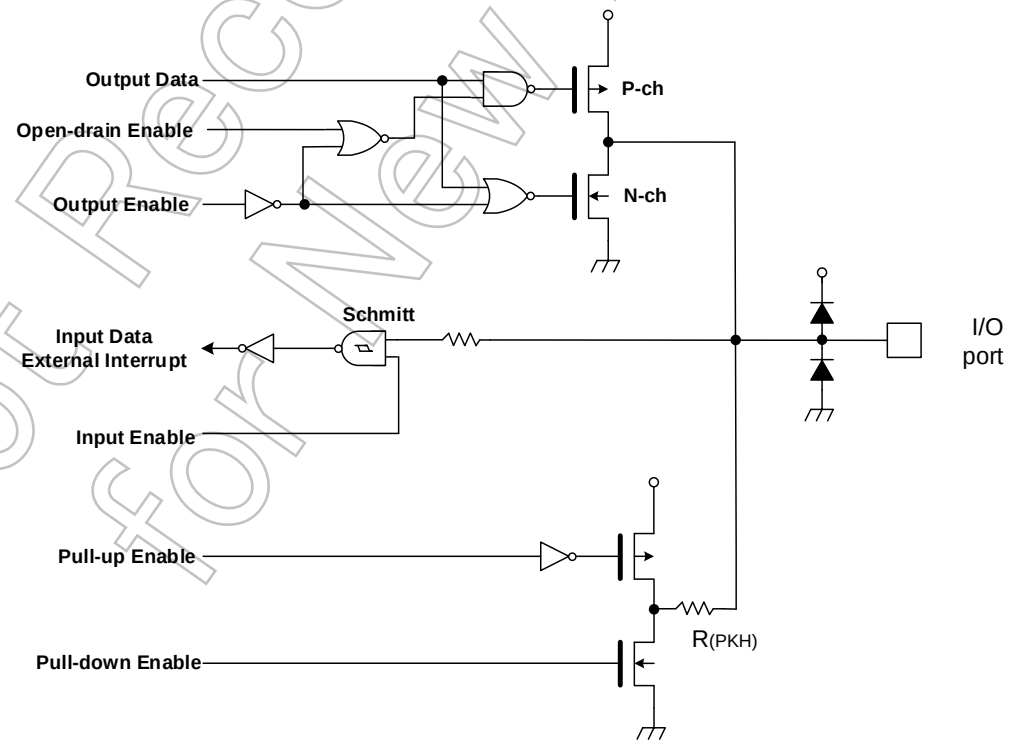
Note: The resistance without the statement of the numerical value in the figure shows input protection resistance.

6.1. Port

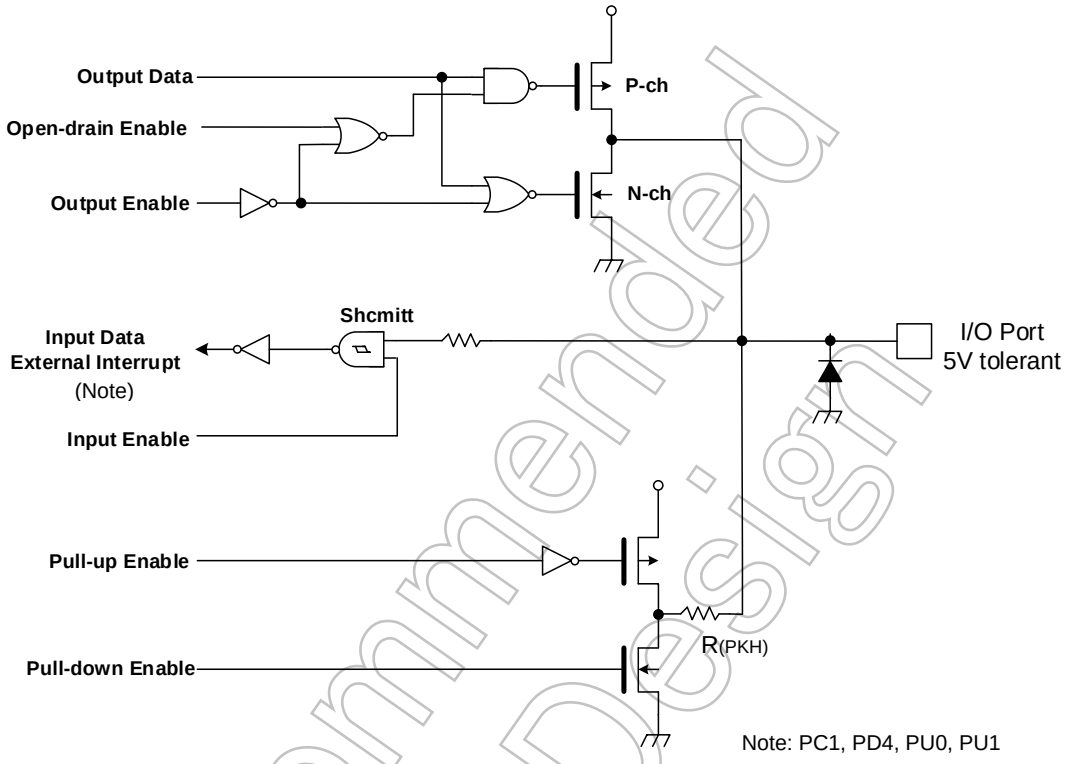
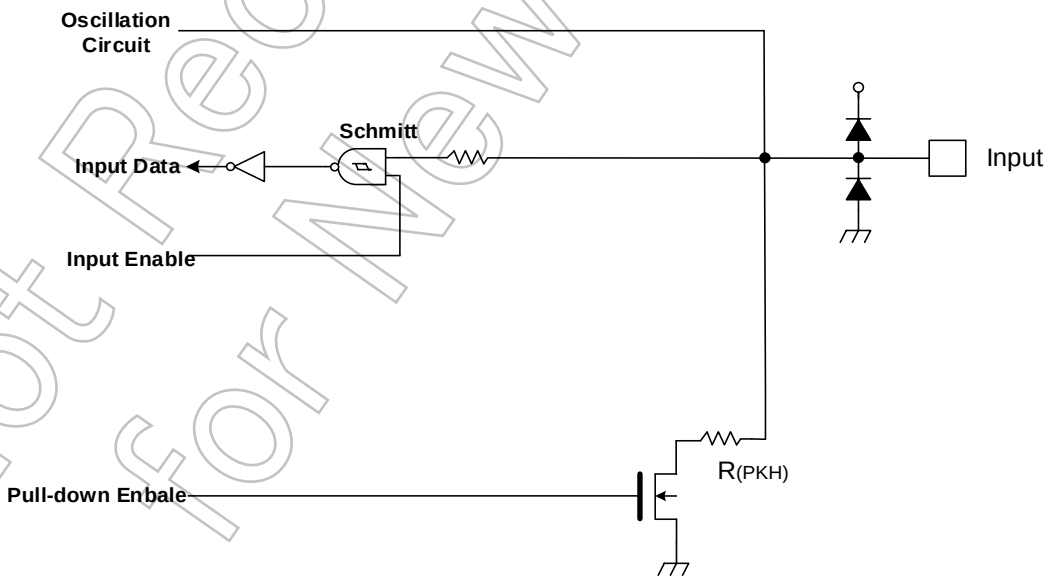
PJ0 to PJ7, PK0 to PK7, PL0 to PL7, PM0 to PM7	**(Programmable pull-up/pull-down, Programmable Open-drain output, Schmitt input, Analog input)**



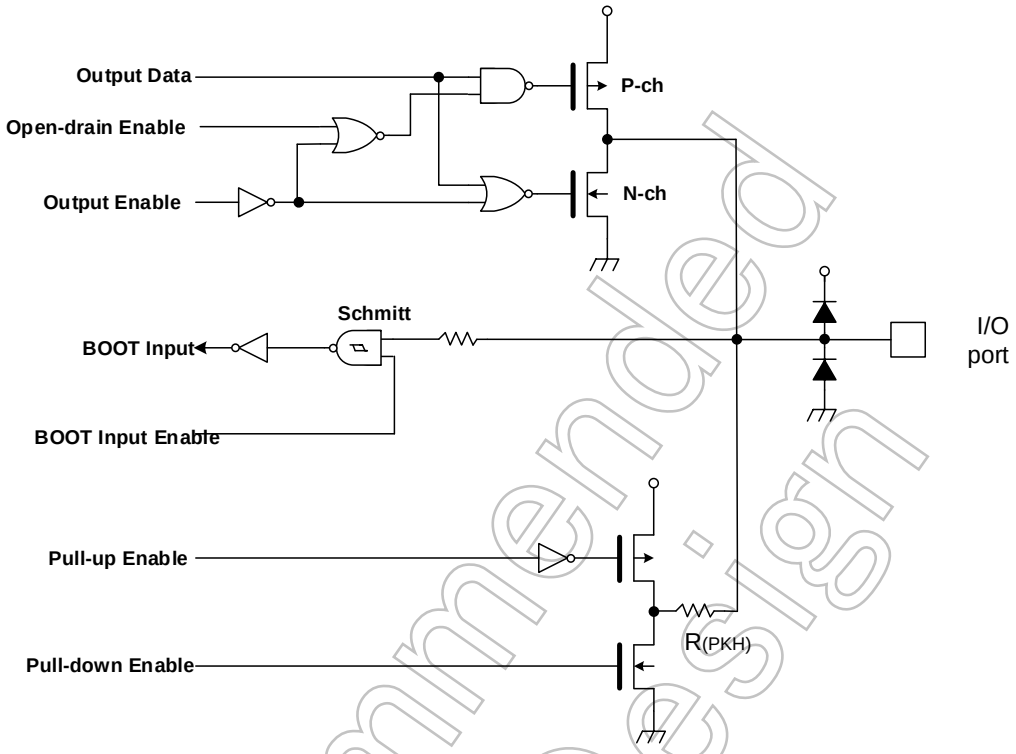
Not Recommended for New Design

PA0, PB0 to PB7 PC4, PC5, PC7, PE0, PE2, PE7, PF0, PF3, PF6, PF7, PG0, PG1, PG4 to PG6, PN0, PP0, PP3 to PP7, PR0 to PR7, PT2 to PT7, PU7, PV0 to PV3, PW0 to PW2, PW5 to PW7	(Programmable Pull-up/Pull-down, Programmable Open-drain Output, Schmitt Input) 
PA1 to PA4, PC2, PC3, PC6, PD0 to PD2, PD5, PE1, PE3 to PE6, PF1, PF2, PF4, PF5, PG3, PN1, PN2, PP1, PP2, PU2 to PU6, PW3, PW4	(Programmable Pull-up/Pull-down, Programmable Open-drain Output, Schmitt Input, External Interrupt Input) 

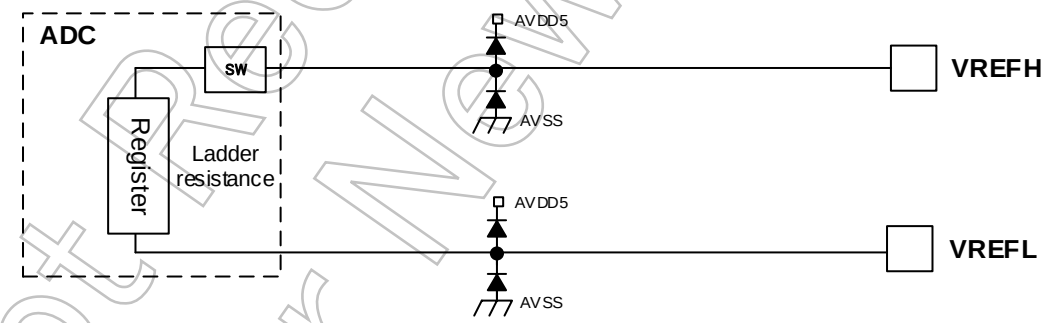
Not Recommended for New Design

PC0, PC1, PT0, PT1, PD3, PD4, PU0, PU1	**(5V tolerant, Programmable pull-up/pull-down, Programmable Open-drain output, Schmitt Input, External Interrupt Input)**  Note: PC1, PD4, PU0, PU1
PH0, PH1	**(Programmable Pull-down, Schmitt Input, Oscillation Circuit)** 

Not Recommended for New Design

PG2/BOOT_N	(Programmable Pull-up/Pull-down, Programmable Open-drain Output, Schmitt Input) 

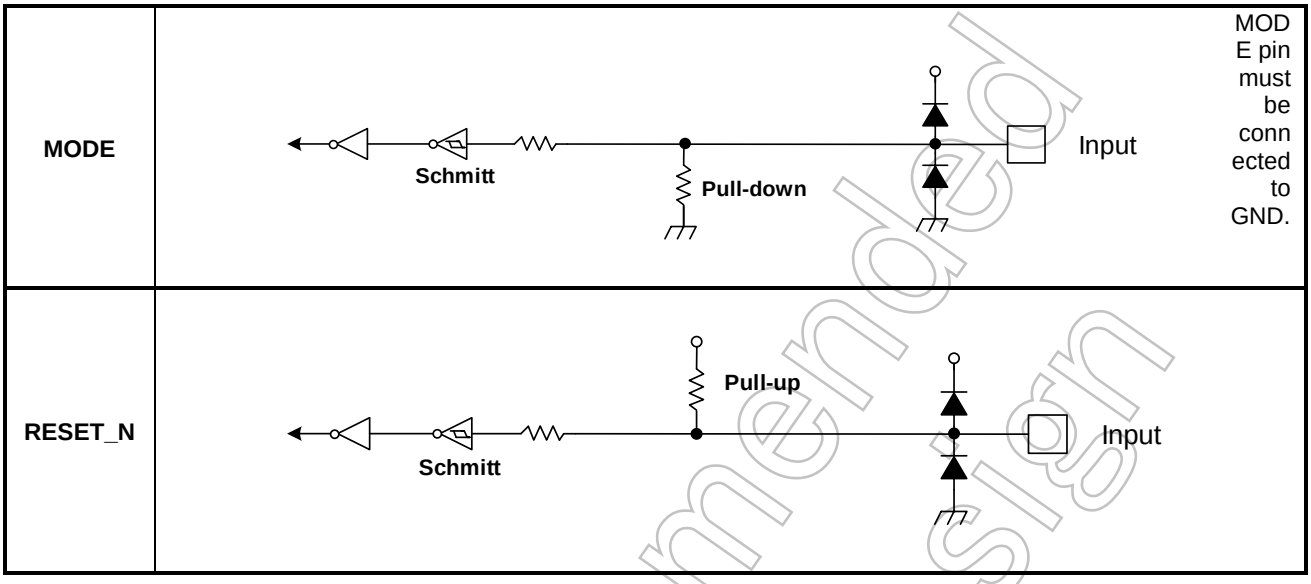
6.2. Analog Reference pin

VREFH VREFL	

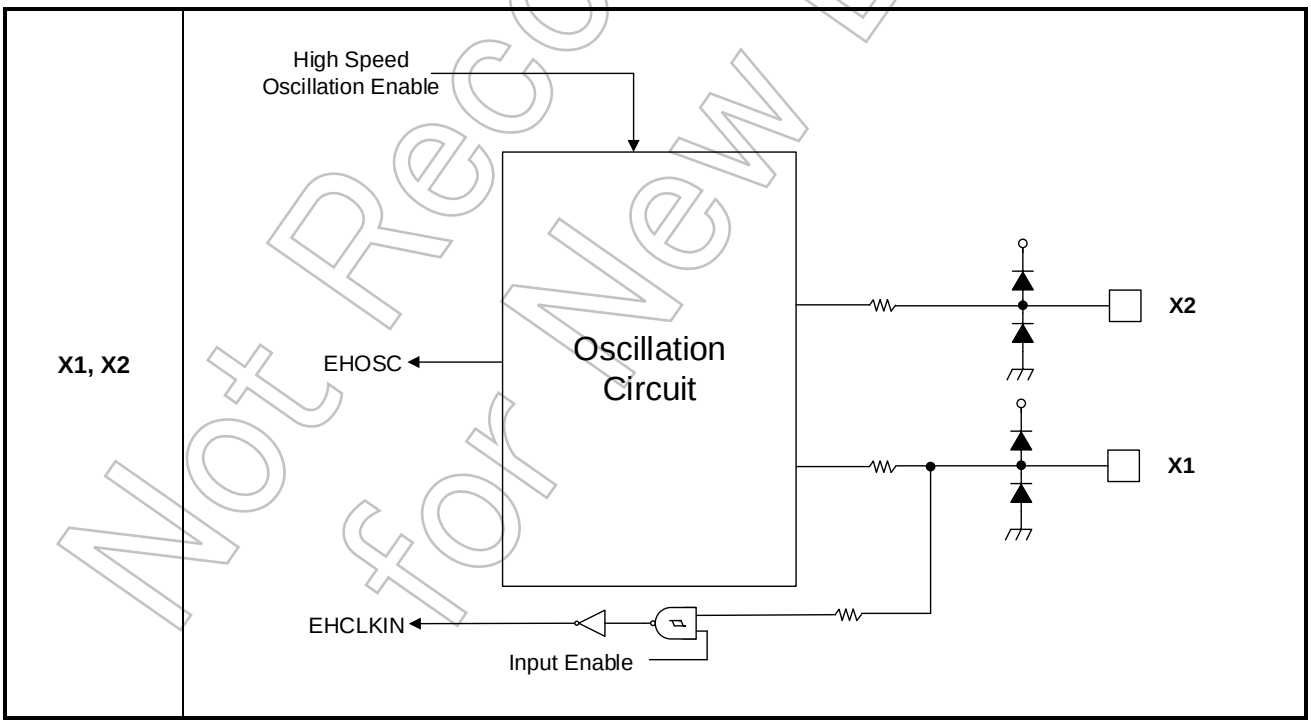
Note: SW: ON/OFF Switch Circuit

Not Recommended for New Design

6.3. Control Pin



6.4. Clock control



Not Recommended for New Design

7. Electrical Characteristics

7.1. Absolute Maximum Ratings

Table 7.1 Absolute maximum ratings

Parameter		Symbol	Rating	Unit
Power supply voltage		DVDD5A DVDD5B	-0.3 to 6.0	V
		AVDD5	-0.3 to 6.0 (Note2)	
Capacitor pin voltage for voltage maintenance		REGOUT1	-0.3 to 1.7	V
		REGOUT2	-0.3 to 3.9	
Input voltage	PA0 to PA4, PB0 to PB7, PC2 to PC7, PD0 to PD2, PD5, PE0 to PE7, PF0 to PF7, PG0, PG1, PG3 to PG6, PH0, PH1, PN0 to PN2, PP0 to PP7, PR0 to PR7, PT2 to PT7, PU2 to PU7, PV0 to PV3, PW0 to PW7, MODE, RESET_N, BOOT_N	V_{IN1} V_{IN2}	-0.3 to DVDD5+0.3(≤6.0V) (Note2)	V
	PJ0 to PJ7, PK0 to PK7, PL0 to PL7, PM0 toPM7	V_{IN3}	-0.3 to AVDD5+0.3(≤6.0V)	
	PC0, PC1, PD3, PD4, PT0, PT1, PU0, PU1	V_{IN4}	-0.3 to 6.0	
Low level output current	Per pin PA0 to PA4, PB0 to PB7, PC2 to PC7, PD0 to PD2, PD5, PE0 to PE7, PF0 to PF7, PG0 to PG6, PH0, PH1, PJ0 to PJ7, PK0 to PK7, PL0 to PL7, PM0 to PM7, PN0 to PN2, PP0 to PP7, PR0 to PR7, PT2 to PT7, PU2 to PU7, PV0 to PV3, PW0 to PW7	I_{OL}	5	mA
	Per pin PC0, PC1, PD3, PD4, PT0, PT1, PU0, PU1	I_{OL4}	25	
	Total of all pins	$\sum I_{OL}$	50	
High level output current	Per pin PA0 to PA4, PB0 to PB7, PC0 to PC7, PD0 to PD5, PE0 to PE7, PF0 to PF7, PG0 to PG6, PH0, PH1, PJ0 to PJ7, PK0 to PK7, PL0 to PL7, PM0 to PM7, PN0 to PN2, PP0 to PP7, PR0 to PR7, PT0 to PT7, PU0 to PU7, PV0 to PV3, PW0 to PW7	I_{OH}	-5	
	Total of all pins	$\sum I_{OH}$	-50	
Power consumption		PD	(Note3)	mW
Soldering temperature		T_{SOLDER}	260	°C
Storage temperature		T_{STG}	-55 to 125	°C
Operational temperature		T_{OPR}	-40 to 105(Note3)	°C
		Tj	-40 to 125	

Not Recommended for New Design

Note1: Absolute maximum ratings are limiting values of operating and environmental conditions which should not be exceeded under the worst possible conditions. The equipment manufacturer should design so that no Absolute maximum rating value is exceeded with respect to current, voltage, power consumption, temperature, etc. Exposure to conditions beyond those listed above may cause permanent damage to the device or affect device reliability, which could increase potential risks of personal injury due to IC blow up and/or burning.

Note2: DVDD5 is a generic name for DVDD5A, DVDD5B. Apply the same voltage to DVDD5 and AVDD5

Note3: The power consumption and the maximum temperature of the ambient temperature (T_{OPR}) should be used within the range not exceeding the junction temperature (Tj). The calculation formula for operating temperature (T_{OPR} (Ta)) is shown below.

$T_{OPR}(Max) = Tj(Max) - PD(Max) \times \theta ja$

PD: Power consumption (mW) → Maximum allowable power (PD(Max)) (mW)

θja: Thermal resistance of the package (°C/W)

Please refer to Table 7.2.

The calculation formula for maximum allowable power (PD(Max)) is shown below.

$PD(Max) = V_{DD} \times I_{DD}(Max) + \sum(I_{OL} \times V_{OL}) + \sum((V_{DD} - V_{OH}) \times |I_{OH}|)$

I_{OL}: "Low" level output current

I_{OH}: "High" level output current

V_{OL}: "Low" level output voltage

V_{OH}: "High" level output voltage

$I_{DD}(Max)$: Consumption current of the MCU excluding I/O.

Please refer to "7.3. DC Electrical Characteristics (2/2)".

Table 7.2 Thermal resistance of IC package and maximum allowable power table

Package	Substrate	Thermal resistance θja (°C/W)	Maximum allowable power (PD(Max)) (mW)	
			T_{OPR}=+85°C	T_{OPR}=+105°C
P-LQFP144-2020-0.50-002	2 layer board	52	768	384
	4 layer board	47	849	425
P-LQFP128-1420-0.50-001	2 layer board	48	833	417
	4 layer board	43	935	467
P-LQFP100-1414-0.50-002	2 layer board	56	714	357
	4 layer board	50	806	403
P-LQFP80-1414-0.65-001	2 layer board	56	714	357
	4 layer board	49	810	405
P-LQFP80-1212-0.50-003	2 layer board	61	661	331
	4 layer board	53	759	380
P-LQFP64-1010-0.50-003	2 layer board	59	677	338
	4 layer board	50	808	404
P-QFP100-1420-0.65-001	2 layer board	43	941	471
	4 layer board	40	1013	506
P-LQFP64-1212-0.65-001	2 layer board	61	661	331
	4 layer board	53	759	380

Not Recommended for New Design

7.2. DC Electrical Characteristics (1/2)

4.5V ≤ DVDD5=AVDD5 ≤ 5.5V
DVSS = AVSS=0V
Ta=-40 to 105 °C

Parameter		Symbol	Conditions	Min	Typ.	Max	Unit
Power supply voltage	DVDD5A, DVDD5B, AVDD5	VDD	fosc = 6 to 12MHz fsys = 1 to 160MHz fsysm=1 to 80MHz	4.5	-	5.5	V
Low level Input voltage	PA0 to PA4, PB0 to PB7, PC2 to PC7, PD0 to PD2, PD5, PE0 to PE7, PF0 toPF7, PG0, PG1, PG3 to PG6, PH0, PH1, PN0 to PN2, PP0 to PP7, PR0 to PR7, PT2 to PT7, PU2 to PU7, PV0 to PV3, PW0 to PW7, MODE, RESET_N, BOOT_N	V_{IL1} V_{IL2}	-	-0.3	-	DVDD5×0.25	V
	PJ0 to PJ7, PK0 to PK7, PL0 to PL7, PM0 to PM7	V_{IL3}	-			AVDD5×0.25	
	PC0, PC1, PD3, PD4, PT0, PT1, PU0, PU1	V_{IL4}	-			DVDD5×0.3	
High level Input voltage	PA0 to PA4, PB0 to PB7, PC2 to PC7, PD0 to PD2, PD5, PE0 to PE7, PF0 to PF7, PG0, PG1, PG3 to PG6, PH0, PH1, PN0 to PN2, PP0 to PP7, PR0 to PR7, PT2 to PT7, PU2 to PU7, PV0 to PV3, PW0 to PW7, MODE, RESET_N, BOOT_N	V_{IH1} V_{IH2}	-	DVDD5×0.75	-	DVDD5+0.3	V
	PJ0 to PJ7, PK0 to PK7, PL0 to PL7, PM0 to PM7	V_{IH3}	-	AVDD5×0.75		AVDD5+0.3	
	PC0, PC1, PD3, PD4, PT0, PT1, PU0, PU1	V_{IH4}	-	DVDD5×0.7		DVDD5+0.3	
Low level output voltage	PA0 to PA4, PB0 to PB7, PC2 to PC7, PD0 to PD2, PD5, PE0 to PE7, PF0 to PF7, PG0 to PG6, PN0 to PN2, PP0 to PP7, PR0 to PR7, PT2 to PT7, PU2 to PU7, PV0 to PV3, PW0 to PW7	V_{OL1} V_{OL2}	DVDD5=4.5V I_{OL}=1.6mA	-	-	0.4	V
	PJ0 to PJ7, PK0 to PK7, PL0 to PL7, PM0 to PM7	V_{OL3}	AVDD5=4.5V I_{OL}=1.6mA	-	-	0.4	
	PC0, PC1, PD3, PD4, PT0, PT1, PU0, PU1	V_{OL4}	DVDD5=4.5V I_{OL}=8mA	-	-	1.0	
High level output voltage	PA0 to PA4, PB0 to PB7, PC0 to PC7, PD0 to PD5, PE0 to PE7, PF0 to PF7, PG0 to PG6, PN0 to PN2, PP0 to PP7, PR0 to PR7, PT0 to PT7, PU0 to PU7, PV0 to PV3, PW0 to PW7	V_{OH1} V_{OH2}	DVDD5=4.5V I_{OH} = -1.6mA	DVDD5-0.4	-	-	V
	PJ0 to PJ7, PK0 to PK7, PL0 to PL7, PM0 to PM7	V_{OH3}	AVDD5=4.5V I_{OH} = -1.6mA	AVDD5-0.4	-	-	

Note1: DVDD5 is a generic name for DVDD5A and DVDD5B. DVSS is a generic name for DVSSA, DVSSB and DVSSC.

Note2: Typ. value is in Ta = 25 °C, DVDD5 = AVDD5 = 5.0V, unless otherwise noted.

Note3: Apply same voltage line to DVDD5 and AVDD5.

Not Recommended for New Design

4.5V ≤ DVDD5=AVDD5 ≤ 5.5V
DVSS=AVSS=0V
Ta= -40 to 105°C

Parameter		Symbol	Conditions	Min	Typ.	Max	Unit
Input leak current		I_{LI}	0.0V ≤ VIN ≤ DVDD5 0.0V ≤ VIN ≤ AVDD5	-5	±0.05	5	μA
Output leak current		I_{LO}	0.2 ≤ VIN ≤DVDD5-0.2 0.2 ≤ VIN ≤AVDD5-0.2	-10	±0.05	10	
Schmitt trigger Input width		V_{TH}	DVDD5=AVDD5=5V	-	1.0	-	V
Reset pull-up resistor		R_{RST}	-	25	30	100	kΩ
Programmable pull-up/pull-down resistor		P_{KH}	Pull-up	25	30	100	
			Pull-down	25	50	100	
Pin capacity (except power supply pin)		C_{IO}	fc =1MHz	-	-	10	pF
Low level output current	Per pin (except the following	I_{OL}	DVDD5=AVDD5=5V	-	-	2 (Note4)	mA
	Per pin PC0, PC1, PD3, PD4, PT0, PT1, PU0, PU1	I_{OL4}	DVDD5=5V	-		12 (Note4)	
	Total of PC0 to PC7, PB0 to PB7, PT0 to PT7, PP0, PD0 to PD5, PG0 to PG6, PE0 to PE7	$\sum I_{OL1}$	DVDD5=5V	-	-	35 (Note5)	
	Total of PP1 to PP7, PR0 to PR7, PF0 to PF7, PU0 to PU7, PN0 to PN2, PV0 to PV3, PW0 to PW7, PA0 to PA4	$\sum I_{OL2}$	DVDD5=5V	-	-	35 (Note5)	
	Total of PJ0 to PJ7, PK0 to PK7, PL0 to PL7, PM0 to PM7	$\sum I_{OL3}$	AVDD5=5V	-	-	35 (Note5)	
High level output current	Per pin	I_{OH}	DVDD5=AVDD5=5V	-2 (Note4)	-	-	mA
	Total of PC0 to PC7, PB0 to PB7, PT0 to PT7, PP0, PD0 to PD5, PG0 to PG6, PE0 to PE7	$\sum I_{OH1}$	DVDD5=5V	-35 (Note5)	-	-	
	Total of PP1 to PP7, PR0 to PR7, PF0 to PF7, PU0 to PU7, PN0 to PN2, PV0 to PV3, PW0 to PW7, PA0 to PA4	$\sum I_{OH2}$	DVDD5=5V	-35 (Note5)	-	-	
	Total of PJ0 to PJ7, PK0 to PK7, PL0 to PL7, PM0 to PM7	$\sum I_{OH3}$	AVDD5=5V	-35 (Note5)	-	-	

Note1: DVDD5 is a generic name for DVDD5A and DVDD5B. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

Note2: Typ. value is in Ta = 25 °C, DVDD5 = AVDD5 = 5.0V, unless otherwise noted.

Note3: Apply same voltage line to DVDD5 and AVDD5.

Note4: The sum of the terminal currents in each group should not exceed the total current of each group.

Note5: The sum of each group current should not exceed the absolute maximum rating.

Not Recommended for New Design

2.7V ≤DVDD5=AVDD5< 4.5V
DVSS=AVSS=0V
Ta=-40 to 105 °C

Parameter		Symbol	Conditions	Min	Typ.	Max	Unit
Power supply voltage	DVDD5A, DVDD5B, AVDD5	VDD	fosc = 6 to 12MHz fsys = 1 to 160MHz fsysm=1 to 80MHz	2.7	-	4.5	V
Low level Input voltage	PA0 to PA4, PB0 to PB7, PC2 to PC7, PD0 to PD2, PD5, PE0 to PE7, PF0 toPF7, PG0, PG1, PG3 to PG6, PH0, PH1, PN0 to PN2, PP0 to PP7, PR0 to PR7, PT2 to PT7, PU2 to PU7, PV0 to PV3, PW0 to PW7, MODE, RESET_N, BOOT_N	V_{IL1} V_{IL2}	-	-0.3	-	DVDD5×0.25	V
	PJ0 to PJ7, PK0 to PK7, PL0 to PL7, PM0 to PM7	V_{IL3}	-			AVDD5×0.25	
	PC0, PC1, PD3, PD4, PT0, PT1, PU0, PU1	V_{IL4}	-			DVDD5×0.3	
High level Input voltage	PA0 to PA4, PB0 to PB7, PC2 to PC7, PD0 to PD2, PD5, PE0 to PE7, PF0 to PF7, PG0, PG1, PG3 to PG6, PH0, PH1, PN0 to PN2, PP0 to PP7, PR0 to PR7, PT2 to PT7, PU2 to PU7, PV0 to PV3, PW0 to PW7, MODE, RESET_N, BOOT_N	V_{IH1} V_{IH2}	-	DVDD5×0.75	-	DVDD5+0.3	V
	PJ0 to PJ7, PK0 to PK7, PL0 to PL7, PM0 to PM7	V_{IH3}	-	AVDD5×0.75		AVDD5+0.3	
	PC0, PC1, PD3, PD4, PT0, PT1, PU0, PU1	V_{IH4}	-	DVDD5×0.7		DVDD5+0.3	
Low level output voltage	PA0 to PA4, PB0 to PB7, PC2 to PC7, PD0 to PD2, PD5, PE0 to PE7, PF0 to PF7, PG0 to PG6, PN0 to PN2, PP0 to PP7, PR0 to PR7, PT2 to PT7, PU2 to PU7, PV0 to PV3, PW0 to PW7	V_{OL1} V_{OL2}	DVDD5=2.7V I_{OL}=0.8mA	-	-	0.4	V
	PJ0 to PJ7, PK0 to PK7, PL0 to PL7, PM0 to PM7	V_{OL3}	AVDD5=2.7V I_{OL}=0.8mA	-	-	0.4	
	PC0, PC1, PD3, PD4, PT0, PT1, PU0, PU1	V_{OL4}	DVDD5=2.7V I_{OL}=4mA	-	-	1.0	
High level output voltage	PA0 to PA4, PB0 to PB7, PC0 to PC7, PD0 to PD5, PE0 to PE7, PF0 to PF7, PG0 to PG6, PN0 to PN2, PP0 to PP7, PR0 to PR7, PT0 to PT7, PU0 to PU7, PV0 to PV3, PW0 to PW7	V_{OH1} V_{OH2}	DVDD5=2.7V I_{OH}= -0.8mA	DVDD5-0.4	-	-	V
	PJ0 to PJ7, PK0 to PK7, PL0 to PL7, PM0 to PM7	V_{OH3}	AVDD5=2.7V I_{OH}= -0.8mA	AVDD5-0.4	-	-	

Note1: DVDD5 is a generic name for DVDD5A and DVDD5B. DVSS is a generic name for DVSSA, DVSSB and DVSSC.

Note2: Typ. value is in Ta = 25 °C, DVDD5 = AVDD5 = 3.0V, unless otherwise noted.

Note3: Apply same voltage line to DVDD5 and AVDD5.

Not Recommended for New Design

2.7V ≤DVDD5=AVDD5< 4.5V
DVSS=AVSS=0V
Ta= -40 to 105°C

Parameter		Symbol	Conditions	Min	Typ.	Max	Unit
Input leak current		I_{LI}	0.0V ≤ VIN ≤ DVDD5 0.0V ≤ VIN ≤ AVDD5	-5	±0.05	5	μA
Output leak current		I_{LO}	0.2 ≤ VIN ≤DVDD5-0.2 0.2 ≤ VIN ≤AVDD5-0.2	-10	±0.05	10	
Schmitt trigger Input width		V_{TH}	DVDD5=AVDD5=3V	-	0.5	-	V
Reset pull-up resistor		R_{RST}	-	25	100	200	kΩ
Programmable pull-up/pull-down resistor		P_{KH}	Pull-up	25	100	200	
			Pull-down	25	100	200	
Pin capacity (except power supply pin)		C_{IO}	fc =1MHz	-	-	10	pF
Low level output current	Per pin (except the following	I_{OL}	DVDD5=AVDD5=3V	-	-	1 (Note4)	mA
	Per pin PC0, PC1, PD3, PD4, PT0, PT1, PU0, PU1	I_{OL4}	DVDD5=3V	-	-	6 (Note4)	
	Total of PC0 to PC7, PB0 to PB7, PT0 to PT7, PP0, PD0 to PD5, PG0 to PG6, PE0 to PE7	$\sum I_{OL1}$	DVDD5=3V	-	-	18 (Note5)	
	Total of PP1 to PP7, PR0 to PR7, PF0 to PF7, PU0 to PU7, PN0 to PN2, PV0 to PV3, PW0 to PW7, PA0 to PA4	$\sum I_{OL2}$	DVDD5=3V	-	-	18 (Note5)	
	Total of PJ0 to PJ7, PK0 to PK7, PL0 to PL7, PM0 to PM7	$\sum I_{OL3}$	AVDD5=3V	-	-	17 (Note5)	
High level output current	Per pin	I_{OH}	DVDD5=AVDD5=3V	-1 (Note4)	-	-	mA
	Total of PC0 to PC7, PB0 to PB7, PT0 to PT7, PP0, PD0 to PD5, PG0 to PG6, PE0 to PE7	$\sum I_{OH1}$	DVDD5=3V	-18 (Note5)	-	-	
	Total of PP1 to PP7, PR0 to PR7, PF0 to PF7, PU0 to PU7, PN0 to PN2, PV0 to PV3, PW0 to PW7, PA0 to PA4	$\sum I_{OH2}$	DVDD5=3V	-18 (Note5)	-	-	
	Total of PJ0 to PJ7, PK0 to PK7, PL0 to PL7, PM0 to PM7	$\sum I_{OH3}$	AVDD5=3V	-17 (Note5)	-	-	

Note1: DVDD5 is a generic name for DVDD5A and DVDD5B. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

Note2: Typ. value is in Ta = 25 °C, DVDD5 = AVDD5 = 3.0V, unless otherwise noted.

Note3: Apply same voltage line to DVDD5 and AVDD5.

Note4: The sum of the terminal currents in each group should not exceed the total current of each group.

Note5: The sum of each group current should not exceed the absolute maximum rating.

Not Recommended for New Design

7.3. DC Electrical Characteristics (2/2)

Ta= -40 to 105°C

Parameter	Symbol	Conditions			Min	Typ.	Max	Unit
		Supply voltage	High-speed oscillator	Operating condition				
NORMAL	I_{DD}	DVDD5= AVDD5= 5.5V	Refer to Table 7.3 and Table 7.4 for detail		-	45	72	mA
IDLE			Oscillation	Refer to Table 7.3 and Table 7.4 for detail	-	7	30	
STOP1			Stop		-	0.8	20	mA

Note1: DVDD5 is a generic name for DVDD5A and DVDD5B. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

Note2: Typ. value is in Ta = 25 °C, DVDD5 = AVDD5 = 5.0V, unless otherwise noted.

Note3: Apply same voltage to DVDD5 and AVDD5.

Note4: Input pin is fixed level, Output pin is open.

Table 7.3 I_{DD} measurement condition (Pin setting, Oscillation Circuit)

		NORMAL	IDLE	STOP1
Pin setting	DVDD5= AVDD5=	5.0V(Typ.), 5.5V(max)		
	X1, X2	Oscillator connected (10MHz)		
	Input pins	Fixed		
	Output pins	Open		
Operation condition (Oscillation Circuit)	System clock (fsys/fsysm)	160MHz/80MHz		Stop
	External High speed frequency oscillator (EHOSC)	Oscillation		Stop
	Internal High speed frequency oscillator (IHOSC1)	Stop		
	PLL	run (16 times)		Stop

Not Recommended for New Design

Table 7.4 I_{DD} measurement condition (CPU, Peripheral)

Peripheral	unit number	NORMAL	IDLE	STOP1
CPU	1	Run (DhrystoneVer.2.1)	Stop	
DMAC	1	(Request from UARTch0, ch2: TX source: RAM)	Stop	
ADC	3	Run (1.0µs, Repeated conversion)	Stop	
OPAMP	3	All ch: Run	Stop	
T32A	6	All ch: Run	Stop	
A-PMD	3	All ch: Run	Stop	
A-ENC32	3	Run	Stop	
A-VE+	1	Run	Stop	
SIWDT	1	Run	Stop	
UART	4	2ch's: Transmission(5Mbps)	Stop	
I^2C	2	Stop		
TSPI	2	2ch's: Transmission(10MHz)	Stop	
CAN	1	Stop		
CRC	1	Stop		
RAMP	2	Run	Stop	
LVD	1	Stop		
OFD	1	Run	Stop	
Debug	1	Stop		
NBDIF	1	Stop		
Input/Output Port	-	Run	Stop	

fsys=160MHz
Ta= -40 to 105°C

Item	Symbol	Condition	Min	Typ.	Max	Unit
Power consumption (ADC, OPAMP run)	I_{AVDD}	AVDD5=5.0V, AVSS=0V	-	18	22	mA

Not Recommended for New Design

7.4. 12-bit AD Converter Characteristics

DVDD5=AVDD5=4.5V to 5.5V
DVSS=AVSS=0V
Ta= -40 to 105°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Analog reference voltage (+)	VREFH	-	4.5	-	AVDD5	V
Analog input voltage	V_{AIN}	VREFL=AVSS	VREFL	-	VREFH	V
Integral nonlinear error (INL)	-	4.5V≤ AVDD5=VREFH ≤5.5V AVSS=VREFL=0V AIN load resistor = 600 Ω AIN load capacity ≥ 0.1μF Conversion time = 1.0μs	**-3**	-	**3**	LSB
Differential nonlinear error (DNL)			**-2**	-	**2**	
Zero-scale error			**-4**	-	**5**	
Full-scale error			**-5**	-	**4**	
Total errors			**-7**	-	**5**	
Stable time	t_{sta}	After set "1" to ***[ADxMOD0]***<DACON>.	3	-	-	μs
Conversion time	t_{conv}	4.5V ≤ AVDD5 ≤ 5.5V	1.0	-	-	

Note1: DVDD5 is a generic name for DVDD5A and DVDD5B. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

Note2: 1LSB = (VREFH - VREFL) / 4096 [V]

Note3: The characteristic when single AD converter operates.

Not Recommended for New Design

7.5. Operational Amplifier (OPAMP) Characteristics

DVDD5=AVDD5= 4.5V to 5.5V
DVSS=AVSS= 0V, Ta= -40 to 105°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Gain (factor) (Note2)	V_{GAIN}	-	2.0	-	15	×
Amp input voltage range (Common mode)	V_{AMPINP} V_{AMPINN}	VINP/VINN pin: AVSS−0.3 to AVDD5+0.3	AVSS-0.3	-	(AVDD5×0.99) /V_{GAIN}	V
Amp input voltage range (Differential)	V_{AMPINP} V_{AMPINN}	V_{GAIN}=2.0	0	-	AVDD5 /(MinV_{GAIN})	
Amp output voltage	V_{VOLT}	-	AVDD5×0.01	-	AVDD5×0.99	
Differential step offset voltage	V_{OFF}	-	-5	-	+5	mV
Gain error range	-	-	-3	-	+3	%
Through rate	Vthr	10pF	6	10	-	V/µs
AMPEN→Output stable time	Tsta1	Upper limit: +5mV Lower limit: -5mV C_L=10pF	-	-	2	µs

Note1: The characteristic when the amplifier unit operates only.

Note2: Gain can selected 2.5, 3, 3.5, 4, 4.5, 6, 7, 8, 10, and 12

Note3: DVDD5 is a generic name for DVDD5A and DVDD5B. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

Note4: Typ. value is in Ta = 25 °C, DVDD5 = AVDD5 = 5.0V, unless otherwise noted.

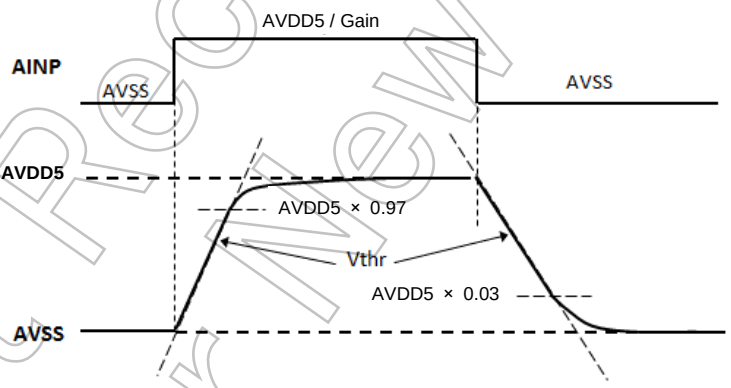


Figure 7.1 Through rate

Not Recommended for New Design

7.6. Characteristics of Internal processing at RESET

DVSSA=DVSSB=DVSSC=AVSS=0V
Ta= -40 to 105°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Internal Initialized time	t_{IINIT}	Power On	-	-	2.15	ms
Internal processing time for Reset	t_{IRST}	-	0.13	-	0.2	
Waiting time till CPU running	t_{CPUWT}	Cold Reset	12	-	15	µs
		Warm Reset	70	-	95	
Power-on rising gradient	V_{PON}	-	0.01	-	100	mV/µs

7.7. Characteristics of Power on Reset

DVSSA=DVSSB=DVSSC=AVSS=0V
Ta= -40 to 105°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Detection voltage	V_{PREL}	Power increases	2.25	2.4	2.55	V
	V_{PDET}	Power decreases	2.2	2.35	2.5	
Detection pulse width	T_{PDET}	-	200	-	-	µs

Not Recommended for New Design

7.8. Characteristics of Voltage Detection Circuit

DVDD5=AVDD5=2.7V to 5.5V
DVSS=AVSS=0V
Ta= -40 to 105°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Detection voltage	V_{LVL0}	Power increases	2.55	2.65	2.75	V
		Power decreases	2.5	2.6	2.7	
	V_{LVL1}	Power increases	2.65	2.75	2.85	V
		Power decreases	2.6	2.7	2.8	
	V_{LVL2}	Power increases	2.75	2.85	2.95	V
		Power decreases	2.7	2.8	2.9	
	V_{LVL3}	Power increases	2.85	2.95	3.05	V
		Power decreases	2.8	2.9	3.0	
	V_{LVL4}	Power increases	3.95	4.05	4.15	V
		Power decreases	3.9	4.0	4.1	
	V_{LVL5}	Power increases	4.15	4.25	4.35	V
		Power decreases	4.1	4.2	4.3	
	V_{LVL6}	Power increases	4.35	4.45	4.55	V
		Power decreases	4.3	4.4	4.5	
	V_{LVL7}	Power increases	4.55	4.65	4.75	V
		Power decreases	4.5	4.6	4.7	
Detection response time	t_{VDDT1}	Power decreases	-	50	200	µs
Detection Release time	t_{VDDT2}	Power increases	-	250	-	
Setup time	t_{LVDEN}	-	-	-	100	
Detection Minimum pulse width	t_{LVDPW}	-	200	-	-	

Note: DVDD5 is a generic name for DVDD5A and DVDD5B. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

Not Recommended for New Design

7.9. AC Electrical Characteristics

7.9.1. Serial Peripheral Interface (TSPI)

7.9.1.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5=AVDD5= 2.7 to 5.5 V
- Ta = -40 to 105°C
- Output level: High = 0.8 × DVDD5, Low = 0.2 × DVDD5
- Input level: High = 0.75 × DVDD5, Low = 0.25 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, and DVDD5B.

7.9.1.2. AC Electrical Characteristics

"T" indicates an operation clock cycle of the TSPI. This operation clock has the same cycle of the system clock (fsysm). This cycle depends on the clock gear setting.

The number of cycles can be 1 to 16. It is specified with TSPIxSCK. The value of "k1" is specified with ***[TSPIxFMTR0]***<CSSCKDL[3:0]>; the value of "k2" is specified with ***[TSPIxFMTR0]***<SCKCSDL[3:0]>. These values are 1 to 16.

Not Recommended for New Design

(1) Master in SPI mode

4.5V ≤DVDD5=AVDD5≤ 5.5V

Parameter	Symbol	Equation		fsysm=80MHz k1=k2=1		Unit
		Min	Max	Min	Max	
TSPIxSCK output frequency	f_{CYC}	-	10	-	10	MHz
TSPIxSCK output cycle	t_{CYC}	100	-	100	-	ns
TSPIxSCK low level output pulse width	t_{WL}	(t_{CYC}/2) - 13	-	37	-	
TSPIxSCK high level output pulse width	t_{WH}	(t_{CYC}/2) - 13	-	37	-	
TSPIxCSn output ← TSPIxSCK rise/fall time	t_{CSU}	(t_{CYC} × k1) - 20	(t_{CYC} × k1) + 9	80	109	
TSPIxSCK rise/fall → TSPIxCSn hold time	t_{CHD}	(t_{CYC} × (k2 + 0.5))-20	-	130	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	35 - 2× T(Note)	-	10	-	
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	2×T - 10.5 (Note)	-	14.5	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY1}	-18	-	-18	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY2}	-	16	-	16	
TSPIxCSn fall → TSPIxTXD delay time	t_{ODLY3}	(t_{CYC} × (k1 - 0.5))-25	(t_{CYC} × (k1 - 0.5))+9	25	59	

Note: In this case ***[TSPIxCR2]***<RXDLY>=1

2.7V ≤DVDD5=AVDD5< 4.5V

Parameter	Symbol	Equation		fsysm=80MHz k1=k2=1		Unit
		Min	Max	Min	Max	
TSPIxSCK output frequency	f_{CYC}	-	10	-	10	MHz
TSPIxSCK output cycle	t_{CYC}	100	-	100	-	ns
TSPIxSCK low level output pulse width	t_{WL}	(t_{CYC}/2) - 16	-	9	-	
TSPIxSCK high level output pulse width	t_{WH}	(t_{CYC}/2) - 16	-	9	-	
TSPIxCSn output ← TSPIxSCK rise/fall time	t_{CSU}	(t_{CYC} × k1) - 20	(t_{CYC} × k1) + 11	80	111	
TSPIxSCK rise/fall → TSPIxCSn hold time	t_{CHD}	(t_{CYC} × (k2 + 0.5))-20	-	130	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	45 - 2×T (Note)	-	20	-	
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	2×T-10.5 (Note)	-	14.5	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY1}	-18	-	-18	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY2}	-	16	-	16	
TSPIxCSn fall → TSPIxTXD delay time	t_{ODLY3}	(t_{CYC} × (k1 - 0.5))-25	(t_{CYC} × (k1 - 0.5))+13	25	63	

Note: In this case ***[TSPIxCR2]***<RXDLY>=1

Not Recommended for New Design

(2) Slave in SPI mode

4.5V ≤DVDD5=AVDD5≤ 5.5V

Parameter	Symbol	Equation		fsysm=80MHz k1=1		Unit
		Min	Max	Min	Max	
TSPIxSCK Input frequency	f_{CYC}	-	10	-	10	MHz
TSPIxSCK Input cycle	t_{CYC}	100	-	100	-	ns
TSPIxSCK low level Input pulse width	t_{WL}	37	-	37	-	
TSPIxSCK high level Input pulse width	t_{WH}	37	-	37	-	
TSPIxCSIN Input ← TSPIxSCK rise/fall time	t_{CSU1}	(t_{CYC} × (k1 + 0.5)) +20	-	170	-	
TSPIxCSIN Input ← TSPIxSCK rise/fall time	t_{CSU2}	(t_{CYC} × k1) -20	-	80	-	
TSPIxSCK rise/fall → TSPIxCSIN hold time	t_{CHD}	7	-	7	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	7	-	7	-	
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	10	-	10	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY1}	0	-	0	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY2}	-	38	-	38	
TSPIxCSIN fall → TSPIxTXD delay time	t_{ODLY3}	-	(t_{CYC} × (k1 - 0.5)) +5	-	55	
TSPIxCSIN high level input pulse width	t_{WDIS}	T × 2 + 20	-	45	-	

2.7V ≤DVDD5=AVDD5<4.5V

Parameter	Symbol	Equation		fsysm=80MHz k1=1		Unit
		Min	Max	Min	Max	
TSPIxSCK Input frequency	f_{CYC}	-	10	-	10	MHz
TSPIxSCK Input cycle	t_{CYC}	100	-	100	-	ns
TSPIxSCK low level Input pulse width	t_{WL}	37	-	37	-	
TSPIxSCK high level Input pulse width	t_{WH}	37	-	37	-	
TSPIxCSIN Input ← TSPIxSCK rise/fall time	t_{CSU1}	(t_{CYC} × (k1 + 0.5)) +20	-	170	-	
TSPIxCSIN Input ← TSPIxSCK rise/fall time	t_{CSU2}	(t_{CYC} × k1) -20	-	80	-	
TSPIxSCK rise/fall → TSPIxCSIN hold time	t_{CHD}	7	-	7	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	7	-	7	-	
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	10	-	10	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY1}	0	-	0	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY2}	-	49	-	49	
TSPIxCSIN fall → TSPIxTXD delay time	t_{ODLY3}	-	(t_{CYC} × (k1 - 0.5)) +5	-	55	
TSPIxCSIN high level input pulse width	t_{WDIS}	T × 2 + 20	-	45	-	

Not Recommended for New Design

(3) Master in SIO Mode

4.5V ≤DVDD5=AVDD5≤ 5.5V

Parameter	Symbol	Equation		fsysm=80MHz		Unit
		Min	Max	Min	Max	
TSPIxSCK Output Frequency	f_{CYC}	-	10	-	10	MHz
TSPIxSCK Output cycle	t_{CYC}	100	-	100	-	ns
TSPIxSCK Low level Output pulse width	t_{WL}	(t_{CYC}/2)-13	-	37	-	
TSPIxSCK High level Output pulse width	t_{WH}	(t_{CYC}/2)-13	-	37	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	35-2×T (Note)	-	10	-	
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	2×T-10.5 (Note)	-	14.5	-	
TSPIxSCK rise/ fall → TSPIxTXD delay time	t_{ODLY1}	-18	-	-18	-	
TSPIxSCK Rise/ fall → TSPIxTXD delay time	t_{ODLY2}	-	16	-	16	

Note: In this case ***[TSPIxCR2]***<RXDLY>=1

2.7V≤DVDD5=AVDD5<4.5V

Parameter	Symbol	Equation		fsysm=80MHz		Unit
		Min	Max	Min	Max	
TSPIxSCK Output Frequency	f_{CYC}	-	10	-	10	MHz
TSPIxSCK Output cycle	t_{CYC}	100	-	100	-	ns
TSPIxSCK Low level output pulse width	t_{WL}	(t_{CYC}/2)-16	-	9	-	
TSPIxSCK High level output pulse width	t_{WH}	(t_{CYC}/2)-16	-	9	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	45-2×T (Note)	-	20	-	
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	2×T-10.5 (Note)	-	14.5	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY1}	-18	-	-18	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY2}	-	16	-	16	

Note: In this case ***[TSPIxCR2]***<RXDLY>=1

Not Recommended for New Design

(4) Slave in SIO mode

4.5V ≤ DVDD5=AVDD5 ≤5.5V

Parameter	Symbol	Equation		fsysm=80MHz		Unit
		Min	Max	Min	Max	
TSPIxSCK Input Frequency	f_{CYC}	-	10	-	10	MHz
TSPIxSCK Input Cycle	t_{CYC}	100	-	100	-	ns
TSPIxSCK Low level Input Pulse Width	t_{WL}	37	-	37	-	
TSPIxSCK High level Input Pulse Width	t_{WH}	37	-	37	-	
TSPIxSCK rise/fall → TSPIxCSIN hold time	t_{CHD}	7	-	7	-	
TSPIxRXD Input ← SPIxSCK rise/fall time	t_{DSU}	7	-	7	-	
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	10	-	10	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY1}	0	-	0	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY2}	-	38	-	38	

2.7V ≤ DVDD5=AVDD5<4.5V

Parameter	Symbol	Equation		fsysm=80MHz		Unit
		Min	Max	Min	Max	
TSPIxSCK Input Frequency	f_{CYC}	-	10	-	10	MHz
TSPIxSCK Input Cycle	t_{CYC}	100	-	100	-	ns
TSPIxSCK Low level Input Pulse Width	t_{WL}	37	-	37	-	
TSPIxSCK High level Input Pulse Width	t_{WH}	37	-	37	-	
TSPIxSCK rise/fall → TSPIxCSIN hold time	t_{CHD}	7	-	7	-	
TSPIxRXD Input ← SPIxSCK rise/fall time	t_{DSU}	7	-	7	-	
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	10	-	10	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY1}	0	-	0	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY2}	-	38	-	38	

Not Recommended for New Design

(1) 1st clock edge sampling (Master)

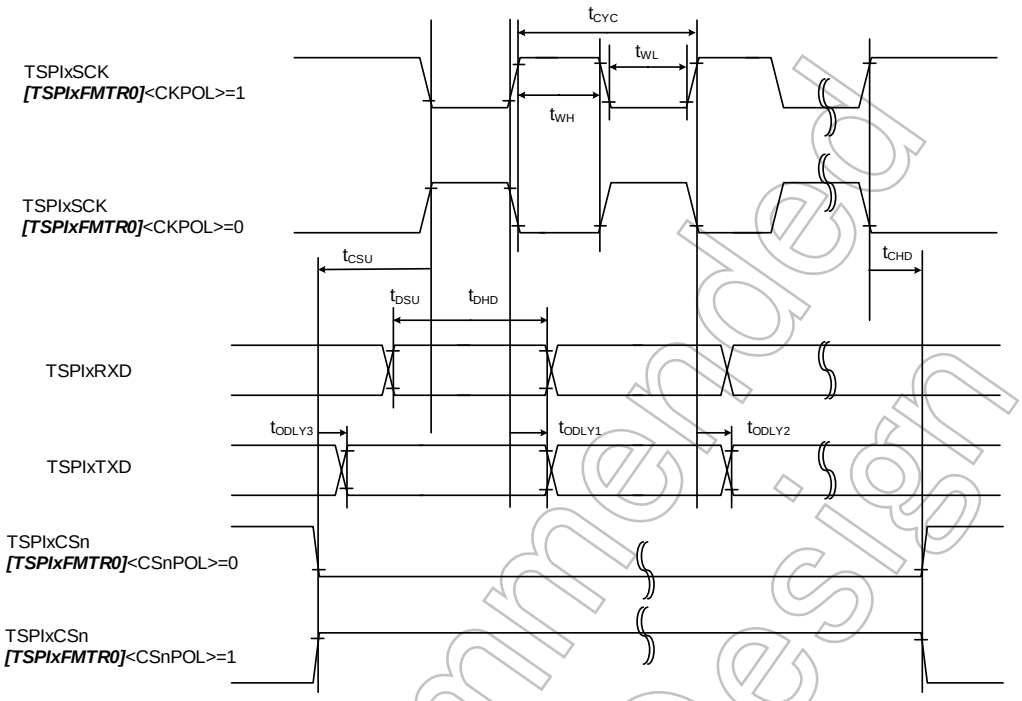


Figure 7.2 1st clock edge sampling (Master)

(2) 2nd clock edge sampling (Master)

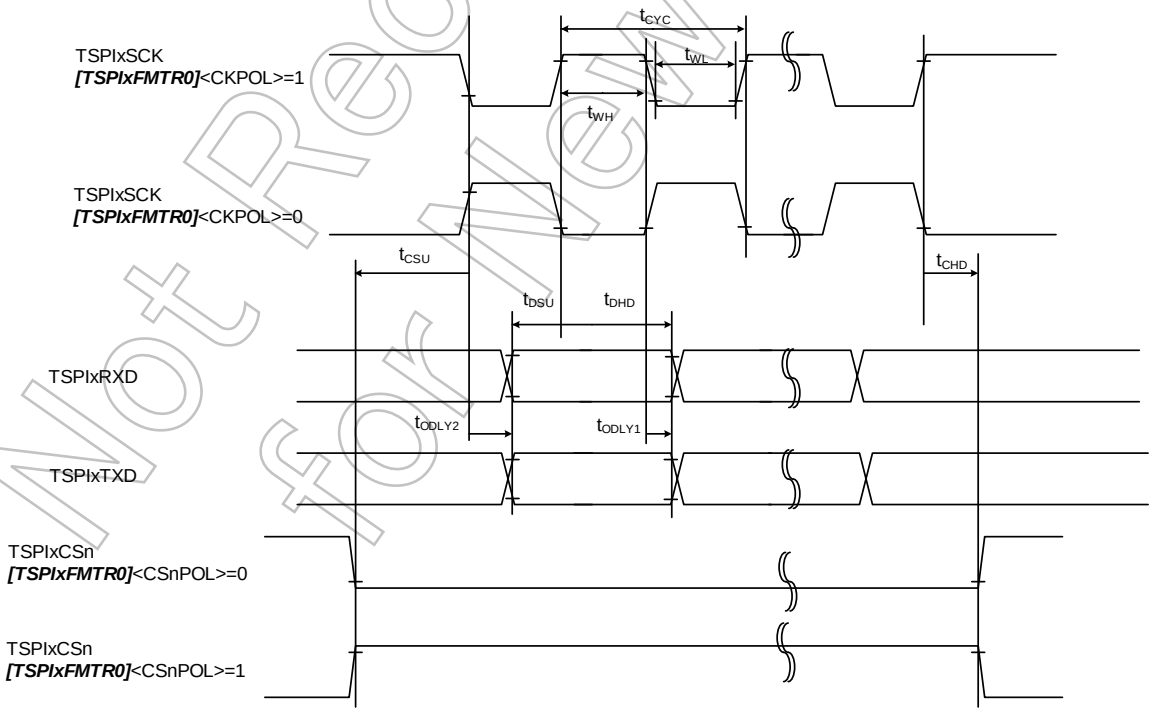


Figure 7.3 2nd clock edge sampling (Master)

Not Recommended for New Design

(3) 2nd clock edge sampling (slave)

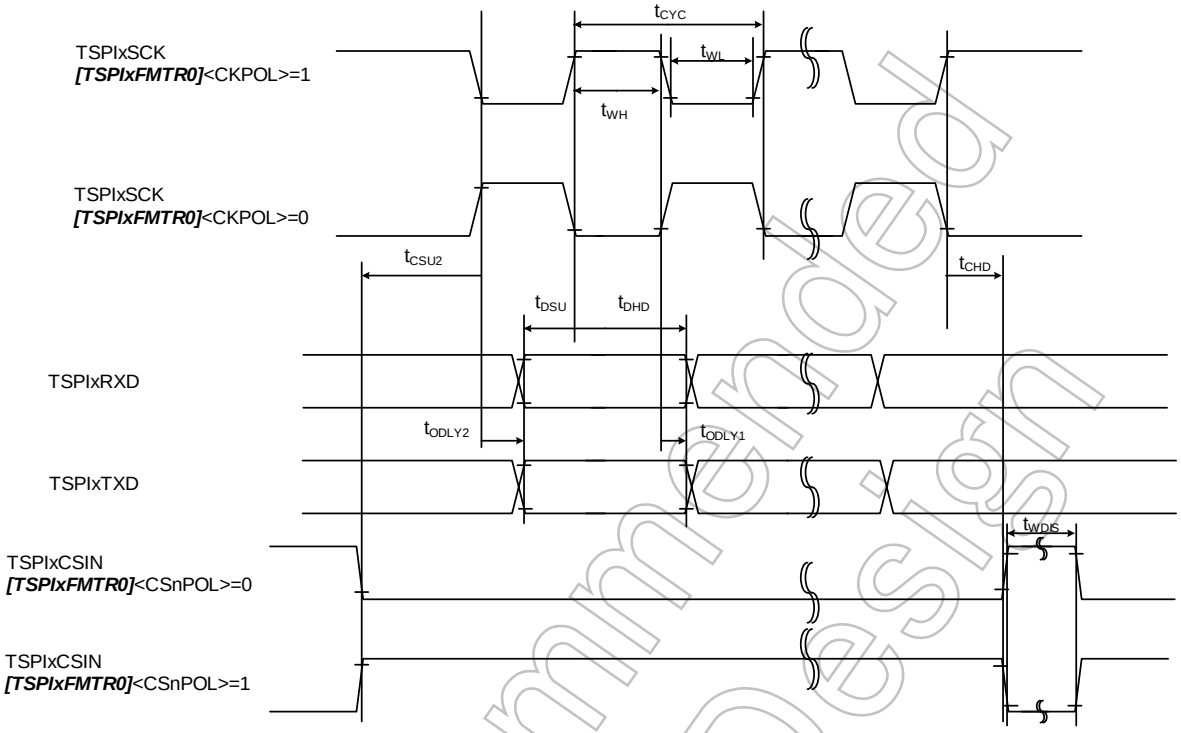


Figure 7.4 2nd clock edge sampling (Slave)

Not Recommended for New Design

7.9.2. I²C Interface (I²C)

7.9.2.1. AC Measurement Conditions

The AC characteristics are the result of the measurement conditions below:

- DVDD5=AVDD5= 2.7 to 5.5 V
- Ta = -40 to 105°C
- Output level: Low = 0.4V
- Input level: High = 0.7 × DVDD5, Low = 0.3 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, and DVDD5B.

7.9.2.2. AC Electrical Characteristics

"T" indicates an operation clock cycle of the I²C. This operation clock has the same cycle of the system clock (fsysm). This cycle depends on the clock gear setting.

"n" indicates a frequency of SCL output clock specified with ***[I2CxCR]***<SCK>.

"p" indicates a prescaler division ratio specified with ***[I2CxPRS]***<PRSCK>.

Parameter	Symbol	Standard mode		Fast mode		Unit
		Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Start condition hold time	$t_{HD, STA}$	4.0	-	0.6	-	µs
SCL clock Low width (Input) (Note1)	t_{LOW}	4.7	-	1.3	-	
SCL clock High width (Input) (Note2)	t_{HIGH}	4.0	-	0.6	-	
Re-start condition setup time (Note5)	$t_{SU, STA}$	4.7	-	0.6	-	
Data hold time (Input) (Note3, 4)	$t_{HD, DAT}$	0	-	0	-	
Data setup time	$t_{SU, DAT}$	250	-	100	-	ns
Stop condition setup time	$t_{SU, STO}$	4.0	-	0.6	-	µs
Bus free time between stop condition and start condition (Note5)	t_{BUF}	4.7	-	1.3	-	

Note1: SCL clock low level width (output): $p \times (2^{n+1}+10)/T$ (***[I2CxOP]***<NFSEL>=0)

Note2: SCL clock high level width (output): $p \times (2^{n+1}+6)/T$ (***[I2CxOP]***<NFSEL>=0)
On I²C bus standard, the maximum speed of standard mode/fast mode is 100kHz/400 kHz respectively. Note that an internal SCL clock frequency is determined by the fsys and the calculation of Note1 and Note2 above-mentioned.

Note3: The data hold time (output) is equal to four cycles of the prescaler clock (Tprsck) started from the internal SCL.

Note4: On I²C bus standard, it is described that a data internal hold time should be set at least 300 ns to avoid unstable condition on the falling of the SCL when the SDA is input; however, this precaution is not supported in this MCU. Also, the edge slope control function for the SCL is not available. Therefore, when the customer designs the MCU, make sure to follow the data hold time (input) in the table above. Note that t_r/t_f on the SCL/SDA should be included in the data hold time.

Note5: Depends on software.

Not Recommended for New Design

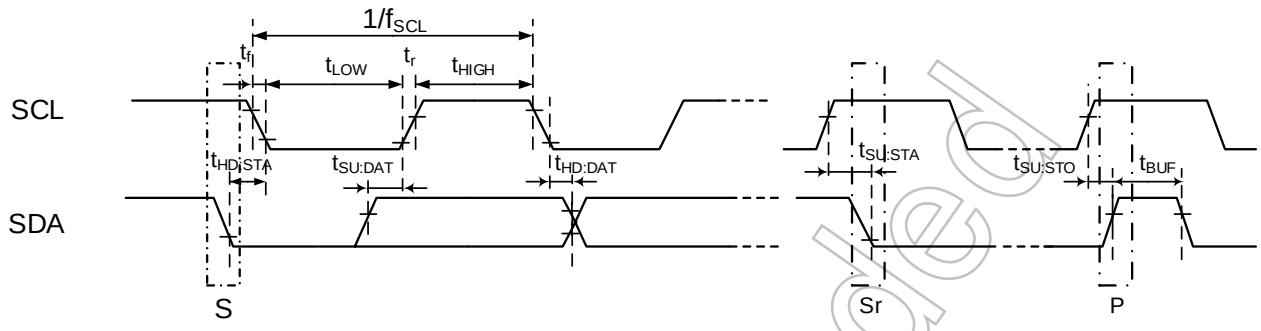


Figure 7.5 AC timing of I²C

Not Recommended for New Design

7.9.3. 32-bit Timer Event Counter (T32A)

This section describes AC characteristics of T32AxINA0/A1, T32AxINB0/B1, and T32AxINC0/C1.

7.9.3.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5=AVDD5= 2.7 to 5.5 V
- Ta = -40 to 105°C
- Input level: High = 0.75 × DVDD5, Low = 0.25 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, and DVDD5B.

7.9.3.2. AC Electrical Characteristics

"T" in the table below indicates the operation clock cycle of the T32A. The operation clock of the T32A is the same cycle as the ΦT0m clock. This cycle is depending on the Prescaler Clock setting.

(1) Operation other than the pulse count

Parameter	Symbol	Calculation		ΦT0m=80 MHz		Unit
		Min	Max	Min	Max	
Low level pulse width	t_{VCKL}	2T + 20	-	45	-	ns
High level pulse width	t_{VCKH}	2T + 20	-	45	-	

(2) At the pulse count

Parameter	Symbol	Calculation		ΦT0m=80 MHz NF=0		Unit
		Min	Max	Min	Max	
Pulse cycle	t_{DCYC}	1000	-	1000	-	ns
Low level pulse width	t_{PWL}	500	-	500	-	
High level pulse width	t_{PWH}	500	-	500	-	
Input setup	t_{ABS}	(NF+1) × T +20	-	32.5	-	
Input hold	t_{ABH}	(NF+1) × T +20	-	32.5	-	

NF Value depends on the ***[T32AxPLSCR]***<NF[1:0]> setting as follows.

[T32AxPLSCR]<NF[1:0]>	NF Value of Formula
00	0
01	2
10	4
11	8

Not Recommended for New Design

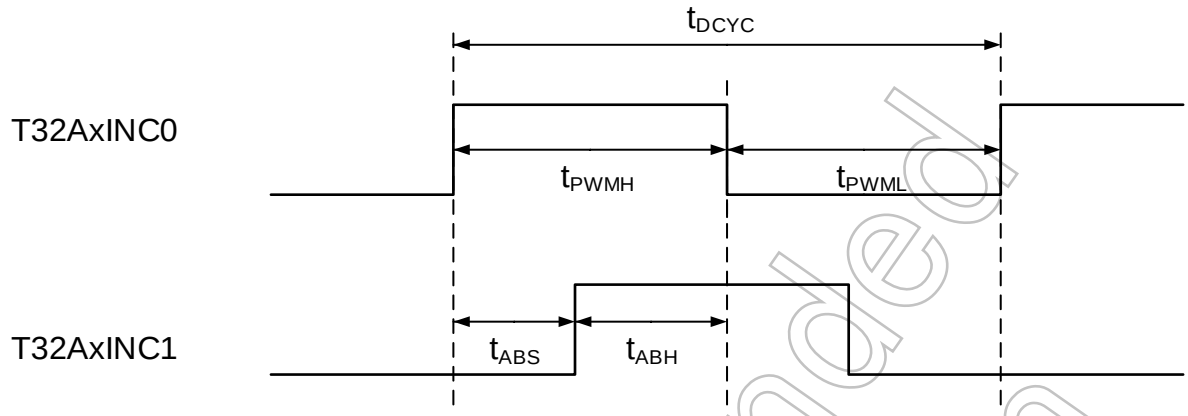


Figure 7.6 Count Pulse input

7.9.4. External Interrupt

7.9.4.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5=AVDD5= 2.7V to 5.5V
- Ta = -40 to 105°C
- Input level: High = 0.75 × DVDD5, Low = 0.25 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, and DVDD5B.

7.9.4.2. AC Electrical Characteristics

"T" in the table below indicates the cycle of the system clock (fsys).

(1) NORMAL, IDLE mode

Parameter	Symbol	Calculation		fsys=160 MHz		Unit
		Min	Max	Min	Max	
Low level pulse width	t_{INTAL1}	T + 100	-	106.25	-	ns
High level pulse width	t_{INTAH1}	T + 100	-	106.25	-	

(2) STOP1 mode

Parameter	Symbol	Calculation				Unit
		Min	Max	Min	Max	
Low level pulse width	t_{INTCL2}	125	-	125	-	ns
High level pulse width	t_{INTCH2}	125	-	125	-	

Not Recommended for New Design

7.9.5. Trigger Input (TRGINx)

7.9.5.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5=AVDD5= 2.7V to 5.5V
- Ta = -40 to 105°C
- Input level: High = 0.75 × DVDD5, Low = 0.25 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, and DVDD5B.

7.9.5.2. AC Electrical Characteristics

"T" in the table below indicates the cycle of the system clock (fsysm).

Parameter	Symbol	Calculation		fsysm=80 MHz		Unit
		Min	Max	Min	Max	
Low level pulse width	t_{ADL}	2T + 20	-	45	-	ns
High level pulse width	t_{ADH}	2T + 20	-	45	-	

Not Recommended for New Design

7.9.6. Debug Communication

7.9.6.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5=AVDD5= 2.7V to 5.5V
- Ta = -40 to 80°C
- Output level: High = 0.8 ×DVDD5, Low = 0.2×DVDD5
- Input level: High = 0.75 × DVDD5, Low = 0.25 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, and DVDD5B.

7.9.6.2. SW Interface

4.5V ≤DVDD5=AVDD5≤ 5.5V

Parameter	Symbol	Min	Max	Unit
CLK cycle	t_{dck}	100	-	ns
Output data hold from on the rising edge of CLK	t_{d1}	4	-	
Output data valid from on the rising edge of CLK	t_{d2}	-	33	
From input data valid to the rising edge of CLK	t_{ds}	20	-	
Input data hold from on the rising edge of CLK	t_{dh}	15	-	

2.7V ≤DVDD5=AVDD5< 4.5V

Parameter	Symbol	Min	Max	Unit
CLK cycle	t_{dck}	100	-	ns
Output data hold from on the rising edge of CLK	t_{d1}	4	-	
Output data valid from on the rising edge of CLK	t_{d2}	-	45	
From input data valid to the rising edge of CLK	t_{ds}	20	-	
Input data hold from on the rising edge of CLK	t_{dh}	15	-	

Not Recommended for New Design

7.9.6.3. JTAG Interface

4.5V ≤DVDD5=AVDD5≤ 5.5V

Parameter	Symbol	Min	Max	Unit
CLK cycle	t_{dck}	100	-	ns
Output data hold from on the rising edge of CLK	t_{d3}	4	-	
Output data valid from on the rising edge of CLK	t_{d4}	-	33	
From input data valid to the rising edge of CLK	t_{ds}	20	-	
Input data hold from on the rising edge of CLK	t_{dh}	15	-	

2.7V ≤DVDD5=AVDD5< 4.5V

Parameter	Symbol	Min	Max	Unit
CLK cycle	t_{dck}	100	-	ns
Output data hold from on the rising edge of CLK	t_{d3}	4	-	
Output data valid from on the rising edge of CLK	t_{d4}	-	45	
From input data valid to the rising edge of CLK	t_{ds}	20	-	
Input data hold from on the rising edge of CLK	t_{dh}	15	-	

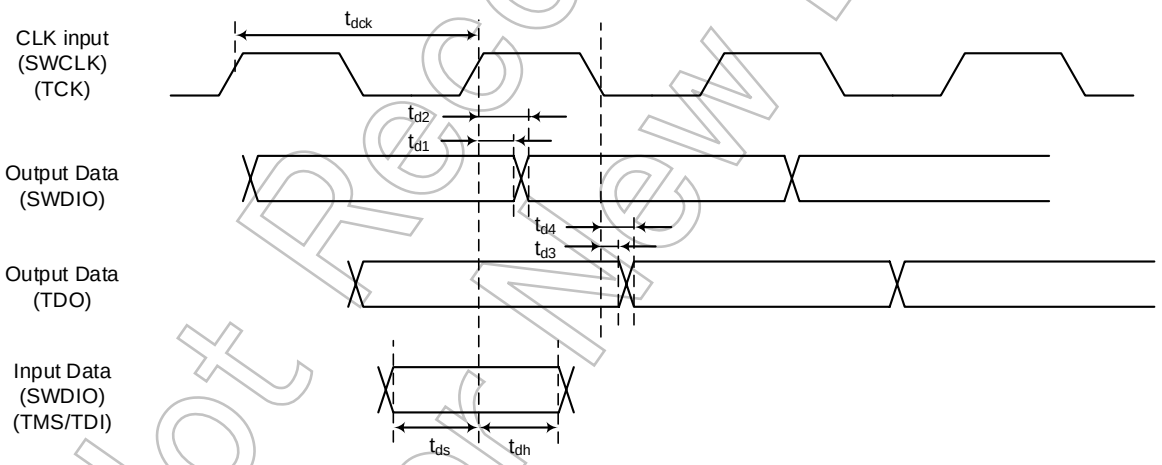


Figure 7.7 JTAG/SW waveform

Not Recommended for New Design

7.9.6.4. ETM Trace

5.0V≤DVDD5=AVDD5≤5.5V
Tj=80°C (Note)

Parameter	Symbol	Min	Max	Unit
TRACECLK cycle	t_{tclk}	25	-	ns
Data valid from rising on TRACECLK	t_{setupr}	2	-	
TRACEDATA hold from on the rising edge of TRACECLK	t_{holdr}	1	-	
TRACEDATA valid from on the falling edge of TRACECLK	t_{setupf}	2	-	
TRACEDATA hold from on the falling edge of TRACECLK	t_{holdf}	1	-	

Note: Refer to Note3 of "7.1.Absolute Maximum Ratings".

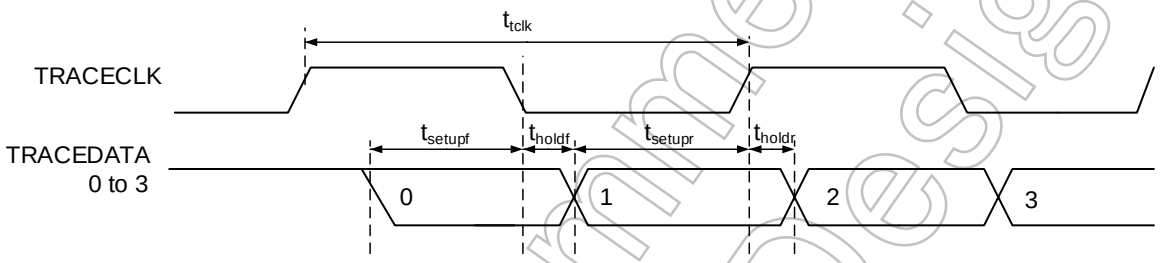


Figure 7.8 Trace signal waveform

Not Recommended for New Design

7.9.6.5. Non Break Debug Interface (NBDIF)

Parameter	Symbol	Min	Max	Unit
NBDCLK cycle time	t_{NDCYC}	80	-	ns
NBDCLK low level pulse width	t_{NDL}	35	-	
NBD DATA output delay time	t_{NDD}	-	t_{NDCYC} - 20	
NBD DATA output hold time	t_{NDHD}	5	-	
NBD DATA setup time	t_{NDS}	20	-	
NBD DATA hold time	t_{NDH}	5	-	
NBDSYNC setup time	t_{NDSYS}	20	-	
NBDSYNC output hold time	t_{NDSYH}	5	-	

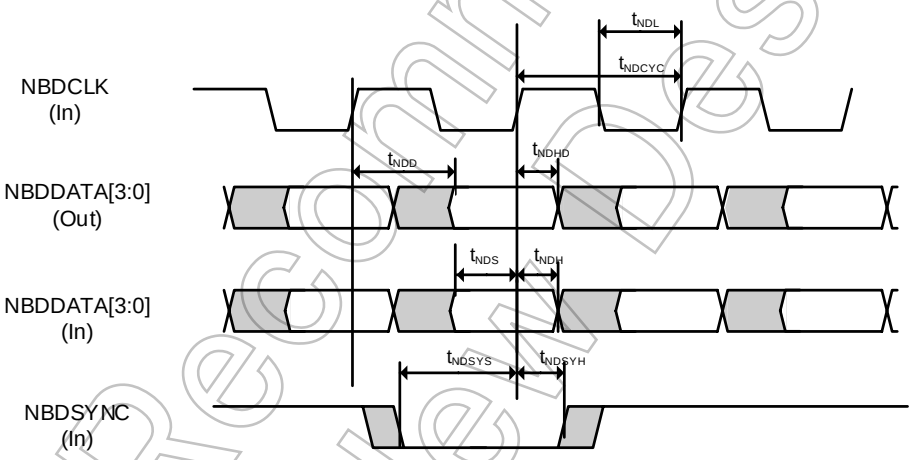


Figure 7.9 AC timing of NBDIF

Not Recommended for New Design

7.9.7. Noise Filter Characteristics

Parameter	Condition	Min	Typ.	Max	Unit
Noise cancel width	DVDD5 = 2.7 to 5.5V Ta = -40 to 105°C	15	30	60	ns

Note: DVDD5 is a generic name for DVDD5A, and DVDD5B.

7.9.8. External Clock Input

7.9.8.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5=AVDD5= 2.7V to 5.5V
- Ta = -40 to 105°C
- Input level: High = 0.75 × DVDD5, Low = 0.25 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, and DVDD5B.

7.9.8.2. AC Electrical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit
Clock frequency($1/t_{ehcin}$)	$f_{EHCLKIN}$	6	-	10	MHz
Clock duty	-	45	-	55	%
Clock rise time	t_r	-	-	10	ns
Clock fall time	t_f	-	-	10	ns

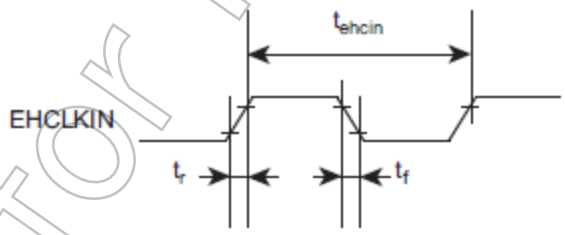


Figure 7.10 External clock input waveform

Not Recommended for New Design

7.10. Flash Memory Characteristics

7.10.1. Code Flash

DVDD5=2.7V to 5.5V
Ta= -40 to 105°C

Parameter	Condition	Min	Typ.	Max	Unit
Endurance	-	-	-	10,000	cycles
Programming time	Word Program time	-	29.5	-	μs
Erase time	Page Erase time	-	18.1	-	ms
	Block Erase time	-	144.2	-	
	Area Erase time(Note2)	-	18.1	-	

Note1: DVDD5 is a generic name for DVDD5A, and DVDD5B. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

Note2: No block with effective protection.

7.10.2. Data Flash

DVDD5=2.7V to 5.5V
Ta= -40 to 105°C

Parameter	Condition	Min	Typ.	Max	Unit
Endurance	-	-	-	100,000	cycles
Programming time	-	-	64.7	-	μs
Erase time	Page Erase time	1	-	3.9	ms
	Block Erase time	15.4	-	62.1	
	Area Erase time(Note2)	-	9.2	-	

Note1: DVDD5 is a generic name for DVDD5A, and DVDD5B. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

Note2: No block with effective protection.

7.10.3. Chip Erase

DVDD5=2.7V to 5.5V
Ta= -40 to 105°C

Parameter	Condition	Min	Typ.	Max	Unit
Chip Erase time	Erasing of Code Flash, Data Flash. Protect Bits(Code), Protect Bits(Data), and Security Bits	-	64.0	-	ms

Note1: DVDD5 is a generic name for DVDD5A, and DVDD5B. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

Note2: When Chip Erase command executes, no block with effective protection.

Not Recommended for New Design

7.11. Regulator

DVDD5=2.7V to 5.5V
Ta= -40 to 105°C

Parameter	Condition	Min	Typ.	Max	Unit
Capacitance of REGOUT1 capacitor	-	-	4.7	-	µF
Capacitance of REGOUT2 capacitor		-	4.7	-	

Note: DVDD5 is a generic name for DVDD5A, and DVDD5B. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

Not Recommended for New Design

7.12. Oscillation Circuit

7.12.1. Internal Oscillation

DVDD5=2.7V to 5.5V
Ta= -40 to 105°C

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Oscillation frequency	f_{IHOSC1}	Factory out, IC data	-	10	-	MHz
	f_{IHOSC2}		-	10	-	

Note1: DVDD5 is a generic name for DVDD5A, and DVDD5B. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

Note2: Not included the influence depend on the variations after Factory shipping. Please execute oscillator adjustment by the trimming register, if it is required.

7.12.2. External Oscillator

DVDD5=2.7V to 5.5V
Ta= -40 to 105°C

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Oscillation frequency	f_{EHOSC}	-	6	-	12	MHz

Note1: DVDD5 is a generic name for DVDD5A, and DVDD5B. DVSS is a generic name for DVSSA, DVSSB, and DVSSC.

Note2: Please contact the oscillator vendor, regarding the matching data of the device and the oscillator.

7.12.3. Oscillation Circuit

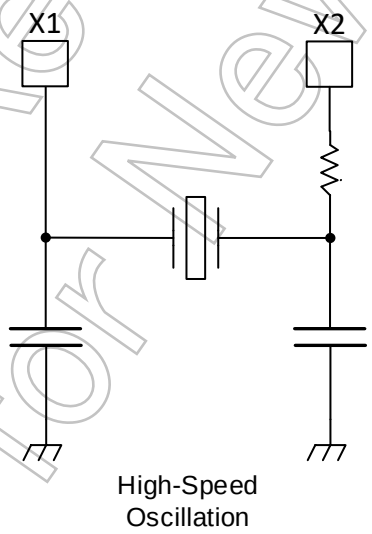


Figure 7.11 Oscillation circuit sample

To obtain a stable oscillation, load capacity and the position of the oscillator must be configured properly.

Since these factors are strongly affected by substrate patterns, please evaluate oscillation stability using the substrate you use.

This product has been evaluated by the oscillator vendor below. Please refer this information when selecting external parts.

Not Recommended for New Design

7.12.4. Ceramic Oscillator

This product has been evaluated by the ceramic oscillator by Murata Manufacturing Co., Ltd.
Please refer to the company's website for details.

7.12.5. Crystal Oscillator

This product has been evaluated by the crystal oscillator by KYOCERA Corporation.
Please refer to the company's website for details.

7.12.6. Precautions for designing printed circuit board

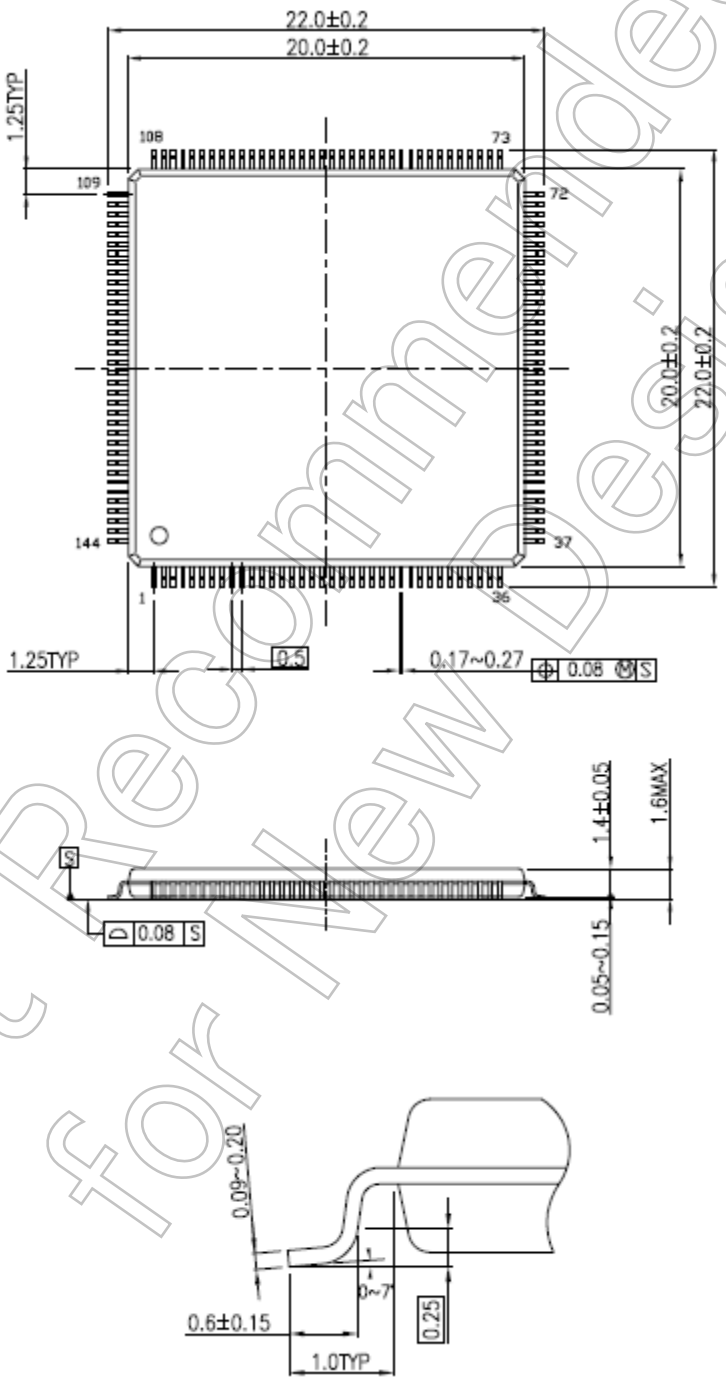
Be sure to design printed circuit board patterns that connect a crystal unit with other oscillation elements so that the length of such patterns become shortest possible to prevent deterioration of characteristics due to stray capacitances and wiring inductance. For multi-layer circuit boards, it is important not to wire the ground and other signal patterns right beneath the oscillation circuit. For more information, please refer to the URL of the oscillator vendor.

Not Recommended for New Design

8. Package Dimensions

8.1. P-LQFP144-2020-0.50-002

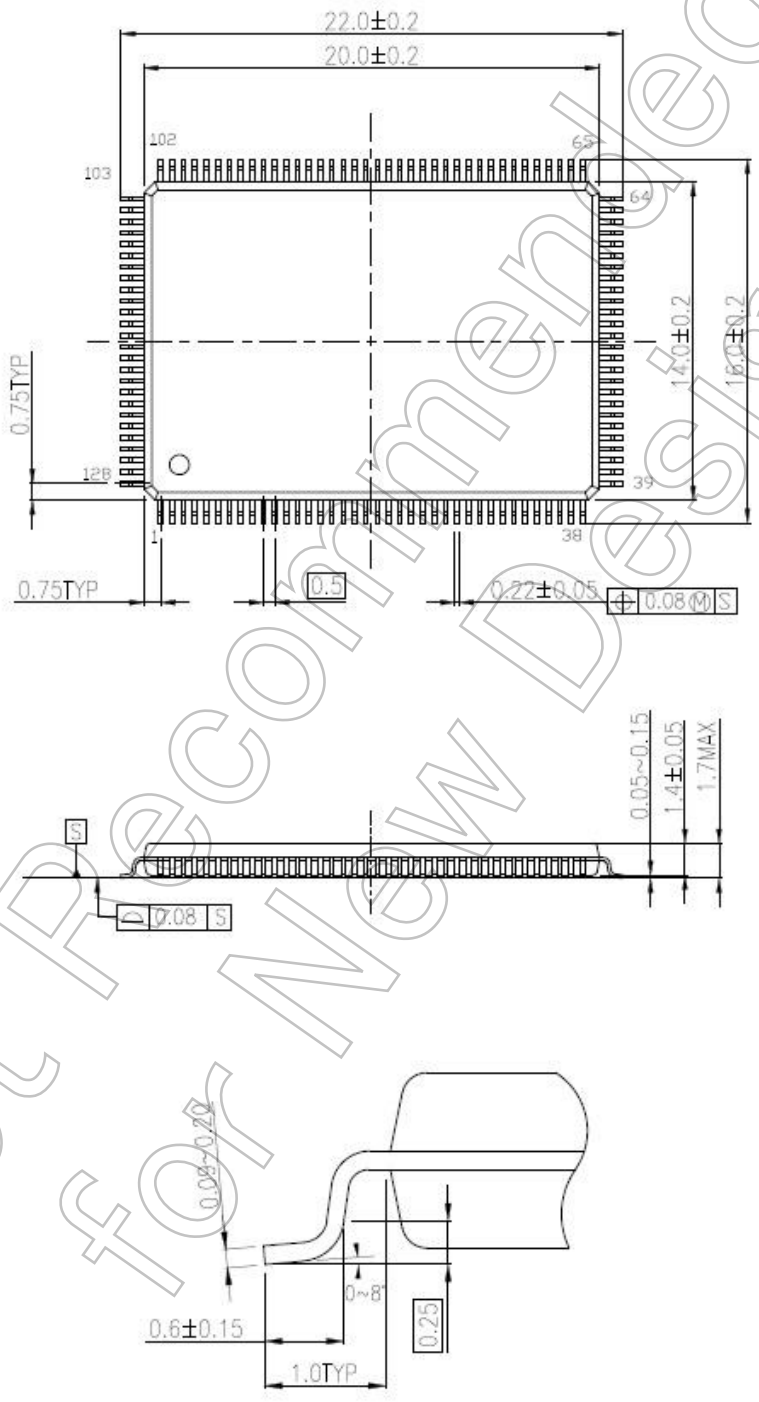
Unit: mm



Not Recommended for New Design

8.2. P-LQFP128-1420-0.50-001

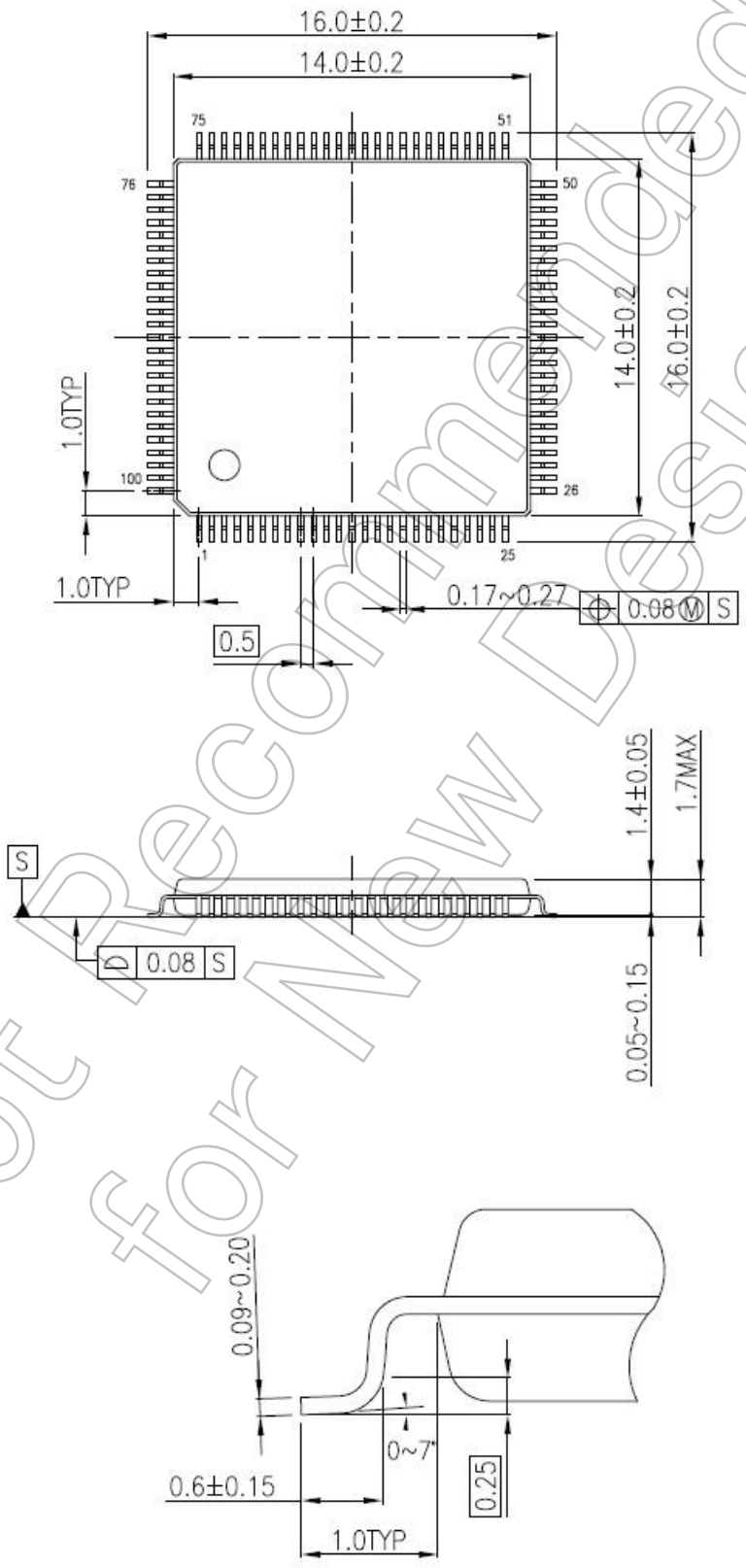
Unit: mm



Not Recommended for New Design

8.3. P-LQFP100-1414-0.50-002

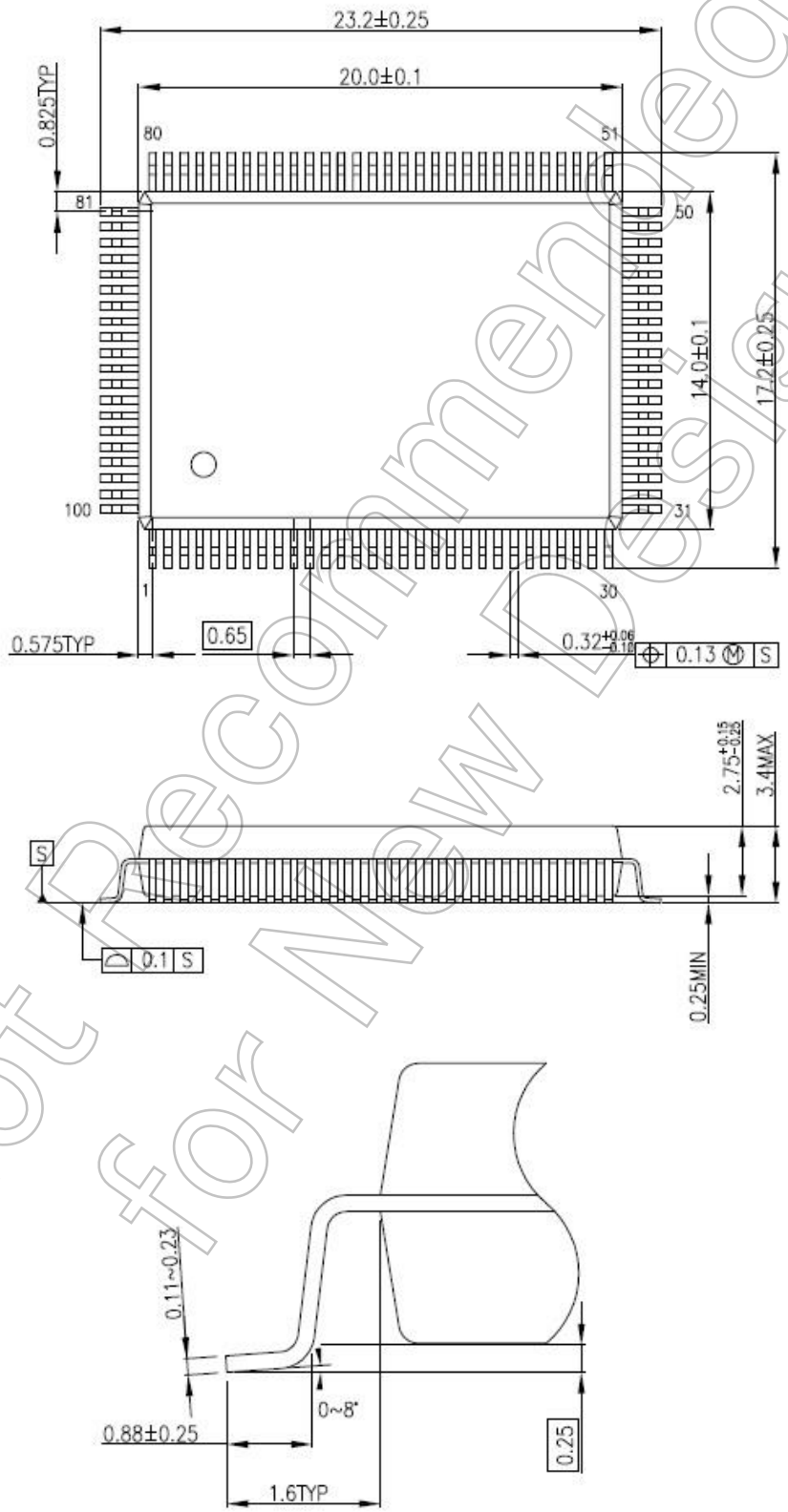
Unit: mm



Not Recommended for New Design

8.4. P-QFP100-1420-0.65-001

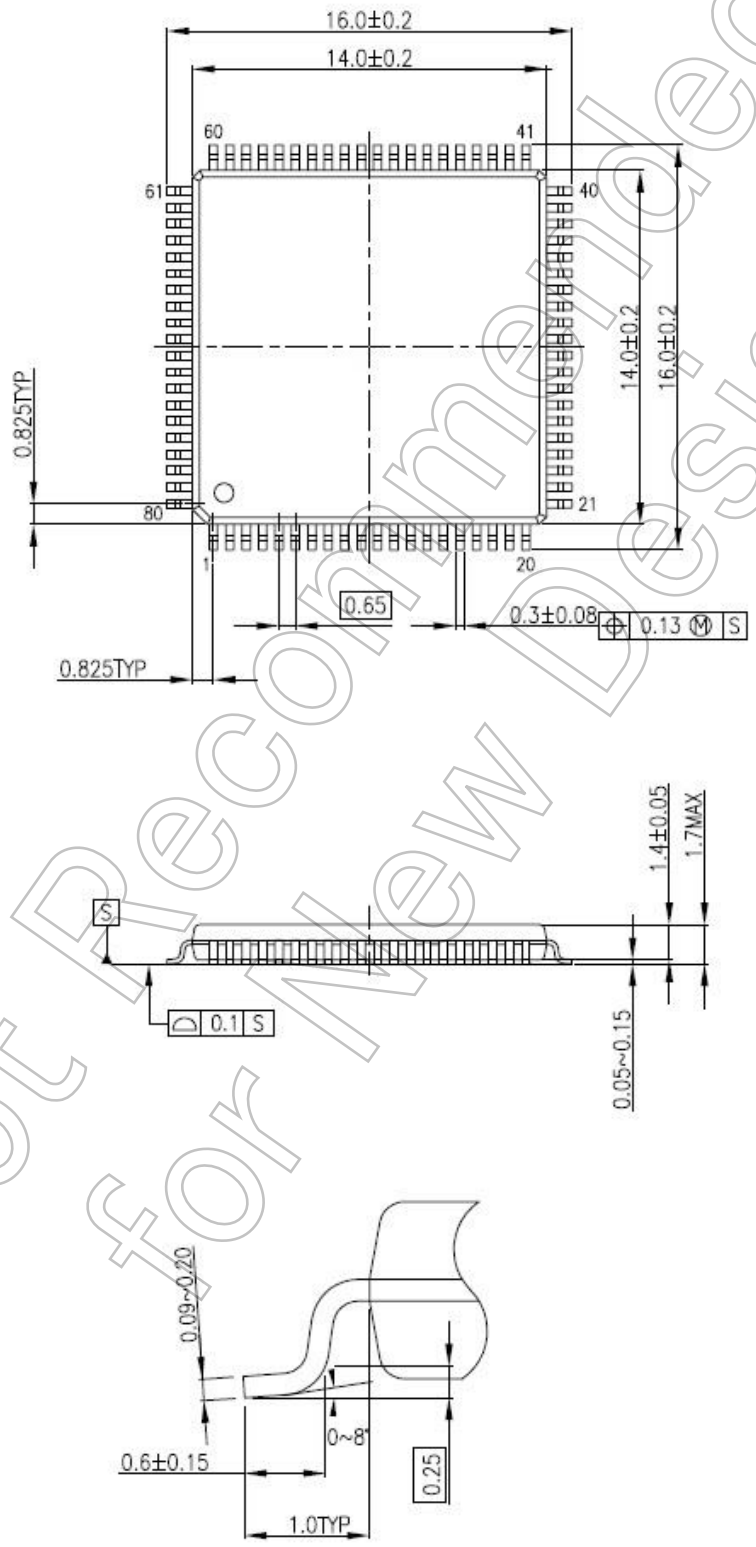
Unit: mm



Not Recommended for New Design

8.5. P-LQFP80-1414-0.65-001

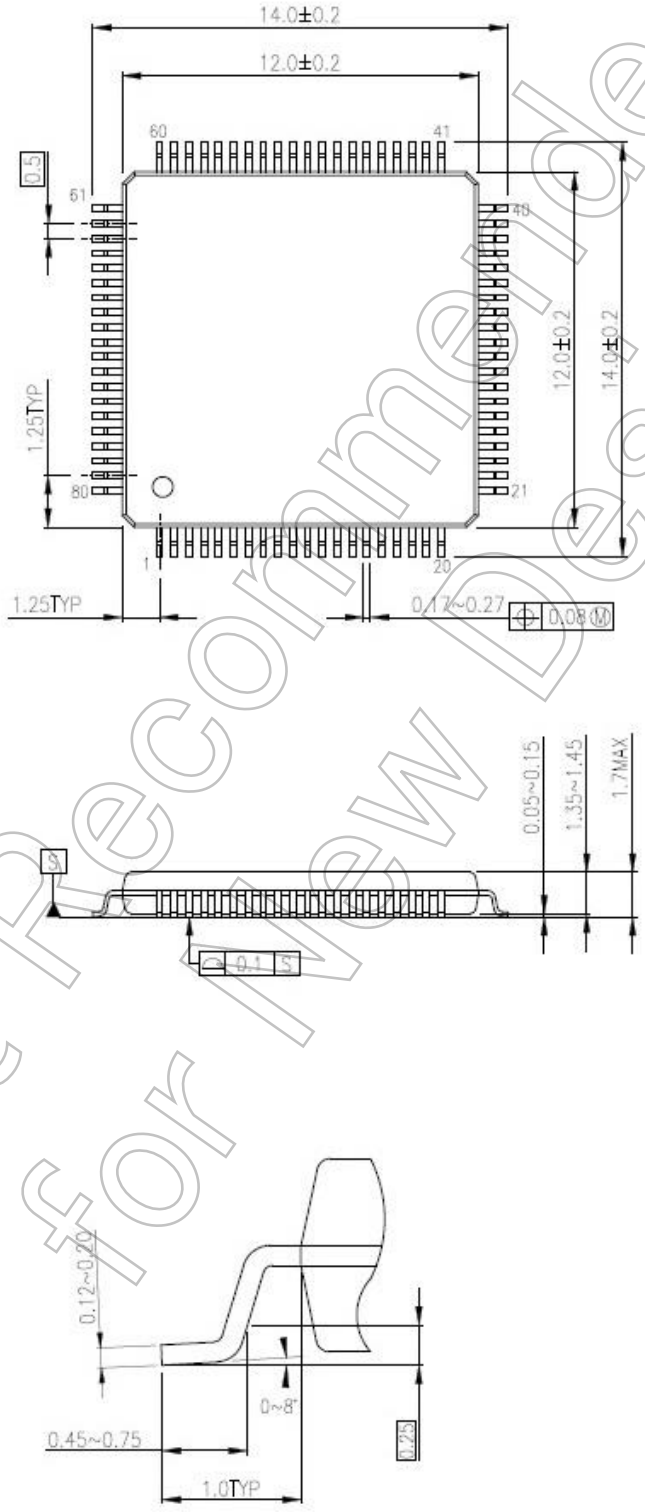
Unit: mm



Not Recommended for New Design

8.6. P-LQFP80-1212-0.50-003

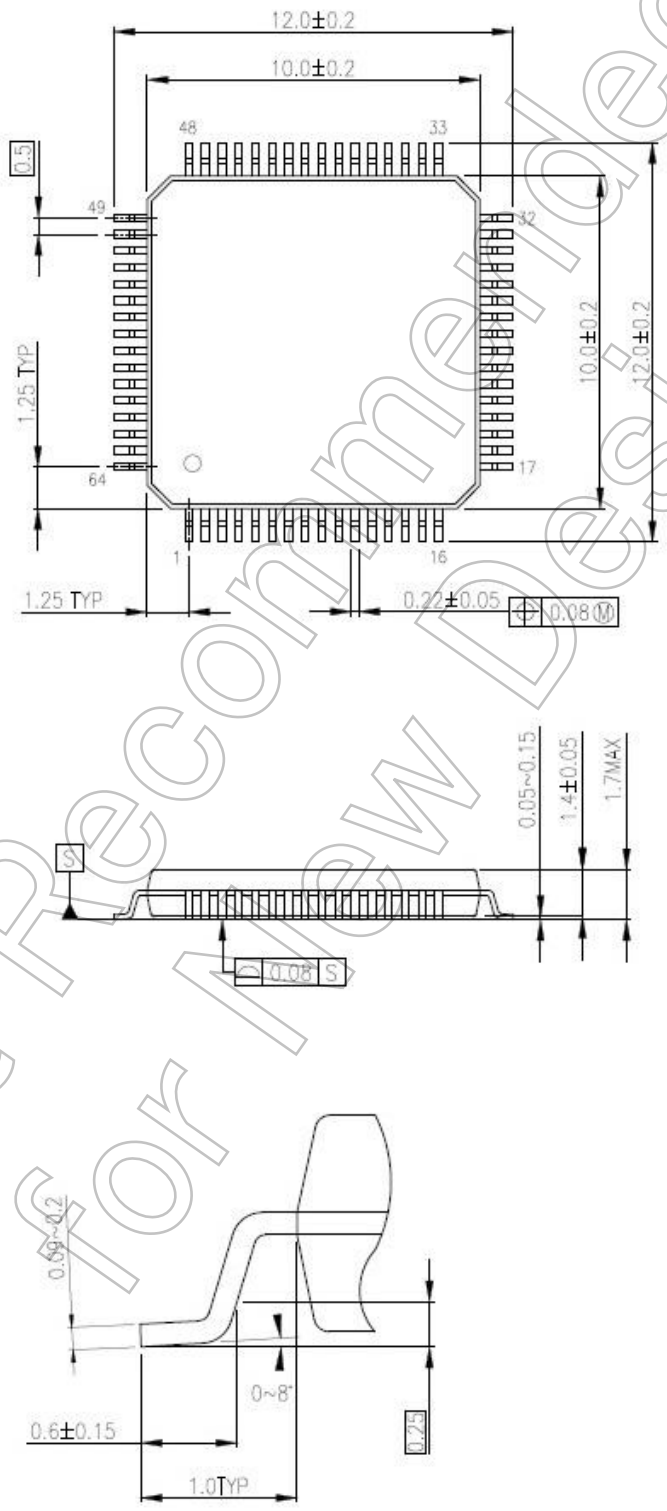
Unit: mm



Not Recommended for New Design

8.7. P-LQFP64-1010-0.50-003

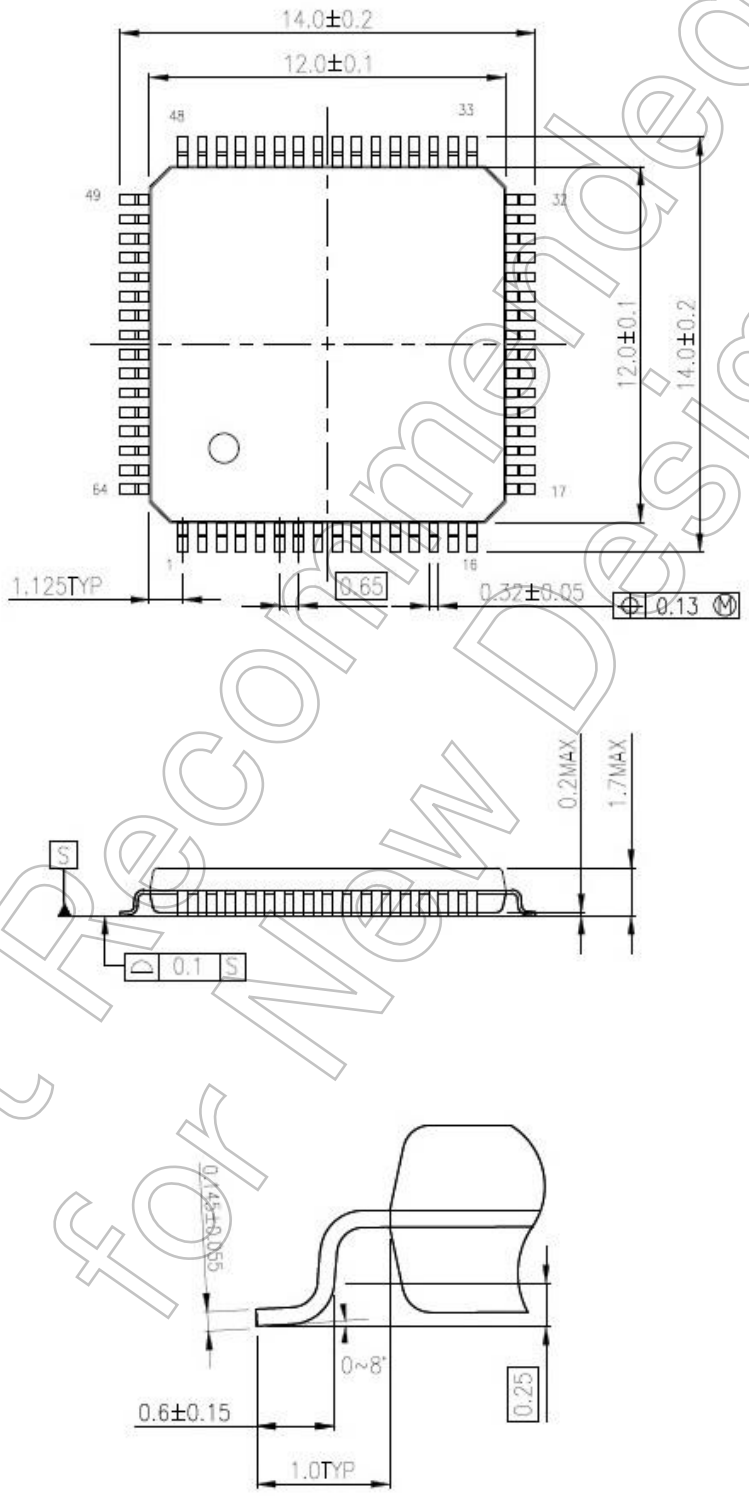
Unit: mm



Not Recommended for New Design

8.8. P-LQFP64-1212-0.65-001

Unit: mm



Not Recommended for New Design

9. Precautions

This Page explains general precautions on the use of our MCUs.

Note that if there is a difference between the general precautions and the description in the body of the document, the description in the body of the document has higher priority.

(1) The MCUs' operation at power on

At power on, internal state of the MCUs is unstable. Therefore, state of the pins is undefined until reset operation is completed.
When a reset is performed by an external reset pin, pins of the MCUs that use the reset pin are undefined until reset operation by the external pin is completed.
Also, when a reset is performed by the internal power on reset, pins of the MCUs that use the internal power on reset are undefined until power supply voltage reaches the voltage at which power on reset is valid.

(2) Unused pins

Unused input/output ports of the MCUs are prohibited to use. The pins are high-impedance.
Generally, if MCUs operate while the high-impedance pins left open, electrostatic damage or latch-up may occur in the internal LSI due to induced voltage influenced from external noise.
We recommend that each unused pin should be connected to the power supply pins or GND pins via resistors.

(3) Clock oscillation stability

A reset state must be released after the clock oscillation becomes stable. If the clock is changed to another clock while the program is in progress, wait until the clock is stable.

Not Recommended for New Design

10. Revision History

Table 10.1 Revision History

Revision	Date	Description
1.0	2018-10-16	First release
1.1	2021-10-15	- Terms and Abbreviations: modified the content of TSPI - 7.8. Modified Min/Max value of V_{LVL4} to V_{LVL7}

Not Recommended for New Design

Appendix

List of All pins

Combination Function A to C: These are the functions which become effective without setting up port function registers.

Combination Function 1 to 7: These are the functions which become effective with setting up port function registers.

M4KQ LQFP144	M4KP LQFP128	M4KN QFP100	M4KN LQFP100	M4KM LQFP80	M4KL LQFP64	Pin Name	Combination Function A	Combination Function B	Combination Function C	Combination Function 1	Combination Function 2	Combination Function 3	Combination Function 4	Combination Function 5	Combination Function 6	Combination Function 7	Input/ Output	PU/PD	5V_T	SMT/ CMOS	Under Reset	After Reset
1	2	4	1	2	2	PU0		INT12		UT2TXDA	UT2RXD	I2C1SDA	T32A02 INB1		UO2		I/O	PU/PD	YES	SMT	Hi-z	Hi-z
2	3	5	2	3	3	PU1		INT07a		UT2RXD	UT2TXDA	I2C1SCL	T32A02 INA0	T32A02 INC0	XO2		I/O	PU/PD	YES	SMT	Hi-z	Hi-z
3	4	6	3	4	4	PU2		INT07b					T32A02 OUTA	T32A02 OUTC	VO2		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
4	5	7	4	5	5	PU3		INT08a		UT1RTS_N			T32A02 INB0	ENC2A	YO2		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
5	6	8	5	6	6	PU4		INT08b		UT1CTS_N			T32A02 OUTB	T32A02 INC1	WO2		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
6	7	9	6	7	7	PU5		INT13		UT1TXDA	UT1RXD		T32A02 INA1	ENC2B	ZO2		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
7	8	10	7	8	8	PU6		INT09		UT1RXD	UT1TXDA			ENC2Z	EMG2		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
8	9	11	8	-	-	PU7									OVV2	PMD2 DBG	I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
9	10	12	9	9	-	PN0				UT0TXDA	UT0RXD	NBDDATA2 (Note3)	T32A05 INA0	T32A05 INC0	ENC0A	TRACE DATA2 (Note3)	I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
10	11	13	10	10	-	PN1		INT16a		UT0RXD	UT0TXDA	NBDDATA3 (Note3)	T32A05 OUTA	T32A05 OUTC	ENC0B	TRACE DATA3 (Note3)	I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
11	12	14	11	11	-	PN2		INT16b		UT0CTS_N			T32A05 INA1	T32A05 INC1	ENC0Z		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
12	13	15	12	-	-	PV0					TSPI1CSIN		T32A01 OUTB				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
13	14	16	13	-	-	PV1				UT0RTS_N	TSPI1RXD						I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
14	15	-	-	-	-	PV2				UT1RTS_N	TSPI1TXD						I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
15	16	-	-	-	-	PV3				UT1CTS_N	TSPI1SCK						I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
16	-	-	-	-	-	PW0							T32A04 INA0	T32A04 INC0			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
17	-	-	-	-	-	PW1							T32A04 OUTA	T32A04 OUTC			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
18	-	-	-	-	-	PW2							T32A04 INA1	T32A04 INC1			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
19	-	-	-	-	-	PW3		INT20b					T32A04 INB0				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
20	-	-	-	-	-	PW4		INT20a					T32A04 INB1				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
21	-	-	-	-	-	PW5							T32A04 OUTB				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
22	-	-	-	-	-	PW6				UT3RTS_N							I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
23	-	-	-	-	-	PW7				UT3CTS_N							I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
24	17	17	14	12	9	DVSSC											-	-	-	-	-	-
25	18	18	15	13	-	PA0				TSPI0CSIN			T32A00 INB0				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
26	19	19	16	14	-	PA1		INT15		TSPI0CS1			T32A00 INB1				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
27	20	20	17	15	10	PA2		INT00		TSPI0RXD			T32A00 INA0	T32A00 INC0	PMD2 DBG	TRGIN0	I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
28	21	21	18	16	11	PA3		INT01b		TSPI0TXD			T32A00 OUTA	T32A00 OUTC		TRGIN1	I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
29	22	22	19	17	12	PA4		INT01a		TSPI0SCK			T32A00 OUTB			TRGIN2	I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
30	23	-	-	-	-	PP4							T32A01 OUTA	T32A01 OUTC	ENC0B		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
31	24	-	-	-	-	PP5							T32A01 INA1	T32A01 INC1	ENC0Z		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
32	25	-	-	-	-	PP6				UT3RTS_N	TSPI1CS0						I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
33	26	-	-	-	-	PP7				UT3CTS_N	TSPI1CS1						I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
34	27	23	20	18	13	PL0	AINA16										I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
35	28	24	21	19	14	PL1	AINA15										I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
36	29	25	22	20	15	PL2	AINA17										I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
37	30	26	23	21	16	PL3	AINA14										I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
38	31	27	24	22	17	PL4	AINA18										I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
39	32	28	25	23	18	PL5	AINA13										I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
40	33	29	26	24	19	PL6	AINA09										I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
41	34	30	27	25	20	PL7	AINA08										I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
42	35	31	28	-	-	PM0	AINA07										I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
43	36	32	29	-	-	PM1	AINA06										I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
44	37	33	30	-	-	PM2	AINA05										I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
45	38	-	-	-	-	PM3	AINA04										I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
46	39	-	-	-	-	PM4	AINA03										I/O	PU/PD	N/A	SMT	Hi-z	Hi-z

Not Recommended for New Design

M4KQ LQFP144	M4KP LQFP128	M4KN QFP100	M4KN LQFP100	M4KM LQFP80	M4KL LQFP64	Pin Name	Combination Function A	Combination Function B	Combination Function C	Combination Function 1	Combination Function 2	Combination Function 3	Combination Function 4	Combination Function 5	Combination Function 6	Combination Function 7	Input/ Output	PU/PD	5V_T	SMT/ CMOS	Under Reset	After Reset
47	40	-	-	-	-	PM5	AINA02										I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
48	41	-	-	-	-	PM6	AINA01										I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
49	42	-	-	-	-	PM7	AINA00										I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
50	43	34	31	26	21	VREFL											-	-	-	-	-	-
51	44	35	32	27	22	AVSS											-	-	-	-	-	-
52	45	36	33	28	23	AVDD5											-	-	-	-	-	-
53	46	37	34	29	24	VREFH											-	-	-	-	-	-
54	47	-	-	-	-	PK7	AINB07										I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
55	48	-	-	-	-	PK6	AINB06										I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
56	49	-	-	-	-	PK5	AINB05										I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
57	50	38	35	30	-	PK4	AINB04										I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
58	51	39	36	31	-	PK3	AINB03										I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
59	52	40	37	32	25	PK2	AINB02										I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
60	53	41	38	33	26	PK1	AINB01										I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
61	54	42	39	34	27	PK0	AINB00										I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
62	55	-	-	-	-	PJ7	AINC07										I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
63	56	-	-	-	-	PJ6	AINC06										I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
64	57	43	40	-	-	PJ5	AINC05										I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
65	58	44	41	-	-	PJ4	AINC04										I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
66	59	45	42	35	-	PJ3	AINC03										I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
67	60	46	43	36	28	PJ2	AINC02										I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
68	61	47	44	37	29	PJ1	AINC01										I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
69	62	48	45	38	30	PJ0	AINC00										I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
70	63	49	46	39	31	PC0				UT0TXDA	UT0RXD		I2C0SDA	T32A02 INA0	T32A02 INC0		I/O	PU/PD	YES	SMT	Hi-z	Hi-z
71	64	50	47	40	32	PC1		INT02a		UT0RXD	UT0TXDA		I2C0SCL	T32A02 OUTA	T32A02 OUTC		I/O	PU/PD	YES	SMT	Hi-z	Hi-z
72	65	51	48	41	33	PC2		INT10				TSPI0CS0		T32A03 OUTA	T32A03 OUTC	PMD0 DBG	I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
73	66	52	49	42	34	PC3		INT03a				TSPI0RXD		T32A03 OUTB		PMD1 DBG	I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
74	67	53	50	43	-	PC4				UT1TXDA	UT1RXD	TSPI0TXD					I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
75	68	54	51	44	-	PC5				UT1RXD	UT1TXDA	TSPI0SCK					I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
76	69	55	52	-	-	PC6		INT02b				TSPI0CS1		T32A02 INA1	T32A02 INC1		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
77	70	56	53	-	-	PC7						TSPI0CSIN		T32A02 INB0			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
78	71	57	54	45	35	PB0							UO0				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
79	72	58	55	46	36	PB1							XO0				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
80	73	59	56	47	37	PB2							VO0				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
81	74	60	57	48	38	PB3							YO0				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
82	75	61	58	49	39	PB4							WO0				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
83	76	62	59	50	40	PB5							ZO0				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
84	77	63	60	51	41	PB6							EMG0				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
85	78	64	61	-	-	PB7							OVV0	PMD0 DBG			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
86	79	-	-	-	-	PT0					I2C0SDA		T32A00 INA0	T32A00 INC0			I/O	PU/PD	YES	SMT	Hi-z	Hi-z
87	80	-	-	-	-	PT1					I2C0SCL		T32A00 OUTA	T32A00 OUTC			I/O	PU/PD	YES	SMT	Hi-z	Hi-z
88	81	-	-	-	-	PT2							T32A00 INA1	T32A00 INC1			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
89	82	-	-	-	-	PT3							T32A00 INB0				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
90	83	-	-	-	-	PT4							T32A00 INB1				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
91	84	-	-	-	-	PT5							T32A00 OUTB				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
92	85	-	-	-	-	PT6				UT2RTS_N							I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
93	86	-	-	-	-	PT7				UT2CTS_N							I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
94	87	65	62	52	42	DVSSA											-	-	-	-	-	-
95	88	66	63	53	43	DVDD5A											-	-	-	-	-	-
96	89	-	-	-	-	PP0							T32A05 INB0				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
97	90	67	64	-	-	PD0		INT17b					T32A02 INB1				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
98	91	68	65	-	-	PD1		INT17a					T32A02 OUTB				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
99	92	69	66	-	-	PD2		INT03b		UT0CTS_N			T32A03 INA0	T32A03 INC0			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
100	93	70	67	-	-	PD3				UT0RTS_N	I2C1SDA		T32A03 INA1	T32A03 INC1	ENC2A		I/O	PU/PD	YES	SMT	Hi-z	Hi-z
101	94	71	68	-	-	PD4		INT18b			I2C1SCL		T32A03 INB0		ENC2B		I/O	PU/PD	YES	SMT	Hi-z	Hi-z
102	95	72	69	-	-	PD5		INT18a					T32A03 INB1		ENC2Z		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
103	96	73	70	54	-	PG0							T32A04 INA0	T32A04 INC0			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
104	97	74	71	55	-	PG1				TSPI1CS1			T32A04 INA1	T32A04 INC1			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
105	98	75	72	56	44	PG2	BOOT_N			TSPI1CS0			T32A04 OUTA	T32A04 OUTC			Output	PU/PD	N/A	SMT	Hi-z (Note1)	Hi-z
106	99	76	73	57	45	PG3		INT21		TSPI1CSIN			T32A04 OUTB				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z

Not Recommended for New Design

M4KQ LQFP144	M4KP LQFP128	M4KN QFP100	M4KN LQFP100	M4KM LQFP80	M4KL LQFP64	Pin Name	Combination Function A	Combination Function B	Combination Function C	Combination Function 1	Combination Function 2	Combination Function 3	Combination Function 4	Combination Function 5	Combination Function 6	Combination Function 7	Input/ Output	PU/PD	5V_T	SMT/ CMOS	Under Reset	After Reset
107	100	77	74	58	46	PG4				TSPI1RXD			T32A04 INB0				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
108	101	78	75	59	47	PG5				TSPI1TXD			T32A04 INB1				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
109	102	79	76	60	48	PG6				TSPI1SCK							I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
110	103	80	77	61	49	PE0				CANTX (Note3) (Note4)					UO1		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
111	104	81	78	62	50	PE1		INT04b		CANRX (Note3) (Note4)			T32A03 INA0	T32A03 INC0	XO1		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
112	105	82	79	63	51	PE2							T32A03 OUTA	T32A03 OUTC	VO1		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
113	106	83	80	64	52	PE3		INT04a					T32A03 INA1	T32A03 INC1	YO1		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
114	107	84	81	65	53	PE4		INT11a					T32A03 INB0		WO1		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
115	108	85	82	66	54	PE5		INT05a	INT11b				T32A03 INB1		ZO1		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
116	109	86	83	67	55	PE6		INT05b					T32A03 OUTB		EMG1		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
117	110	87	84	-	-	PE7									OVV1	PMD1 DBG	I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
118	111	-	-	-	-	PP1		INT19a					T32A05 INB1				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
119	112	-	-	-	-	PP2		INT19b					T32A05 OUTB				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
120	113	-	-	-	-	PP3							T32A01 INA0	T32A01 INC0	ENC0A		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
121	-	-	-	-	-	PR0							T32A05 INB0				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
122	-	-	-	-	-	PR1							T32A05 INB1				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
123	-	-	-	-	-	PR2							T32A05 OUTB				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
124	-	-	-	-	-	PR3				UT2RTS_N				ENC1A			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
125	-	-	-	-	-	PR4				UT2CTS_N				ENC1B			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
126	-	-	-	-	-	PR5							T32A01 INB0	ENC1Z			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
127	-	-	-	-	-	PR6							T32A01 INB1				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
128	-	-	-	-	-	PR7							T32A01 OUTB				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
129	114	88	85	68	56	DVDD5B											-	-	-	-	-	-
130	115	89	86	69	57	REGOUT2											-	-	-	-	-	-
131	116	90	87	70	58	REGOUT1											-	-	-	-	-	-
132	117	91	88	71	59	DVSSB											-	-	-	-	-	-
133	118	92	89	72	60	MODE											-	PD	-	SMT	-	-
134	119	93	90	73	61	PH0	X1	EHCLKIN									Input	PD	N/A	SMT	Hi-z	Hi-z
135	120	94	91	74	62	PH1	X2										Input	PD	N/A	SMT	Hi-z	Hi-z
136	121	95	92	75	63	RESET_N											-	PU	-	SMT	-	-
137	122	96	93	76	-	PF7				UT3RXD	UT3TXDA	NBDDATA1 (Note3)	T32A01 INB1			TRACE DATA1 (Note3)	I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
138	123	97	94	77	-	PF6				UT3TXDA	UT3RXD	NBDDATA0 (Note3)	T32A01 INB0			TRACE DATA0 (Note3)	I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
139	124	98	95	-	-	PF5		INT14b				NBDCLK	T32A01 INA1	T32A01 INC1	ENC1Z	TRACE CLK	I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
140	125	99	96	78	-	PF4		INT14a		UT3RXD	UT3TXDA	NBDSYNC (Note3)	T32A01 OUTA	T32A01 OUTC	ENC1B	TRST_N (Note3)	I/O	PU/PD	N/A	SMT	PU (Note2)	PU (Note2)
141	126	100	97	79	-	PF3				UT3TXDA	UT3RXD		T32A01 INA0	T32A01 INC0	ENC1A	TDI (Note3)	I/O	PU/PD	N/A	SMT	PU (Note2)	PU (Note2)
142	127	1	98	-	-	PF2		INT06b					T32A05 INA1	T32A05 INC1		TDO/ SWV	I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
143	128	2	99	80	64	PF1		INT06a		UT2RXD	UT2TXDA		T32A05 OUTA	T32A05 OUTC		TCK/ SWCLK (Note3) (Note4)	I/O	PU/PD	N/A	SMT	PD (Note2)	PD (Note2)
144	1	3	100	1	1	PF0				UT2TXDA	UT2RXD		T32A05 INA0	T32A05 INC0		TMS/ SWDIO (Note3) (Note4)	I/O	PU/PD	N/A	SMT	PU (Note2))	PU (Note2)

Note1: When RESET_N pin is "Low", built-in pull-up resistor is enabled.

Note2: The Initial value of built-in Pull-up/Pull-down resistor is effective.

Note3: CANTX/CANRX, TRST_N/TDI/TCK/TMS, TRACEDATA0/TRACEDATA1/TRACEDATA2/ TRACEDATA3, NBDDATA0/NBDDATA1/NBDDATA2/NBDDATA3/NBDSYNC are not available in M4KM.

Note4: CANTX/CANRX, TCK/TMS are not available in M4KL.

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Part Naming Conventions

TMP M4K Q F Y x UG

The identification of Toshiba microcontrollers

Revision

Package

Symbol	Package
QG	Plastic shrink quad outline non-leaded package; dry-packed
UG, DUG, FG, DFG	Plastic quad flat package; dry-packed
MG, DMG	Plastic small-outline package; dry-packed
XBG	Plastic ball grid array; dry-packed

Core

Symbol	Core
M4	Arm Cortex-M4 processor with FPU
M3	Arm Cortex-M3
M0	Arm Cortex-M0

Product Group

Family	Group	Application
TXZ	H	For General-purpose/Consumer electronic equipment
	K	For Motor/Inverter control industrial equipment(MCU+AMP/COMP)
	G	For OA/Digital equipment/industrial equipment
	E	For Robotics, Precision instruments control
	P	For Healthcare/ Battery equipment

ROM Size

Symbol	Size[KB]
M	32
P	48
S	64
U	96
W	128
Y	256
Z	384
D	512
E	768
10	1,023
15	1,536
20	2,048
40	4,096
80	8,192

Pin Count

Symbol		Pin count	Symbol		Pin count
0	G	Under 32pin	8	Q	129pin to 144pin
1	H	33pin to 44pin	9	R	145pin to 176pin
2	J	45pin to 48pin	A	S	177pin to 200pin
3	K	49pin to 52pin	B	T	201pin to 224pin
4	L	53pin to 64pin	C	U	225pin to 250pin
5	M	65pin to 80pin	D	V	251pin to 300pin
6	N	81pin to 100pin			
7	P	101pin to 128pin			

ROM Type

Symbol	Type
F	Flash
C	Mask

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