Smart Gate Driver Coupler Tips for Designing DESAT Detection Circuits

Description

This document summarizes some tips for designing peripheral circuits that should be noted when you use the $V_{CE(sat)}$ detection function of a smart gate driver coupler such as TLP5214 and TLP5214A .
The $V_{CE(sat)}$ detection (DESAT detection) circuit which detects the rise of the collector or drain voltage (V_{CE}) when an over-current flows into the power semiconductor switch device (hereinafter referred to 'power device') driven by the gate driver by causes, such as a short circuit of load, makes the power device turn off, and protects it. However, the V_{CE} may rise unusually and largely due to the inductances of the loads when the power device switches, and if it enters the DESAT terminal, an erroneous detection of the DESAT detection circuit may occur. In three-phase inverters and other inverters, noise generated during switching of other phases may cause an erroneous detection of the DESAT detection circuit due to noise circulating through power supply lines and GND lines or electromagnetic induction between wires.
This document provides tips to reduce the likelihood of DESAT false detections.

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1. DESAT Detection Circuit

At first, following is the brief review of the DESAT detection circuit.
The DESAT detection function built in a smart gate driver (SGD) coupler such as TLP5214 or TLP5214A is designed to protect the power device (IGBT, Si or SiC-MOSFET, and GaN-FET, but the IGBT will be exemplified in the following explanation) from excessive currents such as load-shorting current, which may cause breakdown.
The DESAT detection circuit detects the voltage at the collector or drain of the power device to be driven through the DESAT terminal. When the voltage exceeds the specified voltage(V_{DESAT}), the SGD coupler stops the power device and outputs a fault signal from the FAULT_N terminal.

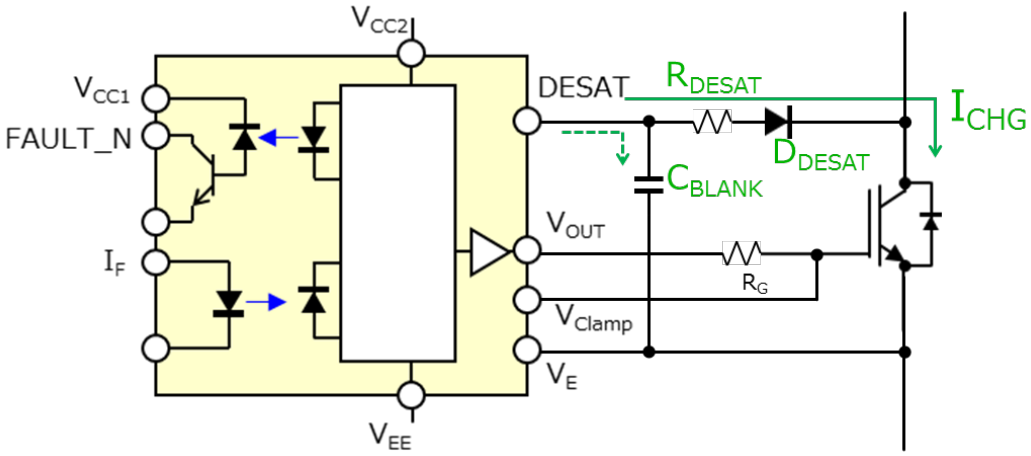

Figure 1.1 Gate Driver Circuit with DESAT Detection Function

In this example shown in Figure 1.1, the IGBT is driven by the TLP5214A. When the IGBT to be driven is on (V_{OUT} is H), I_{CHG} is flowing out of the DESAT terminal, and the C_{BLANK} connected to the DESAT terminal and the V_E terminal is about to be charged. However, since the IGBT is ON, the V_{CE} is saturated, and the I_{CHG} flows into the IGBT through the R_{DESAT} and D_{DESAT}, so the C_{BLANK} is not charged to the DESAT threshold voltage V_{DESAT}.
If the V_{CE} of the IGBT rises due to an overcurrent caused by a load short circuit or the like, the I_{CHG} cannot flow into the IGBT, and the C_{BLANK} starts to be charged. If the DESAT terminal exceeds the threshold voltage V_{DESAT}, the SGD determines that IGBT's desaturation(DESAT) status has been detected (excessive current has flowed), and V_{OUT} shifts soft shutdown mode to turn off the IGBT. FAULT_N signals are also outputted to the controller.
t_{BLANK} time since C_{BLANK} begins to be charged, until protected operation starts is calculated from the saturated voltage $V_{CE(sat)}$ of the IGBT and the forward voltage V_F of the D_{DESAT} and the voltage drop of the R_{DESAT}.

$$t_{BLANK} = \{ C_{BLANK} \times (V_{DESAT} - (V_F + I_{CHG} \times R_{DESAT})) \} / I_{CHG} \quad \cdots\cdots\cdots\cdots\cdots \text{(Equation 1)}$$

This 't_{BLANK}' must be shorter than the short circuit withstand time(t_{sc}) of the IGBT.
See "Smart Gate Driver Coupler TLP5214A/TLP5214 Application Note -Advanced edition-" Section 4.2 'Setting and adjusting blanking times' for t_{BLANK}.

We will present the subject matter in the next chapter.

2. Noise intrusion path

The power device may be installed several cm to several tens of cm away from the SGD because it is a module, or if it is a single unit, it may be equipped with a radiator, or it may be connected with a thick wiring to allow a large load current to flow. Therefore, the length of the three wires(DESAT detection, gate-drive, and emitter-common) from the SGD is required. So, the wiring itself may act as an antenna and cause electromagnetic induction from the wiring with a large load current, or if there are multiple phases in inverter applications, electromagnetic induction from the load current due to switching of other phases, or noise may be introduced from gate-drive signals of other phases through the parasitic capacitance between the wiring pattern, etc. The image is shown in Figure 2.1.

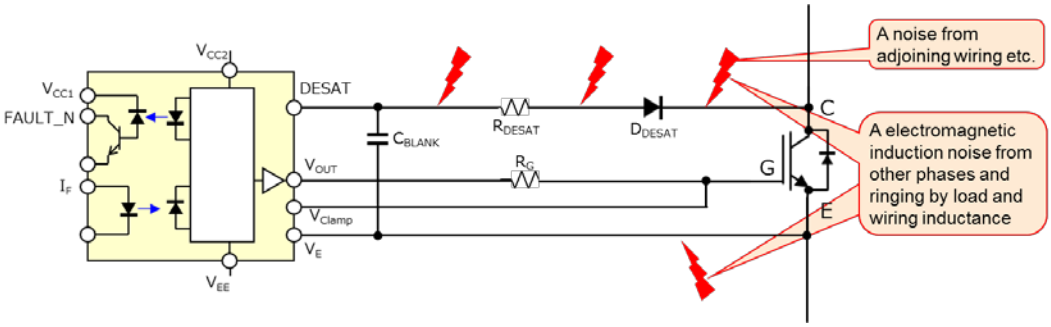

Figure 2.1 Noise Intrusion Image

On printed circuit boards, the voltage signal transmitted by wiring influences between adjacent wirings due to parasitic capacitance, etc., and the current signal flowing between adjacent wirings influences by electromagnetic induction. In particular, the current controlled by the IGBT is as large as several amperes to several hundred amperes, so a large induced magnetic field is generated. In IGBT gate-drive wirings, a peak current of several amperes or more flows to rapidly charge the gate capacitance, which may have a large effect on the surrounding area. Again, parasitic resistance, inductance, and capacitance components are always present in the wiring. For example, a change in the current flowing through the wiring causes a localized change in the voltage due to the resistance and inductance components, and a change in the voltage causes a charge and discharge of the capacitance components, resulting in a change in the current. As described above, not only signals but also voltage changes generated by parasitic components are mutually introduced as voltage noise through parasitic capacitance between wirings, and changes in current are mutually intertwined in a complicated manner as current and voltage noise by electromagnetic induction between parallel wirings.
The wiring of the DESAT detection circuit is wired on the board of the above-mentioned environments, and the circuit impedances are relatively high. Therefore, the wiring around the DESAT detection circuit wiring is susceptible to the influence of the wiring, which may lead to erroneous detection of the DESAT.

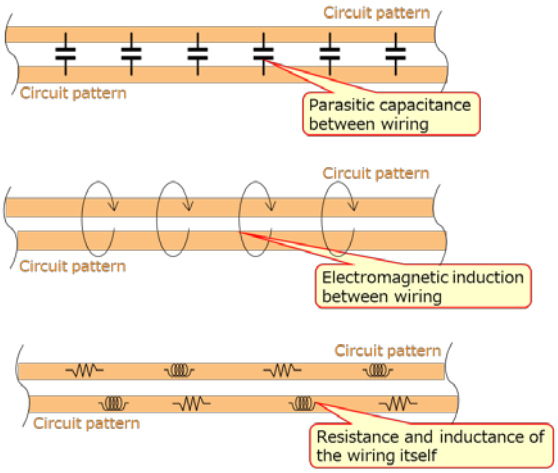

Figure 2.2 Image of Parasitic Elements in Wiring Pattern

3. Tips on circuit wiring pattern design

In order to reduce the malfunction of DESAT detections due to noises around the wiring described above, the following points should be noted on the wiring patterns. DESAT-pin is more impedances than other wiring and is more susceptible to inductions and entering from other wiring. Therefore, the wiring should not be adjacent to the wiring through which current pulses flow or to the wiring tied to nodes where large potential fluctuations occur.

(1) The wiring for DESAT detection is not brought close to the DESAT detection wiring of the other power devices connected to the collectors (drains) of the power devices having the highest voltage fluctuations.
(2) The wiring for DESAT detection does not run parallel to the gate drive wiring of the IGBT through which the current pulses flow.
(3) The R_{DESAT}, D_{DESAT}, and C_{BLANK} should be placed near the SGD so that the low-pass filtering effects of the R_{DESAT}, D_{DESAT}, and C_{BLANK} can be maximized. (The effect of the filter will be described later.)

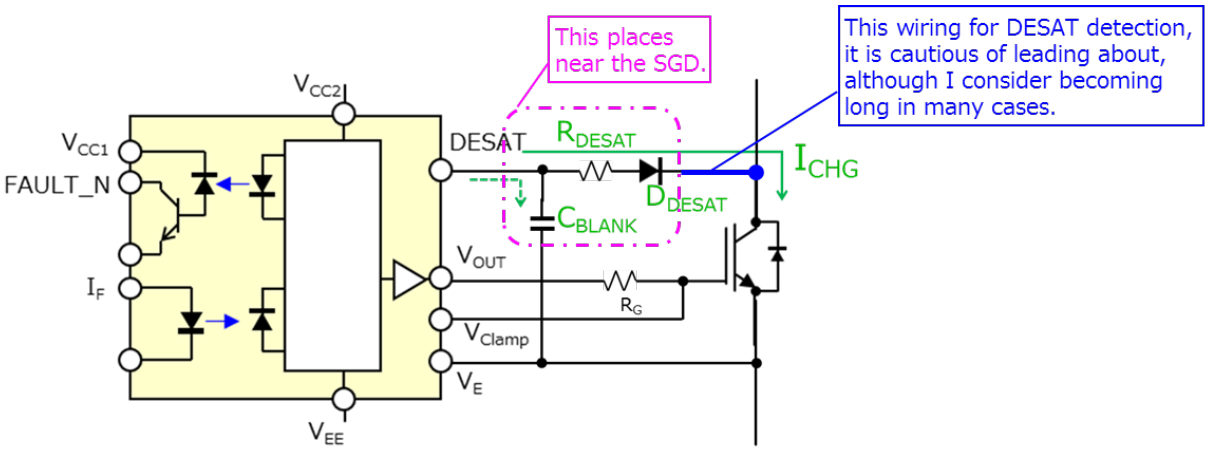

Figure 3.1 Notes on Wiring Routing

If feasible, in order to protect the wiring for DESAT detection from noises so as not to cause a DESAT detection malfunction, it may be effective to surround the right and left sides of the wiring with the common potential (V_E or V_{EE}) of the SGD in parallel with the multilayered wiring layers or the wiring for DESAT detection. Note that this is not the system's GND potential, but the common potential of the SGD itself, which is the criterion for DESAT detection. The DESAT detection operates with the V_E pin connected to the emitters (sources) of the power device as the reference potential. Therefore, it is meaningless if the wiring for DESAT detection is shielded by the common potential of the SGD itself. System GNDs are one of the biggest sources of noise, particularly when driving Upper-Side power devices in inverter applications.

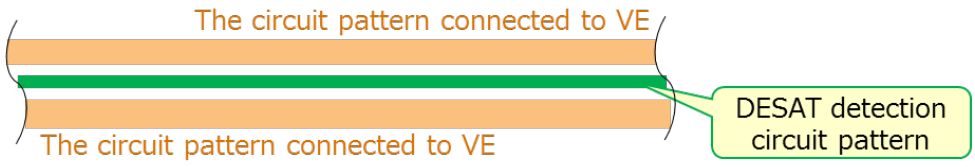

Figure 3.2 Shielding Image of DESAT Circuit Wiring Patterns

4. Tips for determining the constants of DESAT detection circuits

This section presents tips on the C_{BLANK} and R_{DESAT} values of the DESAT detection circuit and how to select the D_{DESAT}.

The blanking time t_{BLANK} based on the short circuit withstand time of the power device is described in detail in Section 4 of the "Smart Gate Driver Coupler TLP5214A/TLP5214 Application Note –Advanced edition-". For details, let us say that the time t_{BLANK} (Equation 1 on page 3) from the time when the IGBT V_{CE} rises due to excessive current flowing, the I_{CHG} stops flowing to the IGBT, and the C_{BLANK} begins to charge until the DESAT terminal exceeds the V_{DESAT} is set to be shorter than the short circuit withstand time.

From the point of view of protecting the IGBT, t_{BLANK} should be shorter. However, even if attention is paid to the layout of components and wiring patterns as described above, C_{BLANK} may be charged by large noises and DESAT-pin voltage exceed the V_{DESAT}, and a malfunction may occur in the FAULT state. Because, it is for that the input impedance of the DESAT-pin is high when the LED for driving signals are on. Then, a low-pass filter is formed using the C_{BLANK}, R_{DESAT}, and D_{DESAT} to prevent it.

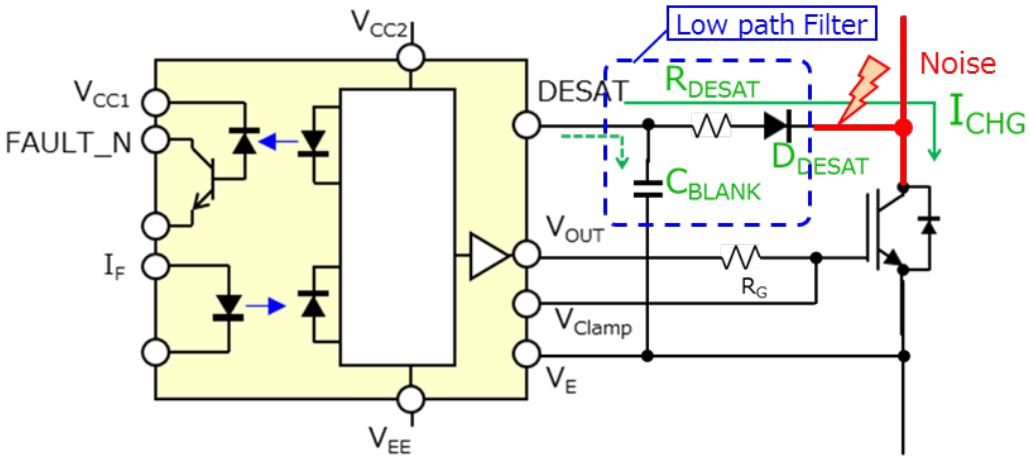

Figure 4.1 Noise Reduction by the Filter

Consider the constants of each device from the viewpoint of the low-pass filter configuration. The larger the C_{BLANK} and R_{DESAT}, the smaller the junction capacitance of the D_{DESAT}, the more effective the filter becomes.

1. D_{DESAT}: A diode with a small current-capacity (about 100mA) is sufficient because the only forward current flowing is the I_{CHG}. You should use a diode with a reverse breakdown voltage sufficiently approximately twice or more higher than the power supply voltage of the IGBT. And you should use a diode with a smaller junction capacitance to prevent DESAT malfunction. Also, it is also effective to use two or more diodes in series. When the diodes are connected in series, the junction capacitance is reduced by a factor of the number of the diodes connected in series, which is effective from the viewpoint of reducing the junction capacitance. However, a reverse breakdown voltage of the diodes should be higher than the power supply voltage of the IGBT. Because the reverse breakdown voltage applied when the IGBT is off may not be applied uniformly to the diodes in series due to variations in leakage current among the diodes. This is related also to calculation of the IGBT short detection threshold voltage($V_{th(IGBT)}$). See "Smart Gate Driver Coupler TLP5214A/TLP5214 Application Note –Advanced edition- " Section 4.5 'Modifying the IGBT short detection threshold voltage'.
2. C_{BLANK}: For example, t_{BLANK} is set to 5μs. Since I_{CHG} is 250μA in TLP5214 or TLP5214A, C_{BLANK} will choose about 200 pF from the Equation 1 on page 3. If the C_{BLANK} is 200pF and the junction capacitance of the D_{DESAT} is 20pF and noise of 100Vp-p is generated in the V_{CE}, the peak voltage of C_{BLANK} is calculated by the voltage division of capacitances.

$$100V \times 20pF / (200pF + 20pF) = 9.1V$$

This noise voltage exceeds the V_{DESAT}(= 6.5V), and may causes malfunction of the FAULT. Therefore, from the viewpoint of capacitance, C_{BLANK} is increased, or a diode with a smaller junction capacitance is chosen as the D_{DESAT}. If smaller diodes are not available, you use the C_{BLANK} with larger capacitance. When 470pF is used as an example, even if the junction capacitance of the D_{DESAT} is 20pF and noise of 100Vp-p is generated in the V_{CE}, the noise voltage applied to C_{BLANK} is reduced as follows.

$$100V \times 20pF / (470pF + 20pF) = 4.1V$$

However, at 470pF, the t_{BLANK} exceeds 5μs, so be careful not to exceed the short circuit withstand time of the IGBT. If the t_{BLANK} needs to be shortened when the C_{BLANK} is increased, the charge current of the C_{BLANK} can be increased by adding an R_B and the I_B is added to I_{CHG}. When connecting a Zener diode or a Schottky barrier diode as shown in Figure 4.2 to protect the DESAT terminal, the components have junction capacitances and are added to the C_{BLANK} as parallel capacitances. The t_{BLANK} must be calculated in addition to the C_{BLANK}. You consider when designing. See "Smart Gate Driver Coupler TLP5214A/TLP5214 Application Note –Advanced edition- " Section 4.4 'Setting the time using an external blanking circuit (R_B)' for R_B calculation.

3. R_{DESAT}: Considering a low-pass filter for noise reduction, if the time constants of the R_{DESAT} and C_{BLANK} are increased, the filter effect for high frequency noise increases for impulses and ringing noise, and false DESAT detection can be decreased. When the IGBT is on, the I_{CHG} flows through the R_{DESAT}, so that the voltage drop increases by the increase of the R_{DESAT}. If an R_B is added, care must be taken because the I_B and the I_{CHG} flow through the R_{DESAT} and the voltage drop is increased. The adjustment of $V_{th(IGBT)}$ must be taken into account.

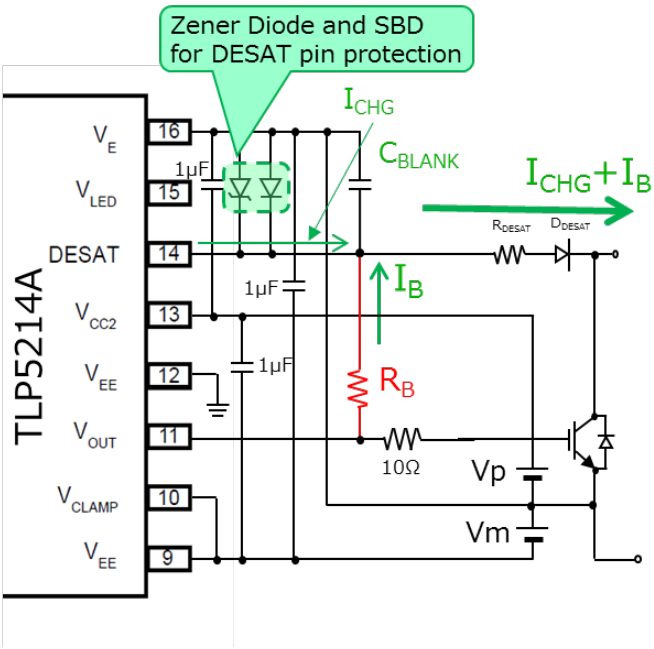

Figure 4.2 Protective Devices and R_B

As described above, the constants of the devices influence each other, and the parasitic devices (inter-wiring capacitance, wiring inductance, wiring resistance) of the printed circuit board are also intertwined complicatedly. Refer to the "Tips" in this document to verify the design adequately.
Observation of the gate-voltage waveform of the IGBT and observation of the waveform of the DESAT terminal cannot be accurately observed using the system GND. Please use an optically isolated differential probe with high CMRR(Common Mode Rejection Ratio) even at high frequencies (80dB or more is recommended).

For reference, I_B and the constants of the DESAT detection system are calculated.
The voltage chart for DESAT detection is shown in Figure 4.3. The voltage concerning C_{BLANK} in case IGBT is ON state, i.e., the voltage drop of D_{DESAT} and R_{DESAT} and the saturation voltage $V_{CE\ (sat)}$ of IGBT, is defined as $V_{CBLK\ (ON)}$. Therefore, the following formula is realized.

$$V_{DESAT} = V_{th(IGBT)} + V_{CBLK(ON)}$$

$V_{CBLK(ON)}$ is decided and calculation is begun. If $V_{th(IGBT)}$ is decided first, please calculate $V_{CBLK(ON)}$ using the following formulas.

$$V_{CBLK(ON)} = V_{DESAT} - V_{th(IGBT)}$$

- Calculation condition (It is calculation in case V_{OUT} is H, i.e., IGBT is ON state.)
  (a) The voltage drop between the V_{CC2} and the V_{OUT} is approximated as zero because the voltage drop is in the very small current range.
  (b) The $V_{CE(sat)}$ of the IGBT is assumed to be 1.8V.
  (c) The V_F of the DESAT diodes (D_{DESAT}) is assumed to be 0.7V.
  (d) The C_{BLANK} is 1500pF to reduce malfunction due to noises.
  (e) The short circuit withstand time of the IGBT is set to 10μs, and the margins are set to 7μs.
  (f) The $V_{CBLK(ON)}$ is 3.0V.
  (g) Supply voltage of SDG is Vp = Vm = 15V.

Calculation based on the above conditions.

$$t_{BLANK} = 7\mu s = \{ C_{BLANK} \times V_{th(IGBT)} \} / (I_{CHG} + I_B)$$
$$= \{ C_{BLANK} \times (V_{DESAT} - V_{CBLK(ON)}) \} / (I_{CHG} + I_B)$$
$$= \{ 1500pF \times (6.5V - 3.0V) \} / (250\mu A + I_B)$$

From the above, I_B = 500μA can be obtained. If we further calculate the R_B,

$$R_B = (Vp - V_{CBLK(ON)}) / I_B = (15V - 3.0V) / 500\mu A = 24k\Omega$$

Since the $V_{CBLK(ON)}$ is 3.0V,

$$V_{CBLK(ON)} = V_{CE(SAT)} + V_{F(DDESAT)} + R_{DESAT} \times (I_B + I_{CHG})$$
$$3.0V = 1.8V + 0.7V + R_{DESAT} \times (500\mu A + 250\mu A)$$

Therefore, the R_{DESAT} is 667Ω.

The time constants of the low-pass filter with R_{DESAT} and C_{BLANK} are 667Ω × 1500pF = 1μs.
In the examples, the $V_{CBLK(ON)}$ was set to 3.0V, but note that increasing the $V_{CBLK(ON)}$ decreases the potential difference(=$V_{th(IGBT)}$) with respect to the V_{DESAT} and reduces the noise margins. If a short circuit is detected immediately after turning on the LED for signals, it is necessary to consider not only the t_{BLANK} calculated in the examples but also the time required for the $t_{DESAT(LEB)}$ and the time required for the DESAT terminal to change from the V_E potential to the $V_{CBLK(ON)}$. It is recommended that the $V_{CBLK(ON)}$ be set lower.
For reference, the timing chart for DESAT detection is shown Figure 4.4.

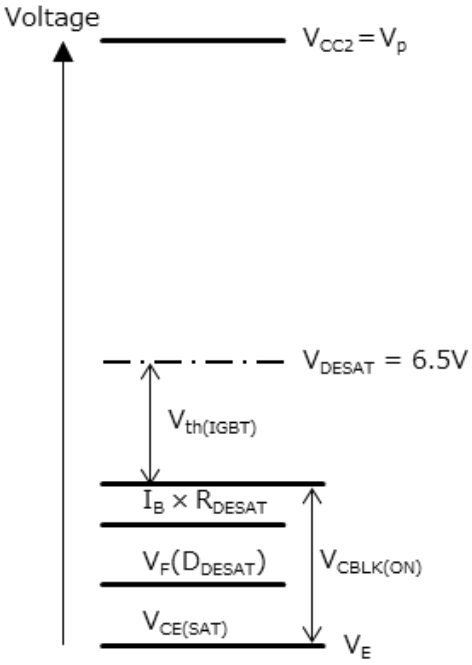

Figure 4.3 Voltage Chart for DESAT Detection

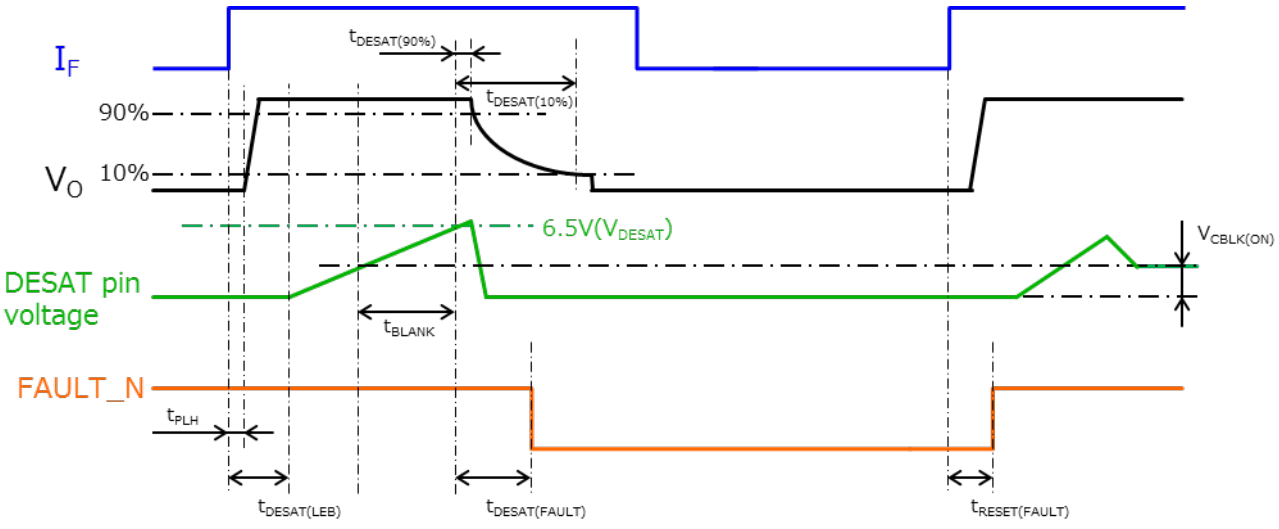

Figure 4.4 Timing Chart for DESAT Detection

Revision history

Version	Date	Details
Rev.1.0	2019-06-28	Created

Notes on Contents

1. **Block Diagrams**
   Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. **Equivalent Circuits**
   The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. **Example computation of circuit constants**
   Numerical values in the text are provided as an example in order to explain the circuit in an easy-to-understand manner. It is not guaranteed to operate with the values stated.

Usage Considerations

Notes on Handling of Products

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The usage beyond absolute maximum rating, the mistaken wiring, the unusual pulse noise etc. which are induced from wiring or load are the cause, and may destroy IC. As the result, it may result in emitting smoke and ignition because high current continues flowing into IC. In order to make influence into the minimum, a proper setup of the capacity of a fuse, pre-arcing time, an insertion circuit position, etc. is needed supposing inflow and an outflow of the high current in destruction.

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