

Load Transient Response of LDO and Methods to Improve it

Outline:

This document explains the operation principle of the load transient response* of the low drop out regulator (LDO) and how to improve the load transient response.

It also explains the effect of the external phase compensation capacitance (CFB) on the variable voltage type.

*: Load transient response: Behavior in which an attempt is made to keep the output voltage constant when the load current (output current) changes suddenly

Table of Contents

Table of Contents	1
1. Introduction	3
2. Importance of an LDO's load transient response	4
2.1. Overview of an LDO's load transient response and its impact on semiconductor devices	4
2.2. Mechanism of load transient response of LDOs	5
2.2.1. Mechanism of load transient response in the event of a sudden load increase.....	5
2.2.2. Mechanism of load transient response in the event of a sudden load decrease.....	8
3. Improving the load transient response of LDOs.....	10
3.1. Using an output capacitor (C_{OUT}) to improve load transient response.....	10
3.2. Using an external phase compensation capacitor (C_{FB}) to improve the load transient response of adjustable-output LDOs.....	12
4. Summary of load transient response improvement.....	13
4.1. Dual-power-supply LDO with an NMOS pass device: Load transient response of the TCR5BM, TCR8BM, and TCR15AG	13
4.1.1. Load transient response of dual-power-supply LDOs with an NMOS pass device.....	13
4.2. Load transient response waveform of the TCR5BM and TCR15AG dual-power-supply LDO series.....	14
4.2.1. Load transient response waveform of the TCR5BM12 500-mA dual-power-supply LDO	14
4.2.2. Load transient response waveform of the TCR15AGADJ 1.5-A dual-power-supply LDO	14
5. Conclusion	16
6. Related Links.....	17
7. RESTRICTIONS ON PRODUCT USE.....	18

1. Introduction

Various semiconductor (electronic) components are used to enhance the performance and functionality of increasingly sophisticated mobile devices and other electronic devices.

Since these semiconductor devices operate at different supply voltages, mobile devices and other devices incorporate several LDOs to generate different voltages from a single battery voltage. To operate at high speed, high-performance semiconductor devices sometimes require a large current, which is subject to considerable changes in a very short period of time. Even in the presence of sudden changes in load current, LDOs must maintain a regulated voltage so as to ensure these semiconductor devices work properly.

The ability of an LDO to maintain a regulated output voltage in response to sudden changes in load current is called load transient response. Nowadays, there is a stringent requirement for load transient response. It is one of the most important parameters for LDOs. This application note discusses the mechanism of load transient response of LDOs and how to improve the transient performance using an external component. This knowledge will be helpful in designing high-performance electronic devices.

2. Importance of an LDO's load transient response

2.1. Overview of an LDO's load transient response and its impact on semiconductor devices

Figure 2.1.1 shows a simplified diagram of a typical LDO with a PMOS pass device. Figure 2.1.2 gives an example of an output voltage waveform in response to changes in load current.

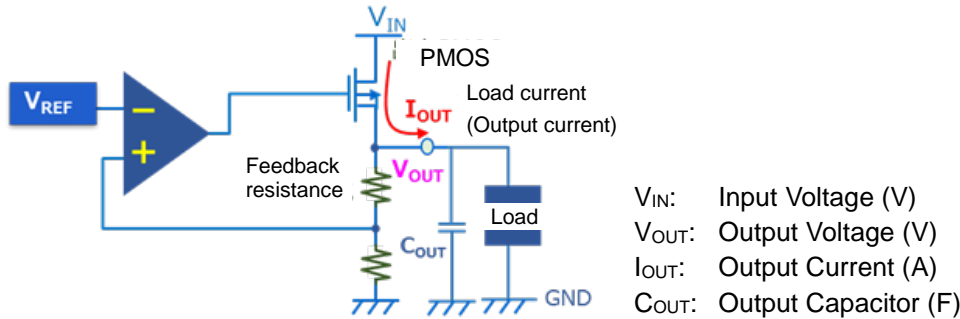


Figure 2.1.1 Simplified diagram of a typical LDO with a PMOS pass device

For example, if an LDO's load (such as an electronic device) suddenly transitions from high-speed operation to an inactive state or vice versa, its operating current changes rapidly, causing a step change in the LDO's load current. An LDO should ideally maintain its output voltage (V_{OUT}) even in the presence of fast load changes. In reality, however, the output voltage (V_{OUT}) of an LDO is subject to slight fluctuations because it cannot respond instantaneously to a transient condition. There is some inherent delay due to the limit of the operating speed (transfer function) of an LDO's internal circuitry. In the event of load changes, the negative feedback loop of an LDO brings its output (V_{OUT}) back to the steady-state voltage after this delay time. Figure 2.1.2 shows a typical load transient response of an LDO (i.e., the response of an LDO to a load transient).

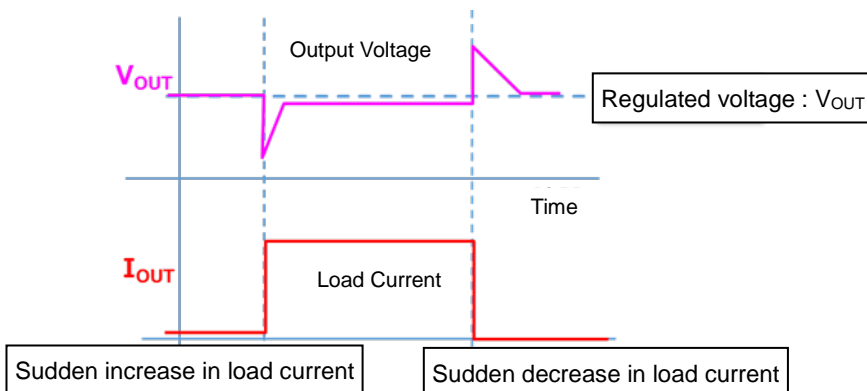


Figure 2.1.2 Example of an output voltage waveform in response to changes in load current

- Sudden increase in load current: The output voltage (V_{OUT}) drops instantaneously and then returns to the steady-state value via negative feedback.
 - Sudden decrease in load current: The output voltage (V_{OUT}) rises instantaneously and then returns to the steady-state value via negative feedback.
- * In reality, the output voltage is subject to a slight change, depending on the steady-state

value of load current. (This is defined as load regulation.)

Because electronic devices operate at low voltage, they are sensitive to supply voltage variations. Although an LDO regulates its output voltage in response to sudden changes in load current, even slight output voltage transients could cause electronic devices to fail or malfunction. Take, for example, an electronic device operating at 1 V. Even a 0.1-V transient variation in an LDO’s output voltage could cause it to fail, leading to a system failure. It is therefore necessary to minimize variations in an LDO’s output voltage.

The following sections discuss the load transient response of an LDO and how to reduce variations in its output voltage (i.e., improve its load transient response).

2.2. Mechanism of load transient response of LDOs

The following subsections describe the operation of an LDO in response to sudden changes in the operating current of the load (e.g., an electronic device) connected to the LDO output (V_{OUT}). Here, the assumption is that no output capacitor (C_{OUT}) is connected to the LDO.

2.2.1. Mechanism of load transient response in the event of a sudden load increase

- Why does a sudden increase in load current cause an LDO’s output voltage to sag?
- First, let’s consider a sudden increase in load current (see Figure 2.2.1 to Figure 2.2.3).

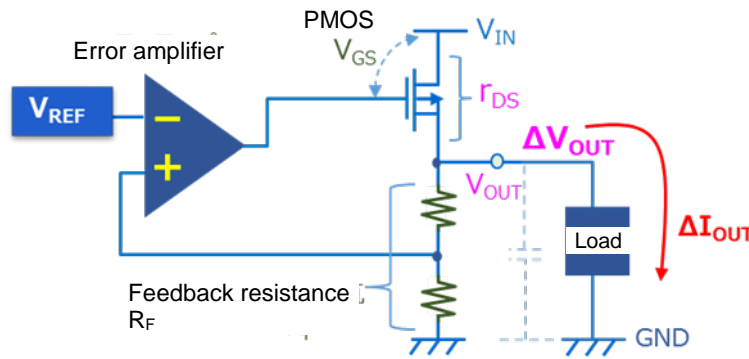


Figure 2.2.1 Simplified diagram of a typical LDO with a PMOS pass device

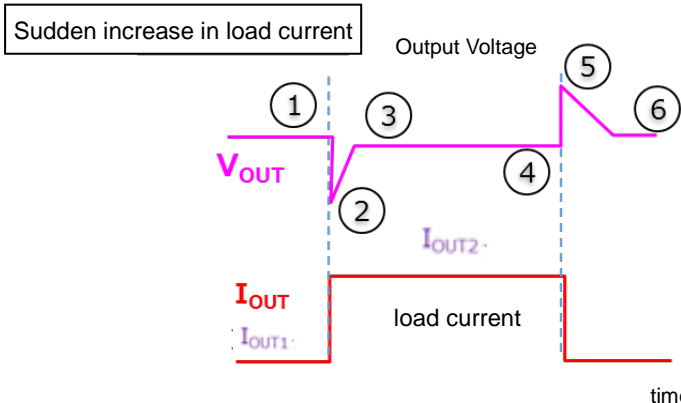


Figure 2.2.2 Load transient response waveform

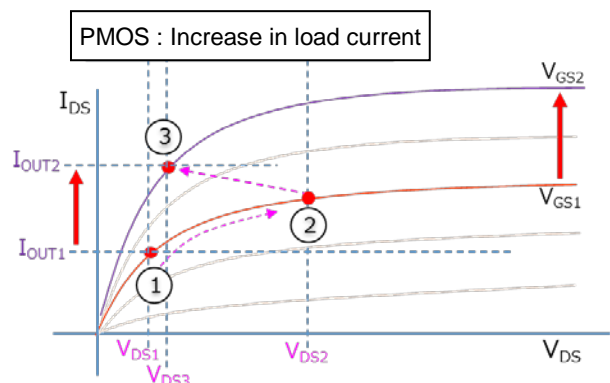


Figure 2.2.3 V_{DS} - I_{DS} curves of the PMOS pass

device

Suppose that the LDO's load current is constant at I_{OUT1} and that the LDO's output voltage (V_{OUT}) is properly regulated (#1). Let the drain-source and gate-source voltages of the PMOS pass device at #1 be V_{DS1} and V_{GS1} , respectively. When the load current suddenly steps from I_{OUT1} to I_{OUT2} , the LDO's output voltage sags considerably (#2) because its negative feedback loop cannot track the change in load current instantaneously. This situation is equivalent to increasing the drain-source voltage of the PMOS pass device from V_{DS1} to V_{DS2} to accommodate the increased load current (I_{OUT2}) while keeping its gate-source voltage at V_{GS1} . V_{DS2} is determined by the combined impedance of the load impedance, the feedback resistor value (R_F), and the output resistance of the PMOS pass device as well as a change in load current (ΔI_{OUT}), as described below. While the drain-source voltage (V_{DS}) of the PMOS pass device changes, the LDO's negative feedback loop begins tracking the load change. As a result, the gate-source voltage of the PMOS pass device increases from V_{GS1} to V_{GS2} to accommodate the increased output current (I_{OUT2}). Once the LDO's output current equals I_{OUT2} , the output voltage stops decreasing, bringing V_{DS2} to V_{DS3} (that is slightly lower than V_{DS1}) via negative feedback. In other words, the output voltage (V_{OUT}) returns almost to the initial voltage (#3).

* Even when the LDO returns to the steady state, the output voltage is slightly lower than the initial voltage (by $V_{DS3} - V_{DS1}$) because the load current has increased from I_{OUT1} to I_{OUT2} .

■ How much does the output voltage sag?

How much does the output voltage sag when the load current suddenly increases? When the load current increases suddenly in a very short period of time, the negative feedback loop cannot track its change instantaneously and thus has no effect on reducing the LDO's output impedance (Z_{OUT}). Therefore, Z_{OUT} is expressed as follows (see Figure 2.2.4).

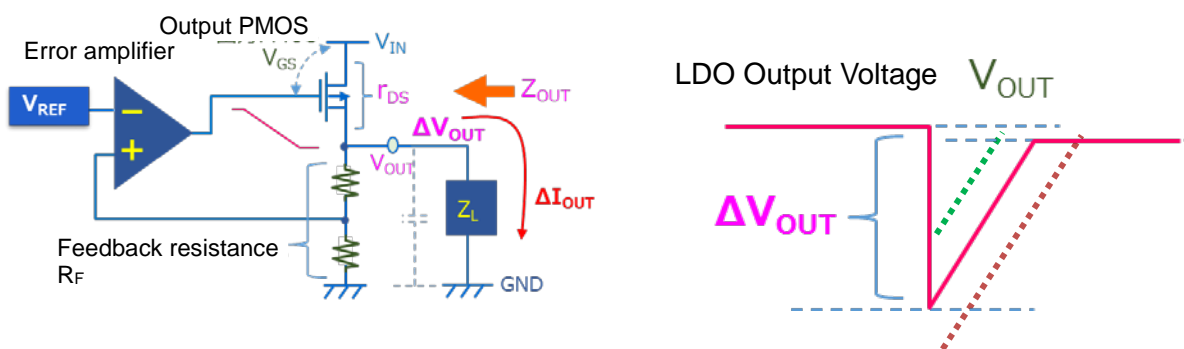


Figure 2.2.4 Example of an LDO's output voltage waveform in response to a sudden increase in load current

$$Z_{OUT} = r_{DS} // R_F // Z_L$$

This represents the combined impedance of a parallel circuit consisting of the output resistance of the PMOS pass device (r_{DS}), the feedback resistor (R_F), and the load impedance (Z_L). Let the increase in load current be ΔI_{OUT} and the resulting change in the output voltage be ΔV_{OUT} . When the

load current increases by ΔI_{OUT} in such a short period of time that the LDO's negative feedback loop cannot track its change instantaneously, the resulting output voltage sag (ΔV_{OUTMAX}) is basically expressed as:

$$\Delta V_{OUTMAX} = (r_{DS} // R_F // Z_L) \cdot \Delta I_{OUT}$$

At this time, an error amplifier provides an error voltage proportional to the output voltage sag. When driven by the error voltage signal, the PMOS pass device accommodates the increased load current, causing the output voltage to stop decreasing. However, it takes some time for the output voltage of the error amplifier to change because of an internal phase compensation capacitor and the gate capacitance of the PMOS pass device. This voltage slope is called the slew rate of the error amplifier. An error amplifier with a fast slew rate (i.e., an error amplifier whose output voltage changes rapidly) can stop the LDO's output voltage from decreasing before it sags by as much as ΔV_{OUTMAX} . However, if it takes a long time for the PMOS pass device to accommodate the increased load current (i.e., the error amplifier has a slow slew rate), the LDO's output voltage sags by ΔV_{OUTMAX} . As described above, the ability of an LDO to respond to sudden load changes (i.e., load transient response) is crucial to maintain a regulated output voltage.

2.2.2. Mechanism of load transient response in the event of a sudden load decrease

- Why does a sudden decrease in load current cause the output voltage to rise?

Next, let's consider a sudden decrease in load current (see Figure 2.2.5 and Figure 2.2.6).

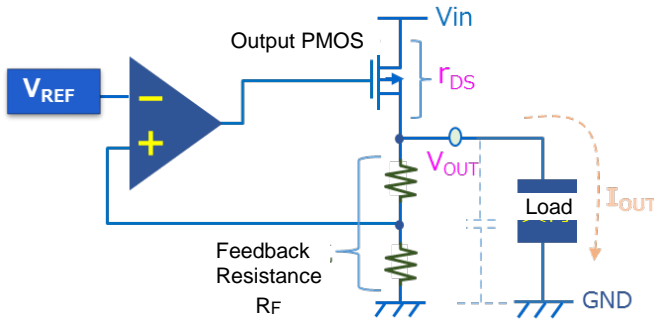


Figure 2.2.5 Simplified diagram of a typical LDO with a PMOS pass device

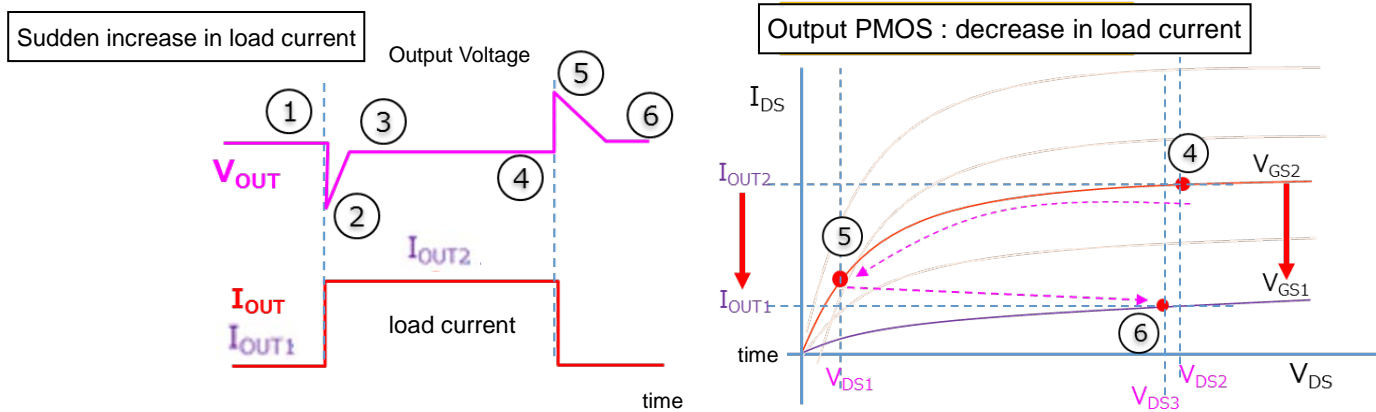


Figure 2.2.6 Load transient response waveform and V_{DS} - I_{DS} curves of the PMOS pass device

Suppose that the LDO's load current is constant at I_{OUT2} and that the LDO's output voltage (V_{OUT}) is properly regulated (#4). Let the drain-source and gate-source voltages of the PMOS pass device at #4 be V_{DS2} and V_{GS2} , respectively. When the load current suddenly steps from I_{OUT2} to I_{OUT1} , the LDO's output voltage rises considerably (#5) because its negative feedback loop cannot track the change in load current instantaneously. This situation is equivalent to decreasing the drain-source voltage of the PMOS pass device from V_{DS2} to V_{DS1} to accommodate the decreased load current (I_{OUT1}) while keeping its gate-source voltage at V_{GS2} . As is the case with a sudden load increase, V_{DS1} is determined by the combined impedance of the load impedance, the feedback resistor value (R_F), and the output resistance of the PMOS pass device as well as a change in load current (ΔI_{OUT}).

- How much does the output voltage rise?

While the drain-source voltage (V_{DS}) of the PMOS pass device changes, the LDO's negative feedback loop begins tracking the load change. As a result, the gate-source voltage of the PMOS pass device decreases from V_{GS2} to V_{GS1} to accommodate the decreased output current (I_{OUT1}). Once the LDO's output current equals I_{OUT1} , the output voltage stops increasing, bringing V_{DS1} to V_{DS3} (that is slightly higher than V_{DS2}). In other words, the output voltage (V_{OUT}) returns almost to the initial voltage (#6).

* Even when the LDO returns to the steady state, the output voltage is slightly higher than the initial voltage (by $V_{DS2} - V_{DS3}$) because the load current has decreased from I_{OUT2} to I_{OUT1} .

As is the case with a sudden load increase, an increase in an LDO's output voltage due to a sudden load decrease is determined by the output impedance (Z_{OUT}) and the output current change (ΔI_{OUT}) during the inherent delay in which the negative feedback loop cannot track ΔI_{OUT} . Likewise, an LDO's negative feedback loop causes a delay dependent on the slew rate of an error amplifier, which lasts until the output current from the PMOS pass device matches the decreased load current.

When an LDO's negative feedback loop cannot track a fast load change, the resulting maximum output voltage change is determined by a change in load current and the output impedance (Z_{OUT}) during the inherent delay in which the LDO's negative feedback cannot track the load change. Without an output capacitor (C_{OUT}), an LDO generally has a large output impedance (Z_{OUT}). Therefore, even a slight load change results in a considerable change in an LDO's output voltage, which could reach even the GND or power supply voltage. Adding an output capacitor (C_{OUT}) is very effective in preventing this situation and thus improving load transient response. The next section describes the effect of an output capacitor (C_{OUT}) on improving load transient response.

3. Improving the load transient response of LDOs

3.1. Using an output capacitor (C_{OUT}) to improve load transient response

As described above, an LDO exhibits extremely poor load transient response without an output capacitor (C_{OUT}), causing its output voltage to vary considerably. This is because the output voltage variation of an LDO is equal to a change in load current multiplied by a large open-loop output impedance of the LDO. Therefore, the output voltage variation of an LDO due to sudden load changes can be reduced by reducing its output impedance. Adding an output capacitor (C_{OUT}) to the output of an LDO is effective for this purpose. This subsection describes the effect of an output capacitor (C_{OUT}).

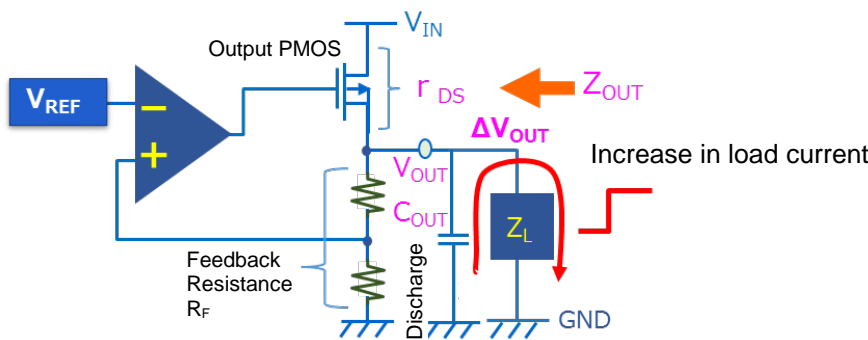


Figure 3.1.1 Load transient response in the event of a sudden load increase when an LDO has an output capacitor (C_{OUT})

Suppose that the load current (I_{OUT}) increases suddenly as shown in Figure 3.1.1. In the discussion of the previous section, the increased load current is supplied only by the PMOS pass device. In contrast, when an output capacitor (C_{OUT}) is connected to an LDO, the increased load current is supplied from the output capacitor (C_{OUT}) during the inherent delay before the current through the PMOS pass device is adjusted through the LDO’s negative feedback loop. As a result, the output capacitor (C_{OUT}) is discharged by the load current. Therefore, the output voltage (V_{OUT}) sag is determined by the value of the output capacitor (C_{OUT}) and a change in load current. This is described in the following paragraphs.

When an output capacitor (C_{OUT}) is connected to an LDO, its output impedance (Z_{OUT}) is expressed as:

$$Z_{OUT} = r_{DS} // R_F // Z_L // Z_{COUT}$$

where, Z_{COUT} is the impedance of the output capacitor, including its equivalent series resistance (R_{ESR}). Suppose that the load impedance and the value of the feedback resistor (R_F) in the LDO are higher than other impedances. Then, the LDO’s output impedance can be expressed as follows by ignoring the load impedance and R_F. (* s is the Laplacian operator.)

$$Z_{OUT} = \frac{r_{DS} \left(\frac{1}{sC_{OUT}} + R_{ESR} \right)}{r_{DS} + \left(\frac{1}{sC_{OUT}} + R_{ESR} \right)} = \frac{\frac{1}{sC_{OUT}} + R_{ESR}}{1 + \left(\frac{1}{sC_{OUT}} + R_{ESR} \right) / r_{DS}}$$

The output resistance (r_{DS}) of the PMOS pass device can also be ignored because it is higher than the impedance of the output capacitor (C_{OUT}) during the sudden load change discussed here. For example, if a load change takes 1 μ s, it has a frequency of at least 250 kHz. If the value of the output capacitor (C_{OUT}) is 1 μ F, its impedance at a frequency of 250 kHz is calculated to be as low as 0.64 Ω . Suppose that an LDO has a supply voltage of 2 V, an output voltage of 1 V, and an output current of 200 mA. Then, the output resistance (r_{DS}) of its PMOS pass device is calculated to be 5 Ω , which is sufficiently higher than the impedance of the output capacitor. Typically, the output capacitor has an equivalent series resistance of less than 10 m Ω . When such an output capacitor is used, its equivalent series resistance can be ignored since it is one order of magnitude lower than its impedance. In light of the above discussion, an LDO's output impedance can be determined largely by the impedance (Z_{COUT}) of the output capacitor (C_{OUT}):

$$Z_{OUT} \cong \frac{1}{sC_{OUT}} = Z_{COUT}$$

As described above, an LDO's output voltage variation due to load changes is equal to a change in load current multiplied by the output impedance of the LDO. Because $CV = IT$ (where, C is the capacitor value, V is the voltage across the capacitor, I is the current flowing through the capacitor, and T is the period of time during which this current flows), the LDO's output voltage variation can be approximated as follows:

$$\Delta V_{OUT} = \frac{\Delta I_{OUT} \cdot T}{C_{OUT}}$$

What does T in this equation represent?

As described above, T is the sum of the time required for an error amplifier to generate an error voltage signal according to its slew rate immediately after a change in an LDO's output voltage and the time required for the PMOS pass device to pass an output current equal to the increased load current. In other words, T is the time required for the negative feedback loop to begin tracking the output voltage change. T is determined by the drive capability of the error amplifier, the capacitances on its output (phase compensation capacitance and the gate capacitance of the PMOS pass device), and the transconductance of the PMOS pass device.

* The above equation is simplified to approximate the output voltage variation (ΔV_{OUT}) due to load changes.

To accurately calculate ΔV_{OUT} due to load changes, it is necessary to accurately determine the transfer function of an LDO's internal circuitry.

3.2. Using an external phase compensation capacitor (C_{FB}) to improve the load transient response of adjustable-output LDOs

There are two types of LDOs: fixed-output LDOs whose output voltage is internally determined and adjustable-output LDOs whose output voltage is programmable via external resistors (Figure 3.2.1).

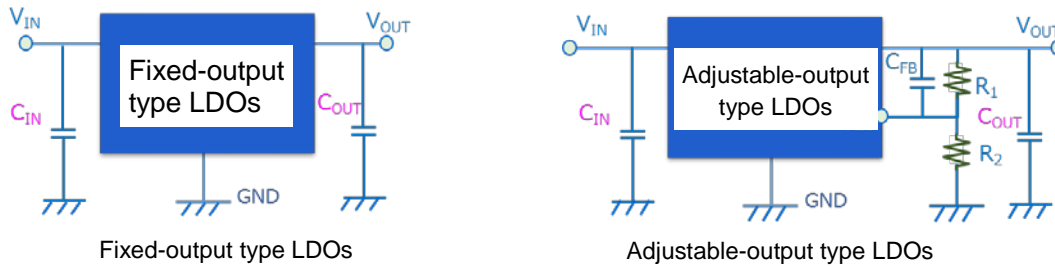


Figure 3.2.1 Fixed- and adjustable-output LDOs

The output voltage of the adjustable-output LDO shown above is programmable via two external resistors (R_1 and R_2).

The output voltage of this LDO is given by:

$$V_{OUT} = \frac{R_1 + R_2}{R_2} V_{ADJ}$$

Toshiba’s LDOs operate properly without an external phase compensation capacitor (C_{FB}). However, LDOs are susceptible to oscillation, depending on their applications. In that case, C_{FB} should be connected in parallel with resistor R_1 . Although this capacitor acts as a phase compensation capacitor, it also helps improve load transient response. Let’s consider the case where the load current suddenly increases as shown in Figure 3.2.2. As described above, connecting a capacitor (C_{OUT}) to the output of an LDO is very effective in suppressing its output voltage variation. Most of the increased load current flows to the output capacitor (C_{OUT}), discharging it, because it has low impedance at high frequency. Although this helps reduce the output voltage variation of the LDO, there still remains a slight variation. In contrast, when a capacitor (C_{FB}) is connected in parallel with resistor R_1 , R_1 is short-circuited at high frequency because of the effect of C_{FB} . Therefore, the output voltage variation of an LDO is transferred to its negative feedback pin (V_{ADJ}) without any decay. In this case, an error amplifier in the LDO provides an error signal with a higher voltage, which causes the PMOS pass device to provide a higher output current. Consequently, the LDO responds faster to an increase in load current, thereby further suppressing output voltage variations.

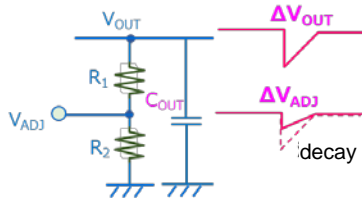


Figure 3.2.2 Output voltage variation of an LDO without C_{FB}

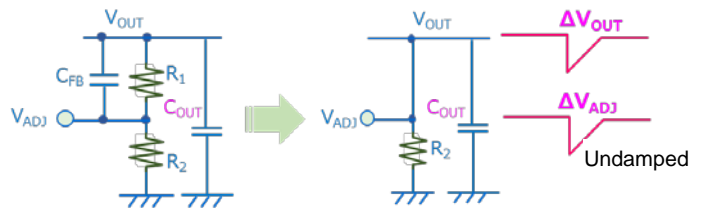


Figure 3.2.3 Output voltage variation of an LDO with C_{FB}

4. Summary of load transient response improvement

From the equation shown in Section 3.1, it can be seen that increasing the value of the output capacitor (C_{OUT}) helps reduce the output voltage variation (ΔV_{OUT}) due to sudden load changes. Care should be taken, however, because a larger output capacitor (C_{OUT}) causes an increase in inrush current during the rise of an LDO's output voltage. The above equation also indicates that reducing the time required for the negative feedback loop to track changes in V_{OUT} (T) helps reduce output voltage variations. T can be reduced by 1) increasing the error amplifier current, 2) reducing the gate capacitance of the PMOS pass device, and 3) reducing the value of a phase compensation capacitor in the error amplifier. However, these measures cause increases in supply current, dropout voltage, and susceptibility to oscillation, respectively. Toshiba's LDOs are optimized, taking these trade-offs into consideration, so as to reduce supply current without compromising dropout characteristics and to achieve fast load transient response without causing oscillation.

4.1. Dual-power-supply LDO with an NMOS pass device: Load transient response of the TCR5BM, TCR8BM, and TCR15AG

4.1.1. Load transient response of dual-power-supply LDOs with an NMOS pass device

Figure 4.1.1 shows a simplified diagram of Toshiba's dual-power-supply LDO with an NMOS pass device.

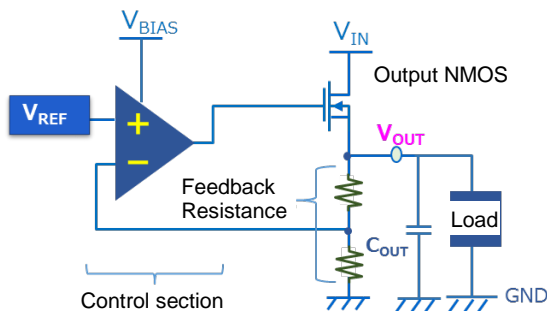


Figure 4.1.1 Simplified diagram of Toshiba's dual-power-supply LDO with an NMOS pass device

Toshiba's dual-power-supply LDO with an NMOS pass device has two separate power supply pins: one for the control section (V_{BIAS}) and the other for the NMOS pass device (V_{IN}). Applying a higher voltage to V_{BIAS} than V_{IN} increases the gate voltage of the NMOS pass device, reducing the dropout voltage of an LDO.

The discussions in the previous sections also apply to dual-power-supply LDOs with an NMOS pass device, except that the output impedance of the dual-power-supply LDO is expressed as below

when the negative feedback loop cannot track sudden load changes (where g_m is the transconductance of the NMOS pass device). As is the case with single-power-supply LDOs, the low impedance of the output capacitor (C_{OUT}) is dominant in the high-frequency region. Therefore, the LDO's output impedance in the event of sudden changes in load current is expressed as follows:

$$Z_{OUT} = \frac{1}{g_m + sC_{OUT}} \cong \frac{1}{sC_{OUT}}$$

The next subsection shows the load transient response waveforms of the TCR5BM, TCR8BM, and TCR15AG dual-power-supply LDOs with an NMOS pass device.

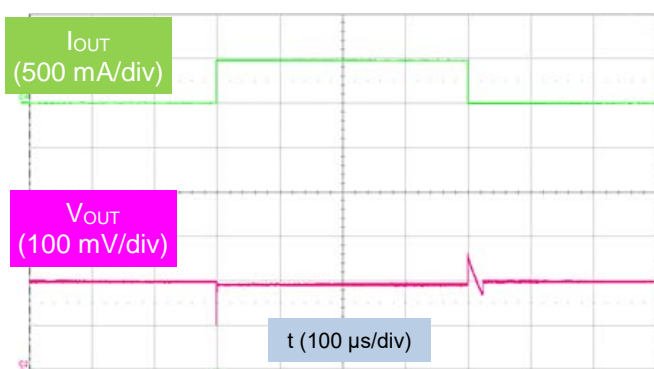
4.2. Load transient response waveform of the TCR5BM and TCR15AG dual-power-supply LDO series

The following subsections show the measured load transient response waveforms of Toshiba's TCR5BM and TCR15AG 500-mA LDO series.

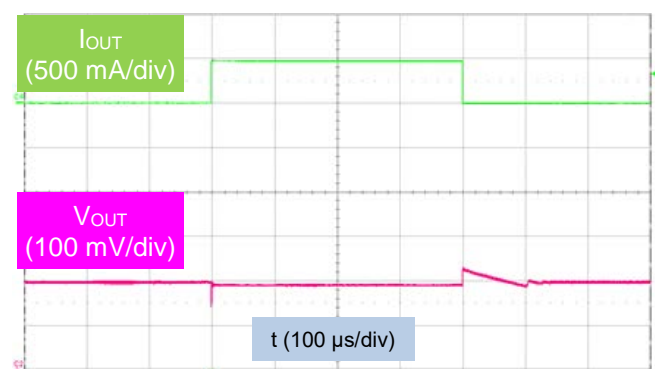
4.2.1. Load transient response waveform of the TCR5BM12 500-mA dual-power-supply LDO

As described in the previous section, the TCR5BM12 allows output voltage variations due to changes in load current to be roughly halved by increasing the value of C_{OUT} from 2.2 μF to 22 μF . In the following figure, the load current steps from 1 mA to 500 mA and then back to 1 mA in roughly 1 μs . If the current change is lower or slower, the output voltage variation becomes lower than the load transient response shown below.

Test conditions: $V_{IN} = 1.35 \text{ V}$, $V_{BIAS} = 3.3 \text{ V}$, $V_{OUT} = 1.2 \text{ V}$, $C_{IN} = 1 \mu\text{F}$, $C_{BIAS} = 0.1 \mu\text{F}$, $I_{OUT} = 1 \text{ mA} - 500 \text{ mA} - 1 \text{ mA}$ ($t_r = t_f \approx 1 \mu\text{s}$)



Load transient response waveform of the TCR5BM12 with a C_{OUT} of 2.2 μF



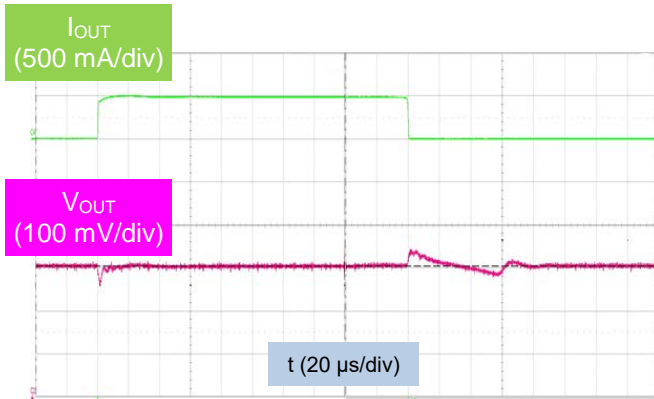
Load transient response waveform of the TCR5BM12 with a C_{OUT} of 22 μF

4.2.2. Load transient response waveform of the TCR15AGADJ 1.5-A dual-power-supply LDO

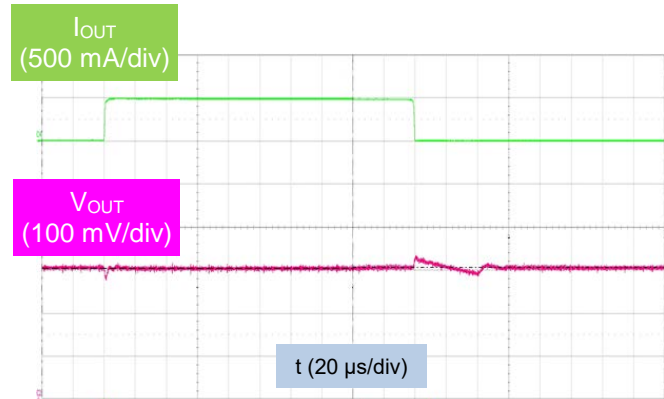
The TCR15AGADJ 1.5-A LDO allows output voltage variations due to changes in load current to be reduced by adding C_{FB} without changing the C_{OUT} value. The added benefit of this is an

improvement in the power supply ripple rejection (PSRR). In the following figure, the load current steps from 1 mA to 500 mA and then back to 1 mA in roughly 1 μ s. If the current change is lower or slower, the output voltage variation becomes lower than the load transient response shown below.

Test conditions: $V_{IN} = 1.35$ V, $V_{BIAS} = 3.3$ V, $V_{OUT} = 1.2$ V ($R1 = 24$ k Ω , $R2 = 24$ k Ω),
 $C_{IN} = 10$ μ F, $C_{BIAS} = 0.1$ μ F, $C_{OUT} = 20$ μ F,
 $I_{OUT} = 10$ mA–500 mA–10 mA ($t_r = t_f \approx 1$ μ s)



Load transient response waveform of the TCR15AGADJ without C_{FB}



Load transient response waveform of the TCR15AGADJ with a C_{FB} of 10 nF

5. Conclusion

LDOs provide a supply voltage for high-performance semiconductor devices operating at low voltage. It is therefore necessary to minimize their output voltage variations due to changes in load current. Toshiba's LDOs are optimized to provide fast load transient response while maintaining good trade-offs with supply current, dropout characteristics, susceptibility to oscillation, and other factors. Increasing the value of the output capacitor (C_{OUT}) helps improve load transient response. In the case of adjustable-output LDOs, connecting a phase compensation capacitor (C_{FB}) in parallel with an external resistor further improves load transient response.

Toshiba's product portfolio includes 300-mA to 1.5-A LDOs with fast transient response suitable for various applications.

Toshiba's LDO regulators with fast load transient response

To download the data sheet for the TCR3DM 300-mA fixed-output LDO regulator → [Click Here](#)

To download the data sheet for the TCR5BM 500-mA fixed-output LDO regulator → [Click Here](#)

To download the data sheet for the TCR8BM 800-mA fixed-output LDO regulator → [Click Here](#)

To download the data sheet for the TCR13AGADJ

1.3-A adjustable-output LDO regulator → [Click Here](#)

To download the data sheet for the TCR15AG series

1.5-A fixed- and adjustable-output LDO regulators → [Click Here](#)

To download a reference design for the TCR15AG

1.5-A adjustable-output LDO regulator → [Click Here](#)

For more information on the usage of LDO regulators, see the Application Note for Low Drop Out (LDO) regulator IC:

To download the Application Note for Low Drop Out (LDO) regulator IC → [Click Here](#)

6. Related Links

■ Product Line Ups (Catalog)

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■ Product Line Ups (Parametric search)

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■ Stock check & Purchase



■ FAQ of Low Dropout Regulator ICs

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■ Application Notes

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