Basics of N-Channel MOSFET Gate Driver ICs

(TCK401G and TCK402G)

Outline:

This Gate Driver IC drives the gate of N-channel MOSFET used for the load switch. A proper high voltage must be applied to the gate to turn MOSFET on with low on-resistance. In addition to the charge pump circuitry that drives the N-channel MOSFET, the built-in overvoltage protection, under voltage malfunction prevention (UVLO), slew rate control, auto-discharge, and back-to-back protection provide a robust power management system.

This document explains the functions and precautions for use using TCK401G/ TCK402G as an example that is ultra-compact and achieves higher operating voltages.

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1. Introduction

The TCK401G and TCK402G are MOSFET gate driver ICs that make it possible to supply high current and voltage to a load using external N-channel MOSFETs. The TCK401G and TCK402G provide reverse-current blocking when two MOSFETs are externally connected in a common-source configuration.

Having a sufficient capability to drive low-on-resistance N-channel MOSFETs, the TCK401G and TCK402G allow a circuit configuration with minimum power dissipation and heat generation. The USB PD Specification requires not only an increase in current to reduce the charging time but also a tolerance for high charging voltage. The TCK401G and TCK402G operate over a wide input voltage range from 2.7 V to 28 V and therefore support USB PD and other rapid-charging loads. These MOSFET gate driver ICs incorporate a slew rate control function to limit unexpected inrush current during switch-on in order to protect the subsequent IC or circuitry. The TCK401G and TCK402G also provide automatic output discharge at switch-off. Therefore, they can be used for applications requiring stringent power management without any concern about a lag between a switch-off signal and the time when the output voltage reaches zero.

This application note discusses the operations and features of the TCK401G and TCK402G, N-channel MOSFET gate driver ICs designed for high-current power management to reduce system power consumption and improve system stability.

1.1. Applications of the TCK401G and TCK402G

The TCK401G and TCK402G are optimum for the following applications(Figure 1.1):

- Battery charging and other power management applications
- Charging/discharging circuits for devices with a USB connector
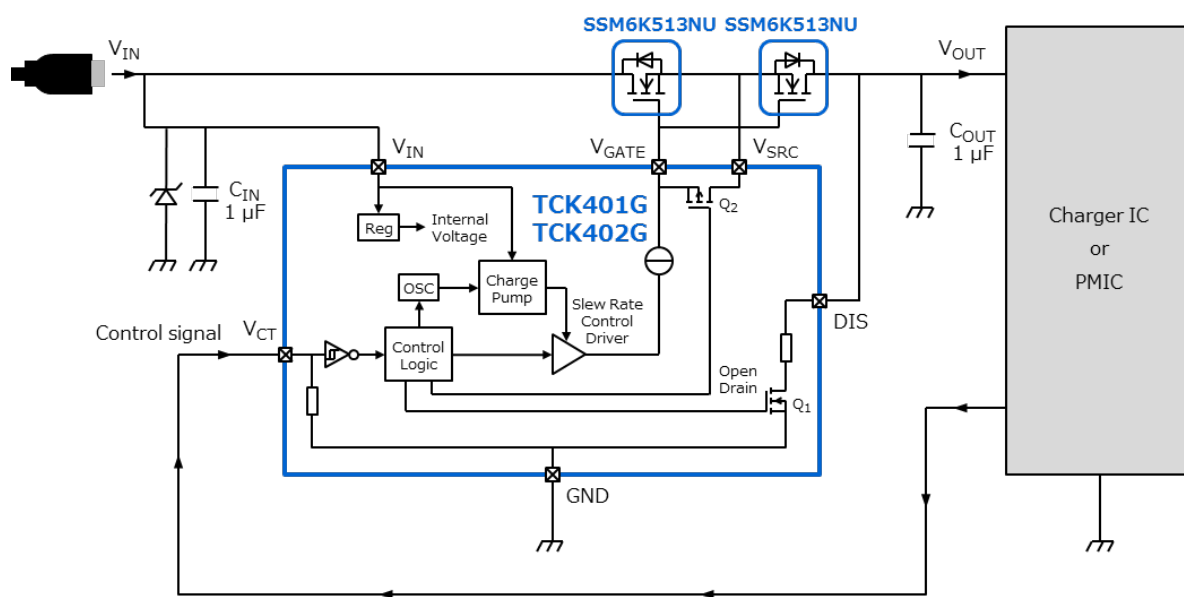

Figure 1.1 Application example for the TCK401G and TCK402G

To perform a parametric search of MOSFETs suitable for applications like the one shown in Figure1.1.

→ Click Here

To perform a parametric search of TVS (ESD protection) diodes suitable for high-current applications such as charging circuits → Click Here

2. Difference between the TCK401G and TCK402G

The TCK401G and TCK402G differ only in the input logic of the mode control terminal (V_{CT}) as shown in Table 2.1. Except for this difference in the input logic, they are identical in all other respects, including their operations and electrical characteristics. The TCK401G with the active-High V_{CT} terminal turns on when High-level voltage (i.e., voltage higher than V_{IH}) is applied to the V_{CT} terminal as shown in Figure 2.1, causing the voltage of the V_{GATE} terminal, which drives external MOSFETs, to rise. In contrast, the TCK402G with the active-Low V_{CT} terminal turns on when Low-level voltage (i.e., voltage lower than V_{IL}) is applied to the V_{CT} terminal as shown in Figure 2.2, causing the voltage of the V_{GATE} terminal to rise.
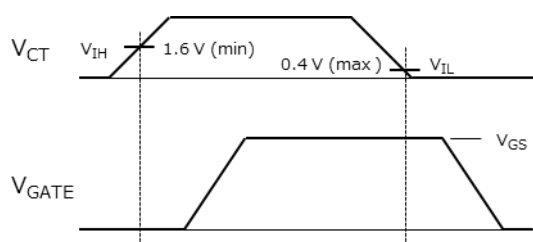
Figure 2.1 Operation of the TCK401G (active-High)
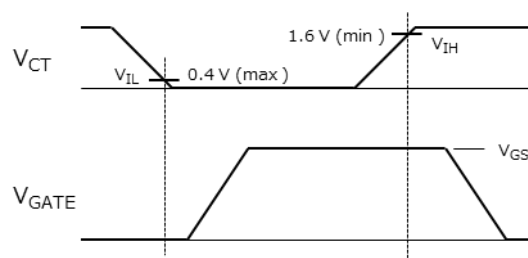
Figure 2.2 Operation of the TCK402G (active-Low)

Table 2.1 Difference between the TCK401G and TCK402G

Part number	Logical sense of V_{CT}	Pull resistor on V_{CT}
TCK401G	Active-High	Pull-down
TCK402G	Active-Low	Pull-down

3. Internal block diagram and operations of the TCK401G and TCK402G
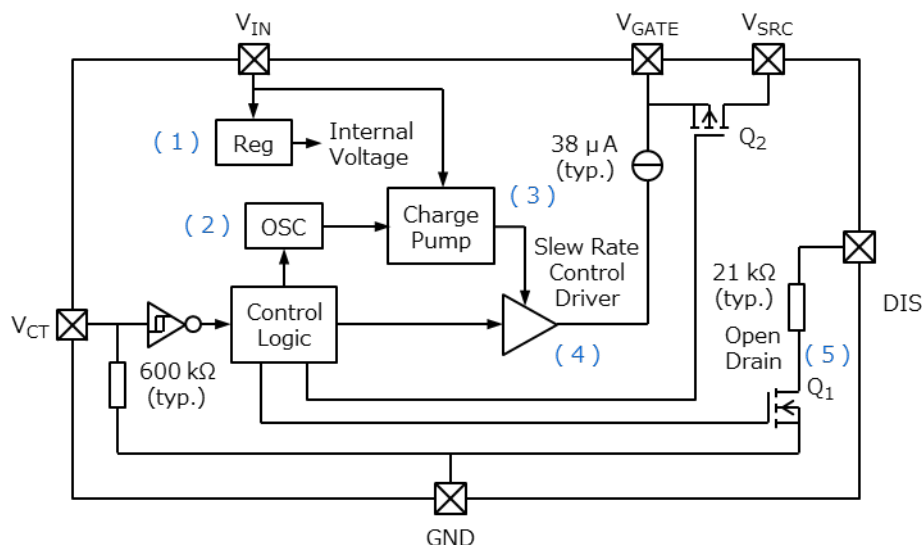
Figure 3.1 Internal block diagram of the TCK401G and TCK402G

(1) Voltage regulator for the internal control circuit

The voltage regulator regulates the supply voltage for the internal circuit.

(2) Oscillator

The oscillator drives a charge pump, which drives the gates of external N-channel MOSFETs.

(3) Charge pump

A charge pump is a voltage booster that generates a voltage for the gate drive of N-channel MOSFETs. In the case of the TCK401G and TCK402G, as the input voltage (V_{IN}) increases, the gate voltage (V_{GATE}) increases as shown in Figure 3.2. The charge pump controls voltage boost according to changes in the input voltage (V_{IN}) so that the V_{GATE} voltage will not exceed the maximum permissible gate drive voltage (V_{GS}). When V_{IN} exceeds roughly 28 V, the TCK401G and TCK402G shut down automatically for system protection. Table 3.1 shows the V_{GATE} characteristics with respect to V_{IN}. For example, when V_{IN} = 12 V, V_{GATE} is 20.5 V typical (12 V + 8.5 V) and 22 V maximum (12 V + 10 V).
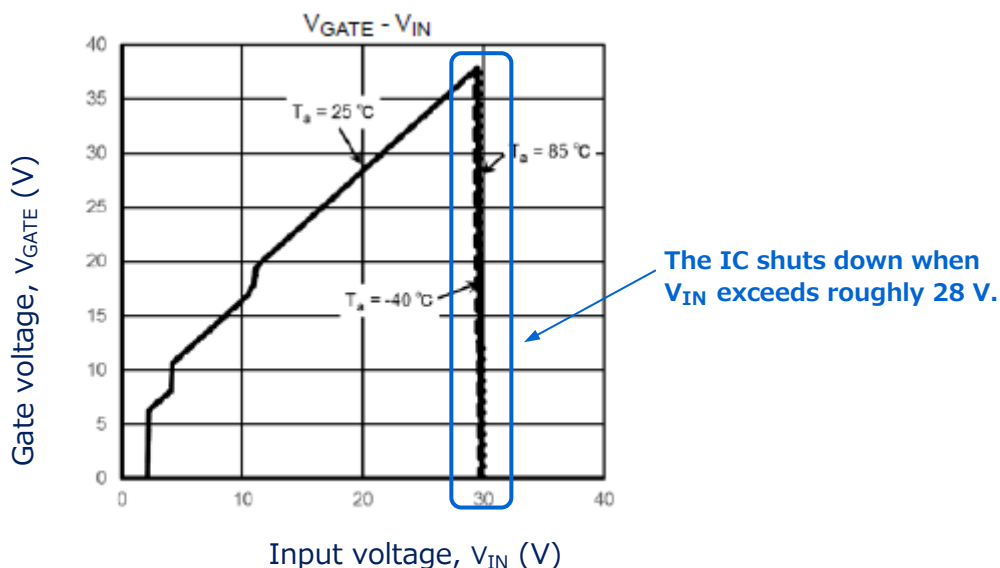
Figure 3.2 V_{GATE} − V_{IN} curve of the TCK401G and TCK402G

Table 3.1 Gate drive voltage characteristics of the TCK401G and TCK402G

Characteristic	Symbol	Test Conditions	T_a = 25°C			T_a = −40 to 85°C		Unit
			Min	Typ.	Max	Min	Max	
Gate drive voltage (V_{GATE} − V_{IN})	V_{GS}	V_{IN} = 3 V	−	4.0	−	2.8	5.1	V
		V_{IN} = 5 V	−	6.5	−	5.1	7.9	V
		V_{IN} = 9 V	−	6.5	−	5.1	7.9	V
		12 V ≤ V_{IN} ≤ 28 V	−	8.5	−	6.9	10	V

(4) Gate drive circuit with inrush current suppression capability (slew rate control)

Inrush current is limited by the slew rate control circuit. When a large capacitive load is connected to the output MOSFET, turning it on at high speed causes a large current to flow to charge the load. At this time, V_{IN} drops instantaneously because of the impedance of board traces on the V_{DD} side of a load switch IC, causing system instability or malfunction. The slew rate control circuit limits inrush current to ensure a stable system boot-up. The TCK401 and TCK402G also incorporate a constant-current source (38 µA typical), which drives the gates of external MOSFETs.

Table 3.2 Output current (gate drive current) characteristic of the TCK401G and TCK402G

Characteristic	Symbol	Test Conditions	T_a = 25 °C			Unit
			Min	Typ.	Max	
Output current	$I_{GATE(ON)}$	V_{IN} = 5 V	−	38	−	µA

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Figure 3.3 shows the output waveforms of a load switch composed of discrete MOSFETs whereas Figure 3.4 shows the output waveforms of a load switch configured using the TCK401G.

Test conditions: V_{IN} = 5V, V_{CT}= 0 V → 5 V, I_{OUT} = 5 A, C_{OUT} = 4.7 µF, T_a = 25°C
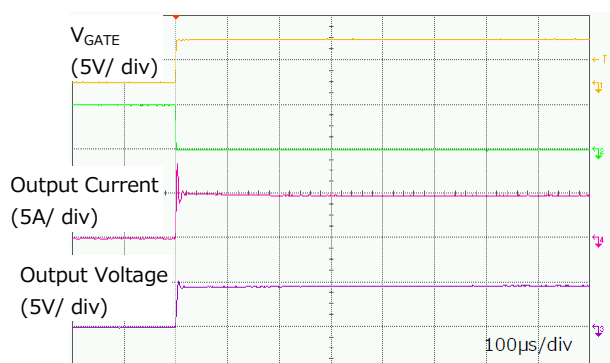
Figure 3.3 Output waveforms of a load switch composed of discrete MOSFETs

Figure 3.4 Output waveform of a load switch configured using the TCK401G

(4-1) When a load switch is composed of discrete MOSFETs (Figure 3.3)
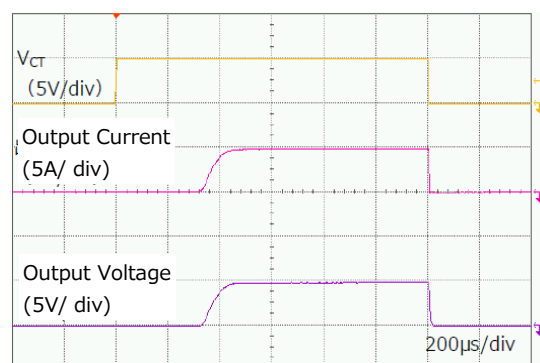
In the case of a load switch composed of discrete MOSFETs, the peak output current of the MOSFETs with a C_{OUT} of 4.7 µF reaches 7 to 8 A when the load current is set to 5 A. In addition, the ringing caused by the peak current might generate electromagnetic interference (EMI) that adversely affects electronic circuits. It is therefore necessary to suppress inrush current during switch-on transitions.

(4-2) When the TCK401G is used (Figure 3.4)

In contrast, the TCK401G controls the rising slew rate of its output voltage to suppress inrush current, thereby reducing ringing and EMI. A downside of slew rate control is that it causes a delay from when a control signal is applied to the V_{CT} terminal of the TCK401G to when the TCK401G begins operation. This delay is caused by the time required for signal processing in the TCK401G.
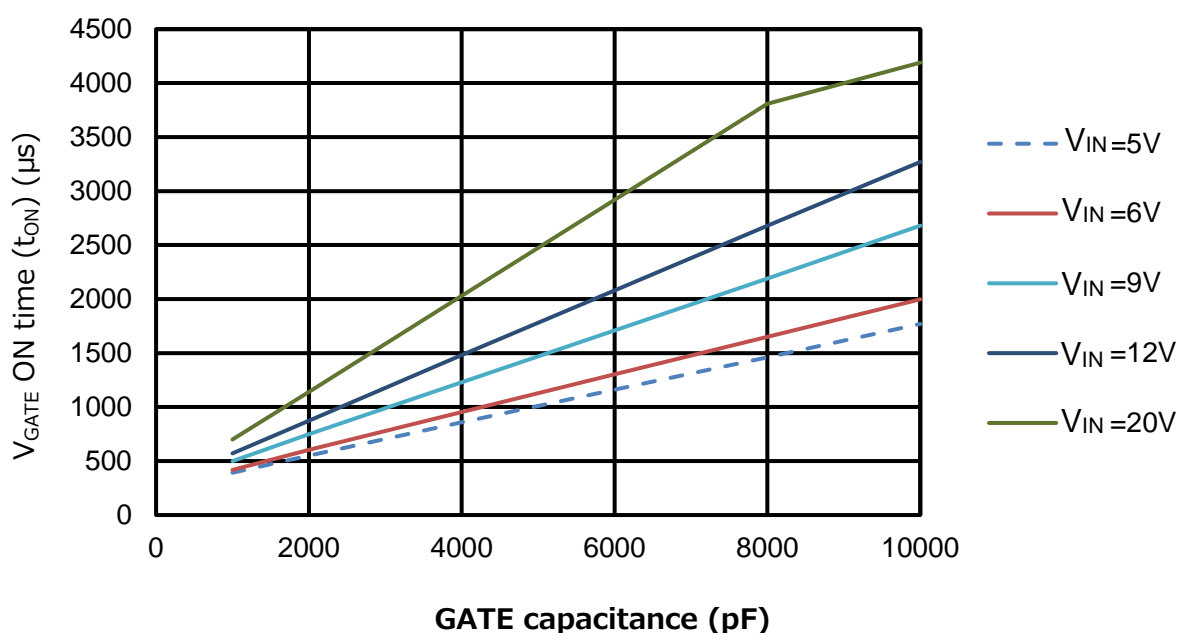
* V_{GATE} ON time (t_{ON}) of the TCK401G

The V_{GATE} output of the TCK401G drives the MOSFET gate inputs. The V_{GATE} ON time (t_{ON}) shown in its datasheet is not a specification that defines the switching time of external MOSFETs in actual applications. In practice, the turn-on time of the MOSFETs depends on their gate capacitance and threshold voltage (V_{th}) as shown in Table 3.3 and Figure 3.5. The V_{GATE} ON time (t_{ON}) of the TCK401G is specified at a gate capacitance of 2000 pF. The assumption is that the TCK401G is used to drive two back-to-back MOSFETs in a common-source configuration, each with a gate capacitance of roughly 1000 pF. When the TCK401G drives MOSFETs with lower gate capacitance, its V_{GATE} ON time is less than indicated in the datasheet. This means the switching time of external MOSFETs becomes shorter. Conversely, when the TCK401G drives MOSFETs with higher gate capacitance, the MOSFET switching time becomes longer because of a longer V_{GATE} ON time. When MOSFETs with a high threshold voltage (V_{th}) are used, it is recommended to use the TCK401G at an input voltage (V_{IN}) as high as possible in order to raise the V_{GATE} voltage. For a description of the datasheet specification

of the V_{GATE} ON time, see Section 5.1, "Switching times of the V_{GATE} terminal."

**Table 3.3 V_{GATE} ON time (t_{ON}) simulation data**

V_{IN} (V)	Gate capacitance (pF)						Unit
	1000	2000	4000	6000	8000	10000	
V_{IN} = 5 V	392	550	860	1160	1460	1770	
V_{IN} = 6 V	418	605	953	1302	1650	1998	
V_{IN} = 9 V	499	750	1230	1710	2190	2680	µs
V_{IN} = 12 V	571	874	1480	2080	2680	3270	
V_{IN} = 20 V	700	1140	2030	2920	3810	4190	

Figure 3.5 V_{GATE} ON time - Gate capacitance

(5) Automatic output discharge circuit

A load remains charged after the TCK401G or TCK402G turns off when it is connected to a capacitive load. This makes it impossible to set an appropriate power supply sequence for a system with multiple load switch ICs. When a load switch IC turns off, the automatic output discharge circuit in the TCK401G or TCK402G turns on an internal MOSFET connected between DIS and GND terminals to discharge the load quickly. This circuit reduces the discharge time even when a large output capacitor is connected to a load switch IC, simplifying the setting of a system power sequence.
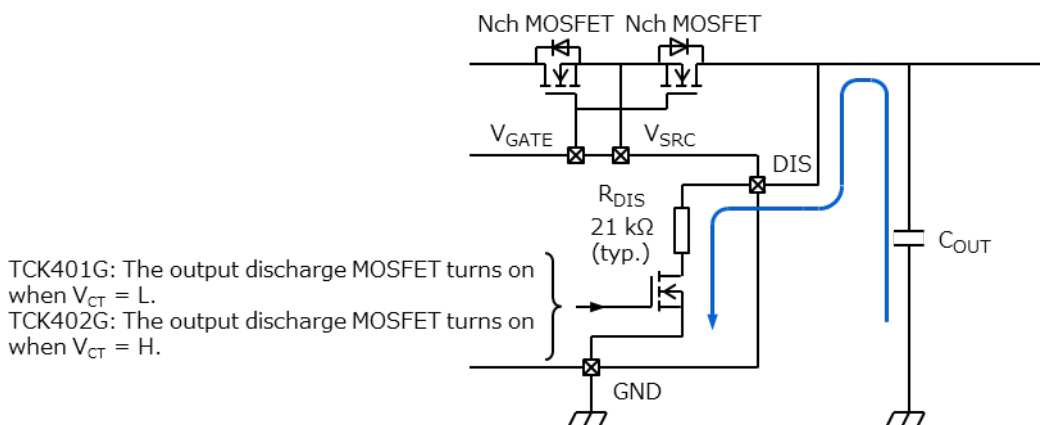
Figure 3.6 Automatic output discharge circuit of the TCK401G and TCK402G

Test conditions: V_{IN} = 5 V, V_{CT}= 0 V → 5 V, I_{OUT} = 5 A, C_{OUT} = 4.7 μF, T_a = 25°C
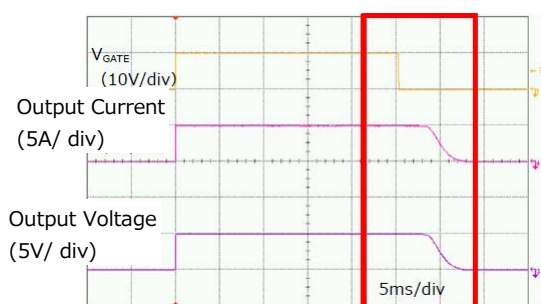
Figure 3.7 Output waveform of the TCK401G when the automatic output discharge function is disabled

Figure 3.8 Output waveform of the TCK401G when the automatic output discharge function is enabled

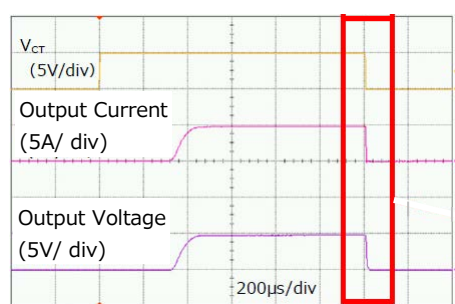# 4. Protection features

4.1. Reverse-current blocking using external common-source MOSFETs

The reverse-current blocking function prevents current from flowing in the reverse direction from the output to the input when the TCK401G and TCK402G are disabled, for example, when the V_{IN} power supply is off or when the V_{CT} terminal is in the inactive state. The TCK401G and TCK402G provide reverse-current blocking using external back-to-back MOSFETs. When two external N-channel MOSFETs are connected back-to-back in a common-source configuration as shown in Figure 4.1, the TCK401G and TCK402G prevent reverse current at turn-off by switching off both the MOSFETs simultaneously.

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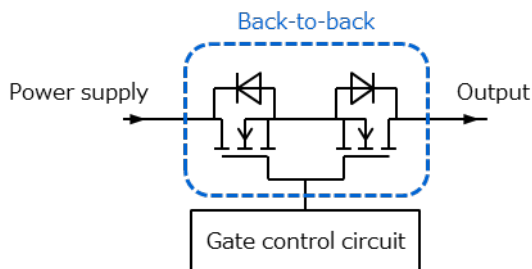
Figure 4.1 Reverse-current blocking using back-to-back MOSFETs

4.2. Undervoltage lockout (UVLO)

Undervoltage lockout (UVLO) is a feature to prevent system malfunction even when a decrease in V_{IN} causes the output gate voltage (V_{GATE}) to drop below the minimum operating voltage of the subsequent IC or circuitry. The UVLO circuit turns off the output gate voltage (V_{GATE}) in the event of an excessive drop in V_{IN}(Figure 4.2).
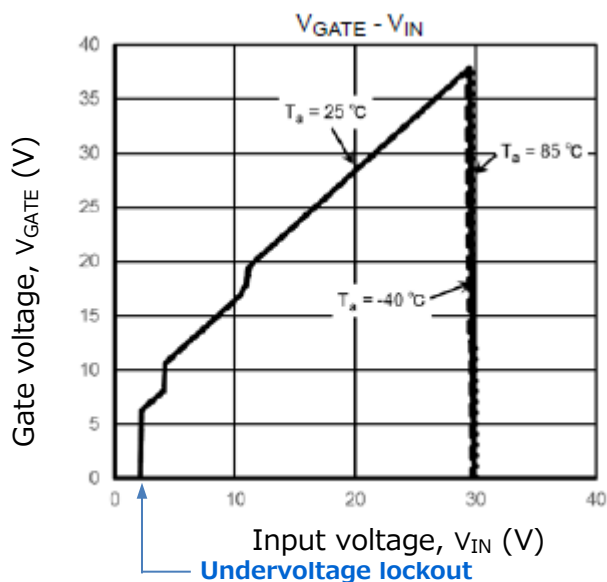
Figure 4.2 Undervoltage lockout (UVLO) operation

4.3. Overvoltage lockout (OVLO)

In the event of V_{IN} exceeding the prescribed voltage, the overvoltage lockout (OVLO) circuit turns off the output to protect the subsequent IC or circuitry(Figure 4.3).
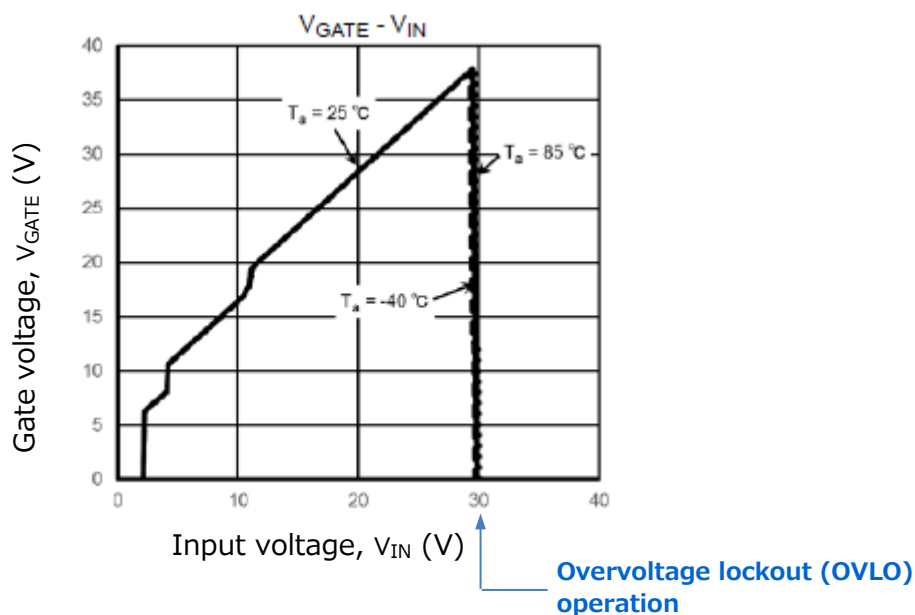
Figure 4.3 Overvoltage lockout (OVLO) operation

4.4. Input-tolerant function

The input-tolerant function prevents current from flowing from the V_{CT} terminal to the V_{IN} terminal when the control terminal (V_{CT}) voltage exceeds V_{IN} and when $V_{IN} = 0$ V(Figure 4.4).
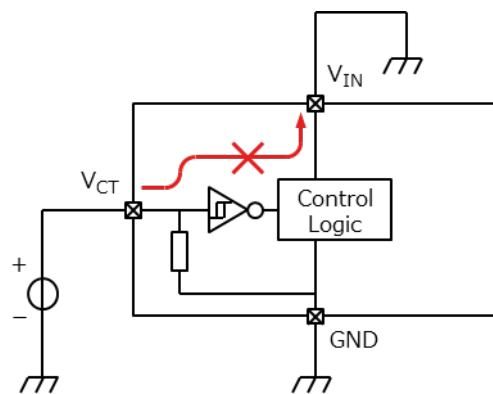
Figure 4.4 Input-tolerant function

5. Switching times of the TCK401G and TCK402G

5.1. Switching times of the V$_{GATE}$ terminal

The V$_{GATE}$ output drives the gate inputs of external MOSFETs. When the V$_{CT}$ input assumes the active state, the TCK401G and TCK402G boost the voltage applied to the V$_{IN}$ input and pass it to the V$_{GATE}$ output. The following describes the conditions at which the slew rate control function is specified.

Figure 5.1 and Figure 5.2 show the timing chart of the V$_{CT}$ and V$_{GATE}$ terminals of the TCK401G and TCK402G respectively. The V$_{GATE}$ ON time (t$_{ON}$) shown in the AC Characteristics table in the datasheet is the time required for the V$_{GATE}$ voltage to rise from the 50% point of V$_{CT}$ to (V$_{IN}$ + 1) V. The slew rate control circuit maintains the slope of the V$_{GATE}$ output. Therefore, the higher the VIN voltage, the longer the V$_{GATE}$ ON time (t$_{ON}$). The V$_{GATE}$ OFF time (t$_{ON}$) is the time required for the V$_{GATE}$ voltage to decrease from the 50% point of V$_{CT}$ to 0.5 V.
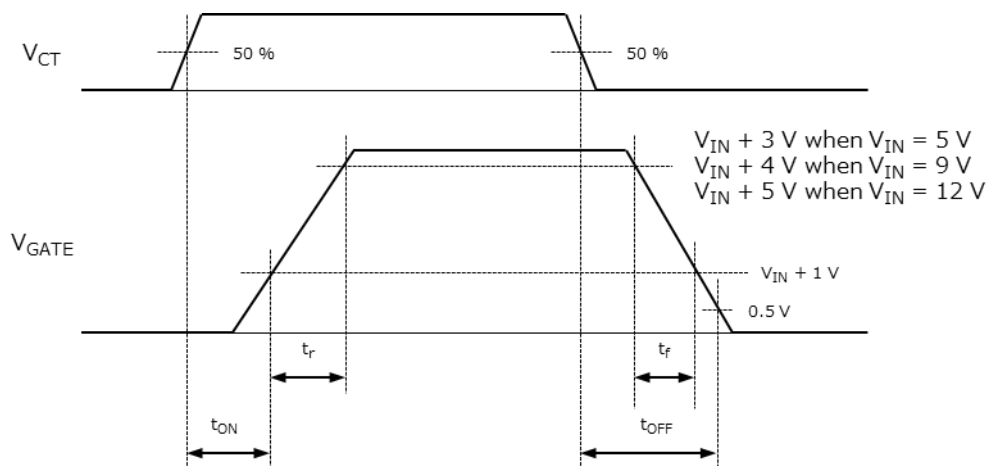
Figure 5.1 Switching times of the TCK401G
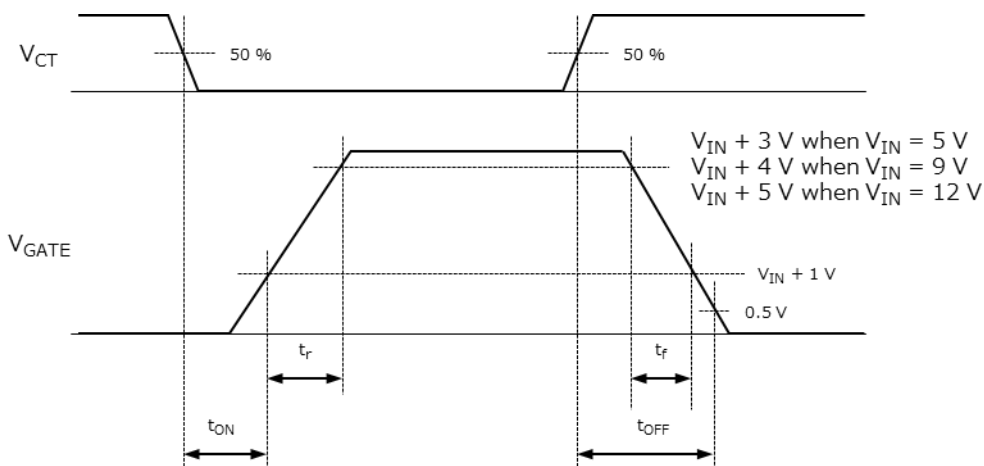
Figure 5.2 Switching times of the TCK402G

6. Usage Considerations
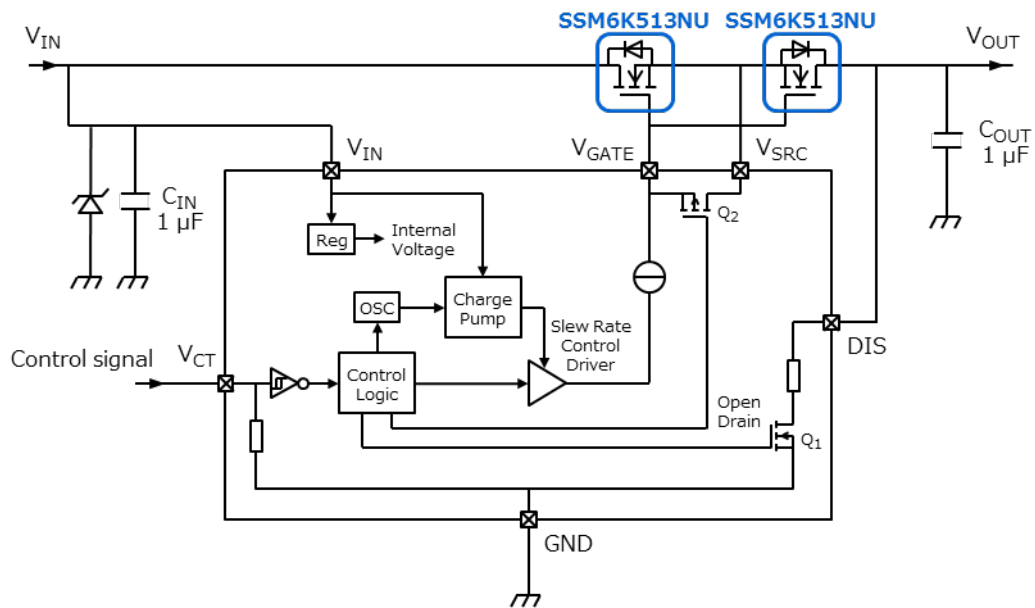
Figure 6.1 Applications circuit for the TCK401G and TCK402G

6.1. Input and output capacitors

Connect an input capacitor (C_{IN}) and an output capacitor (C_{OUT}) to ensure stable operation of the TCK401G and TCK402G. C_{IN} and C_{OUT} should be at least 1 µF and connected as close as possible to the input and output terminals. The withstand voltage of these capacitors should be sufficiently higher than their operating voltage(Figure 6.1).

6.2. V_{CT} terminal

A Schmitt trigger inverter is connected to the V_{CT} terminal of the TCK401G and TCK402G. The Schmitt trigger inverter has different thresholds (V_P and V_N) for positive-going and negative-going inputs. As shown in Figure 6.2(b), it provides a stable output even in the event of the control signal being superimposed with contact chatter and ringing from a mechanical switch. In contrast, non-Schmitt inverters with a single threshold might cause the output to malfunction as shown in Figure 6.2 (a).

Figure 6.2 Operations of typical and Schmitt trigger inverters

6.3. V$_{SRC}$ terminal

When two MOSFETs are driven, voltage might remain at the V$_{GATE}$ terminal even after the TCK401G or TCK402G switches off owing to the effect of capacitance, causing excessive gate-source voltage (V$_{GS}$) to be applied to the MOSFETs. To prevent this, the V$_{SRC}$ terminal short-circuits the V$_{GATE}$ output to the source terminals of the MOSFETs when the TCK401G or TCK402G is off. The V$_{SRC}$ terminal may be left open if the MOSFETs have a sufficient margin for V$_{GS}$.
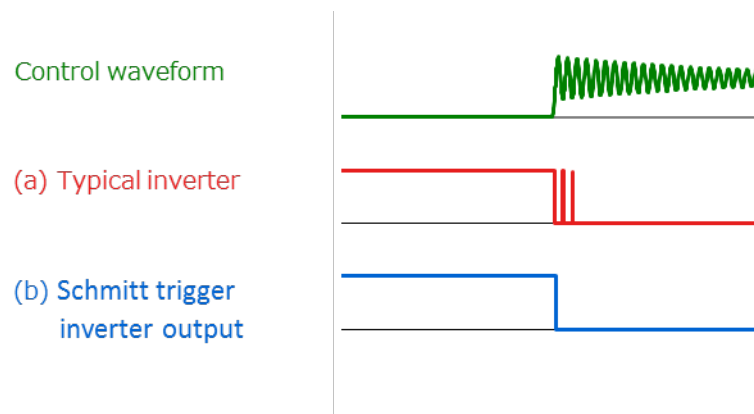
In cases where the TCK401G or TCK402G drives only one MOSFET, the V$_{SRC}$ terminal may also be left open if the MOSFET gate-source voltage (V$_{GS}$) has a sufficient margin.

It is recommended to connect V$_{SRC}$ to V$_{OUT}$ if V$_{GS}$ does not have an adequate margin. Connecting the V$_{SRC}$ and V$_{OUT}$ terminals together causes an increase in t$_{OFF}$ because of the effect of C$_{OUT}$.

Therefore, allow a sufficient margin when selecting MOSFETs.

6.4. DIS terminal

Connect the DIS terminal to V$_{OUT}$ if automatic output discharge is necessary when the TCK401G or TCK402G turns off. Otherwise, the DIS terminal may be left open.

7. Conclusion

This application note has discussed the basics of the TCK401G and TCK402G, gate driver ICs for load switch ICs, such as their electrical characteristics and protection features shown in the datasheet. Load switch ICs are very effective for the power management of mobile and other electronic devices. Toshiba provides not only gate driver ICs but also various low-loss load switch ICs incorporating MOSFETs. We hope that you have found this application note useful in considering using load switch ICs.

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