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Evaluation methodology for current collapse phenomenon of GaN HEMTs

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***Abstract*—Methods of both evaluation and analysis of current collapse (C/C) in GaN HEMTs are discussed. Recently, guidelines to the methods of evaluation of C/C in comparing device characteristics have been required as the increase in on-resistance resulting from C/C depends significantly on stress conditions and the applied method. Therefore, as a guideline, we propose the DC voltage stress and inductance load switching stress for the evaluation.**

***Index Terms*—Current collapse, Evaluation method, GaN transistors, High electron mobility, Inductance load switching.**

I. Introduction

By taking advantage of its low-loss high-speed switching, the GaN power device is a promising candidate for achieving high efficiency and/or downsizing of the system. This device, however, has a serious issue in that the on-resistance (R_{on}) increases because of the current-collapse (C/C) phenomenon under switching operations causing an increase in device loss and temperature [1]. As a reliability issue, the evaluation of C/C is important.

II. Current Collapse Phenomenon

In GaN power devices, C/C is a phenomenon in which R_{on} increases depending on the stress condition (e.g., drain voltage) [2,3]. The cause stems from some of the electrons accelerating under voltage stress getting trapped in the crystal or a dielectric film, or even at the interface between dielectric and semiconductor layer. The location and density of these traps depend on the device structure and manufacturing process. When electrons are trapped, negative charges cause depletion of the channel of the two-dimensional electron gas (2DEG), resulting in an increase in R_{on} and a decrease in drain current I_{ds} (Fig. 1) [4]. We investigated the depletion mode GaN HEMT (Fig. 2).

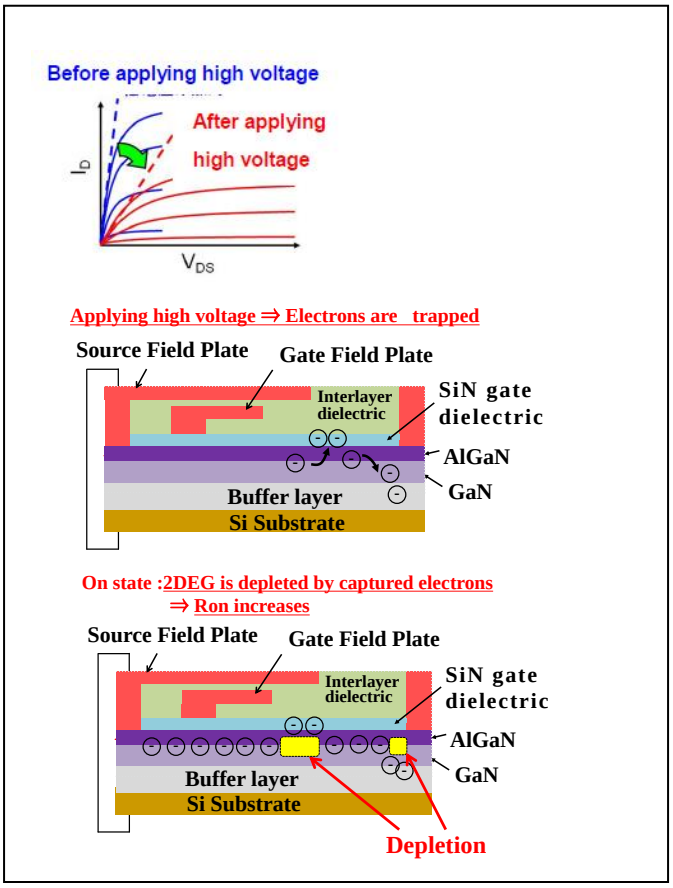

Figure 1. Mechanism of current collapse.

III. Measurement Methods of C/C

We propose two methods of measurement of the C/C. The first is a method using DC voltage stress (Fig. 3a,b); the second is a method using inductance (L) load switching stress (Fig. 4a,b). Because the first may be performed on wafers, it is possible to measure many devices at once as the device temperature does not rise significantly in practice. However, it is different from the operating condition of the actual

application. In contrast, the second method of evaluation is close to the actual applications and represents a situation of severe stress when current and voltage are simultaneously applied (Fig. 4b). This method (L-load or hard-switching) generates hot electrons, as shown by simulations in ref [5]. Hot electrons will reach traps deeper in both the buffer layer and dielectrics than DC off-state stress. More trapped charge will cause more dynamic R_{on} degradation. Also, it is necessary to consider the increase in R_{on} arising from an elevated device temperature.

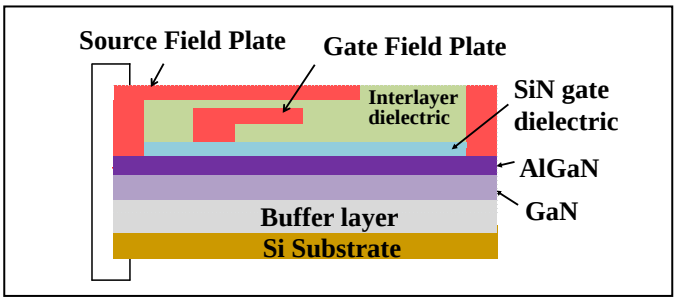

Figure 2. Schematic cross section of a typical HEMT device.

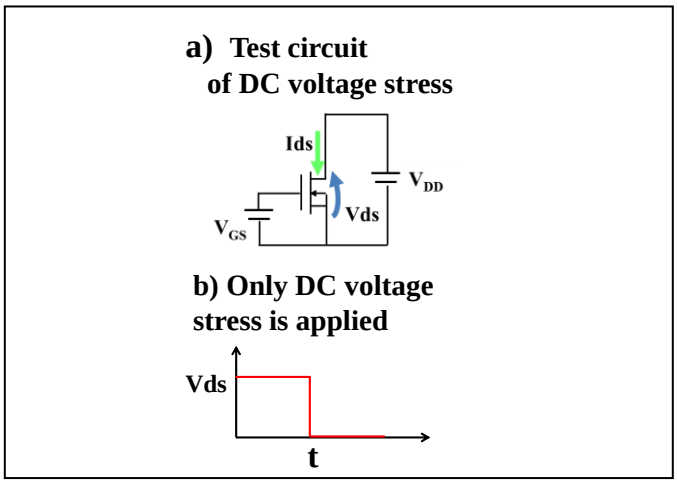

Figure 3. Measurement methods for C/C. a) Test circuit of DC voltage stress, b) Wave form of DC stress.

IV. CURRENT COLLAPSE TEST METHOD EVALUATING ON-RESISTANCE UNDER DC VOLTAGE STRESS

In this test, DC voltage stress is applied between the drain and the source in the off state, and the change in R_{on} before and after applying the stress is measured (Fig. 5a,b). After the initial R_{on} is measured, DC voltage stress during time t_1 is applied between the drain and source while the gate is in the off state. R_{on} is measured after a time period t_2 (Fig. 5b). In this way, the increasing rate of change in R_{on} before and after DC voltage stress is derived. When the period t_2 is too short, electron trapping is insufficient to cause but a small increase in R_{on}. When the period t_2 becomes long, electrons are released and R_{on} decreases. This time response depends on the level of trapping. Jin et al. have assessed this level from the time response as a function of temperature [6].

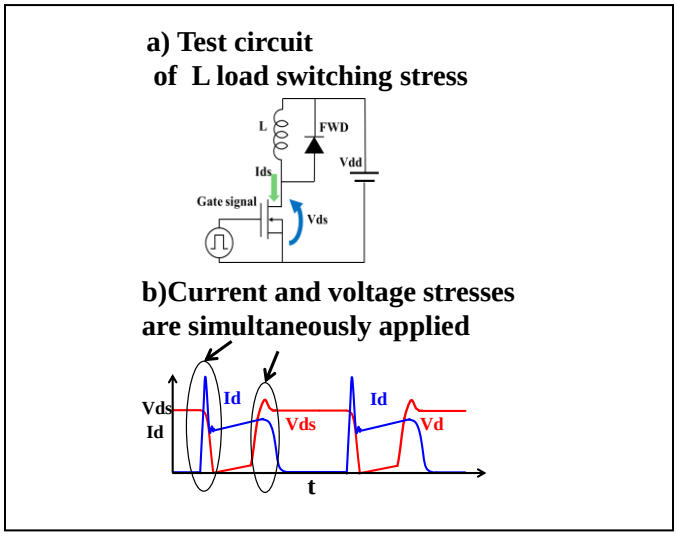

Figure 4. a) Test circuit of L load switching stress, b) Wave form of L load switching.

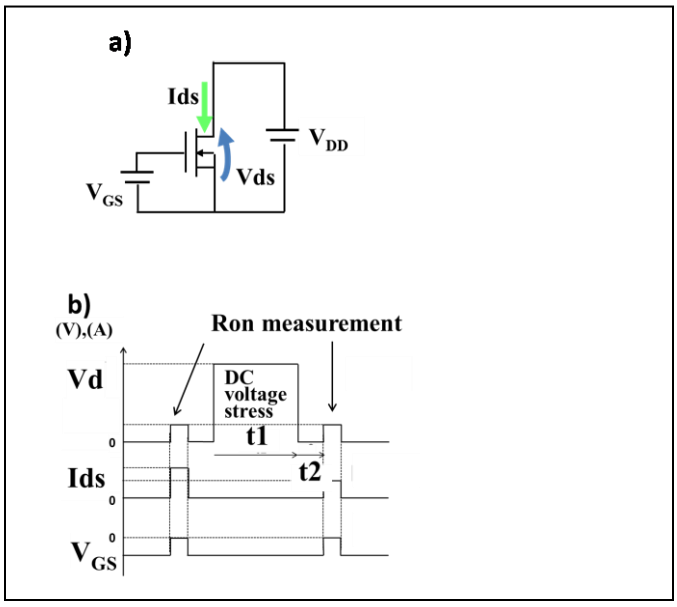

Figure 5. Test method by DC voltage stress. a) Test circuit, b) Timing chart for DC voltage stress test.

Fig. 6 shows the results of the evaluation of C/C using DC voltage stress. In this measurement, t1 and t2 are 30s and 1s, respectively. In subsequent measurements, the backside of the substrate is connected to the source. The results obtained are for samples with a) different Field Plate(FP) structures on the same epitaxial wafer and b) the same FP structure with different epitaxial conditions and structures. The FP structure, the epitaxial structure and the epitaxial

condition dependence of the current collapse were shown. In Fig. 5b, no difference in C/C is observed under low voltages, but under high voltages, a difference in the epitaxial conditions can be seen. Because, under a high electric field, the depletion layer reaches the drain, the vertical electric field at the drain edge is stronger. In this way, we were able to check the quality of epitaxial structures and the surface process using DC voltage stress.

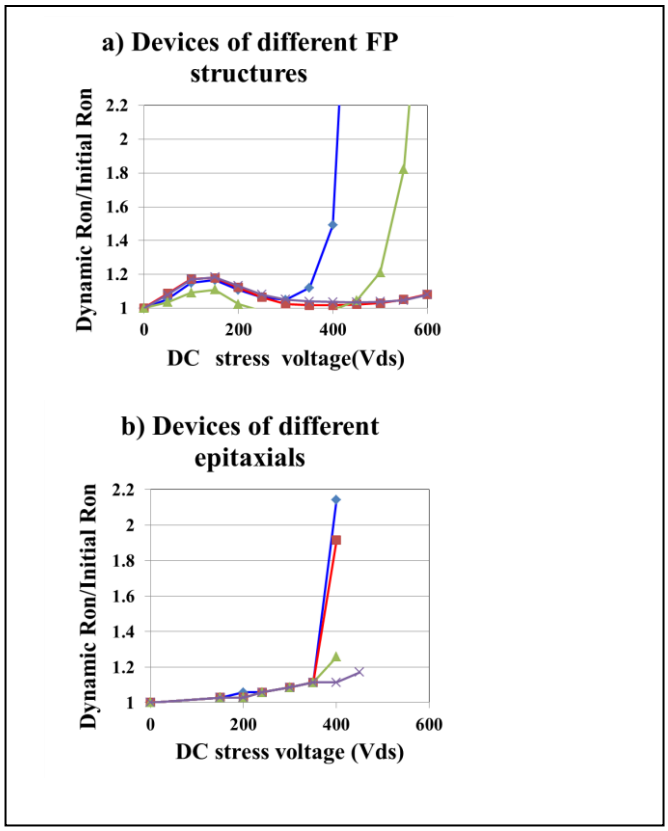

Figure 6. Device dependence of C/C by DC voltage stress. a) Devices of different FP structures were measured. b) Devices of different epitaxial structures and conditions were measured.

However, even though the results of DC voltage stress were good, there were defective samples detected only using the *L* load switching test (Fig. 7). Our finding is consistent with other reports in the literature, where hard-switching was shown to cause more dynamic R_{on} degradation than soft-switching [1, 7].

V. Current Collapse Test Method Evaluating On-Resistance under *L* Load Switching

In this test, the increase in R_{on} during hard switching with *L* loading is evaluated [8].

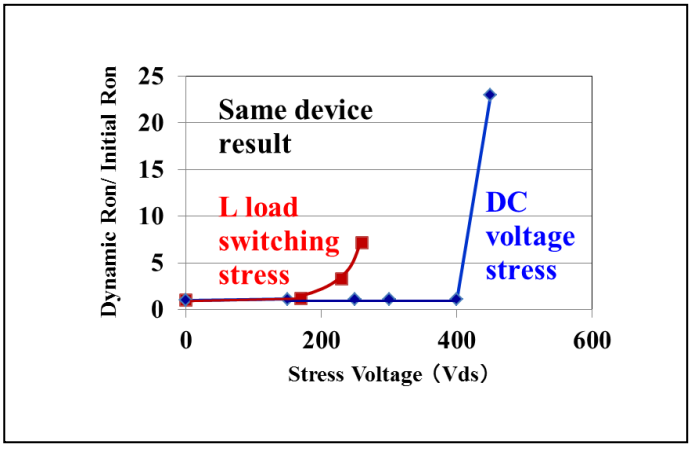

Figure 7. Comparison of DC voltage stress and L load switching stress for the same device. These are cases where defective devices cannot be inspected by the DC stress test alone.

A. *On-resistance measurement during L load switching*

The C/C is caused by not only the drain-source voltage V_{ds} but also the current I_{ds} under *L* load switching. The C/C is evaluated from the ratio of the initial R_{on} and post-test R_{on} (Fig. 8).

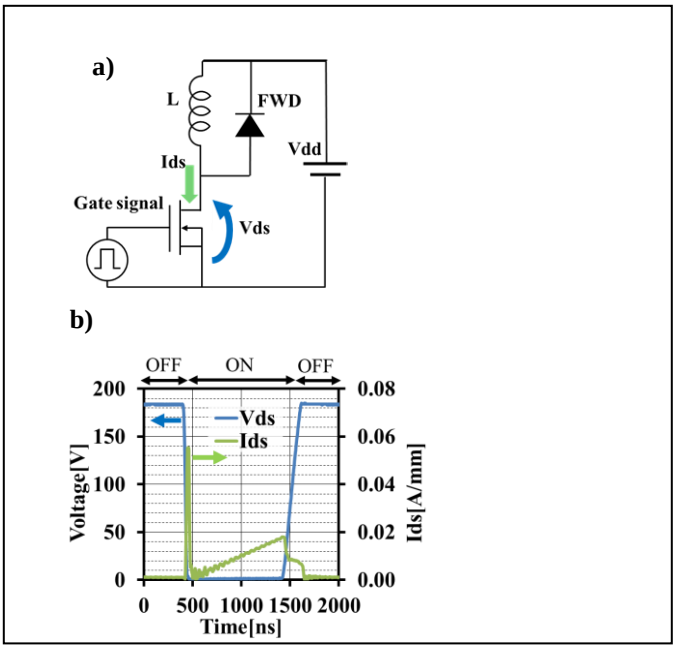

Figure 8. Test method using *L* load switching. a) Test circuit. b) Example waveform of *L* load switching.

Because severe C/C occurs when high voltage and high current are applied at the same time, *L* load switching becomes more severe than when only DC voltage stress is applied. Also, the *L* load switching condition is close to actual applications. As C/C depends on the applied voltage

[3,8], the test condition is based on the driving voltage assumed by the application and the rated voltage.

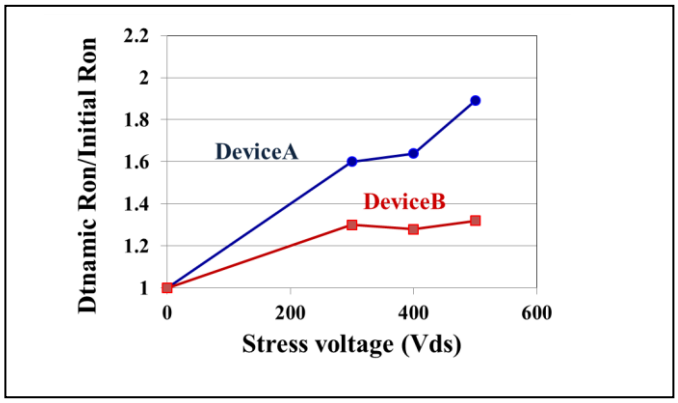

Figure 9. Results of *L* load switching for two devices with different epitaxial structures and surface processes.

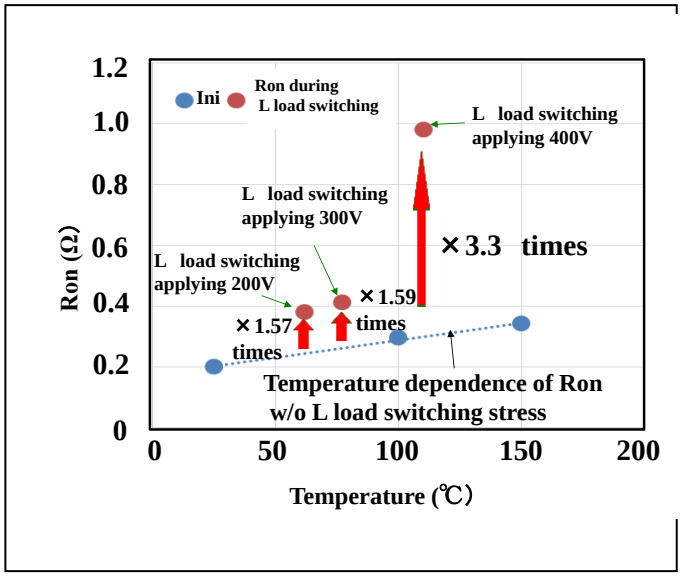

Figure 10. Temperature dependence of R_{on}. The actual rate of increase in R_{on} because of C/C needs the temperature dependence to be considered.

Fig. 9 shows the switching voltage dependence of C/C using the *L* load switching method. The switching frequency is 10kHz, drain current is 3A. The results of two devices are shown in which the epitaxial structure and the surface process are different. In contrast, R_{on} depends on the temperature, so it is necessary to evaluate the device temperature during the operation and correct R_{on} by considering this temperature dependence (blue line in Fig. 10). At 400V switching, R_{on} increases from the initial value of 0.2 Ω to 1.0 Ω, so the rate of increase in R_{on} was 5-fold. However, considering that the device temperature rises to 120°C, the rate of increase because of C/C was considered to be 3.3 times.

B. Direct measurement of carrier number

Mobility depends strongly on the temperature whereas carrier number has a weak dependence [9]. We focused on carrier number to evaluate C/C. Direct measurements of the carrier number are possible using the capacitance measurement technique [10, 11]. Changes in capacitance of the GaN HEMT devices are related to carrier depletion in the 2DEG. As drain voltage increases, the depletion region expands toward the drain direction from the gate edge. The dual field plate (FP) structure (Fig. 2) leads to a two-step change in capacitance, which is related to the depletion of the 2DEG under the gate-FP and source-FP, respectively (Fig. 11).

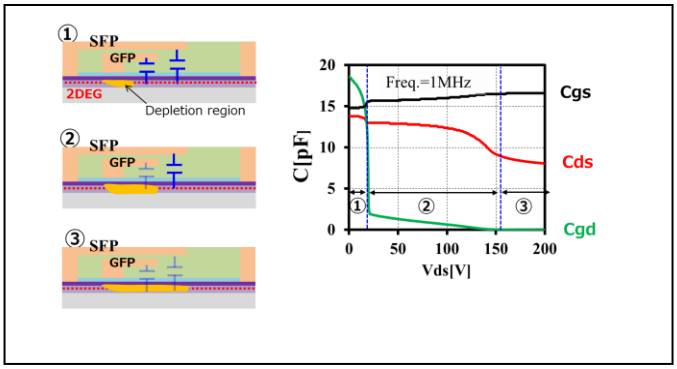

Figure 11. Capacitance measurement for C/C. Because the depletion under the field plate appears in the capacitor, capacitance indicates carrier number and its position.

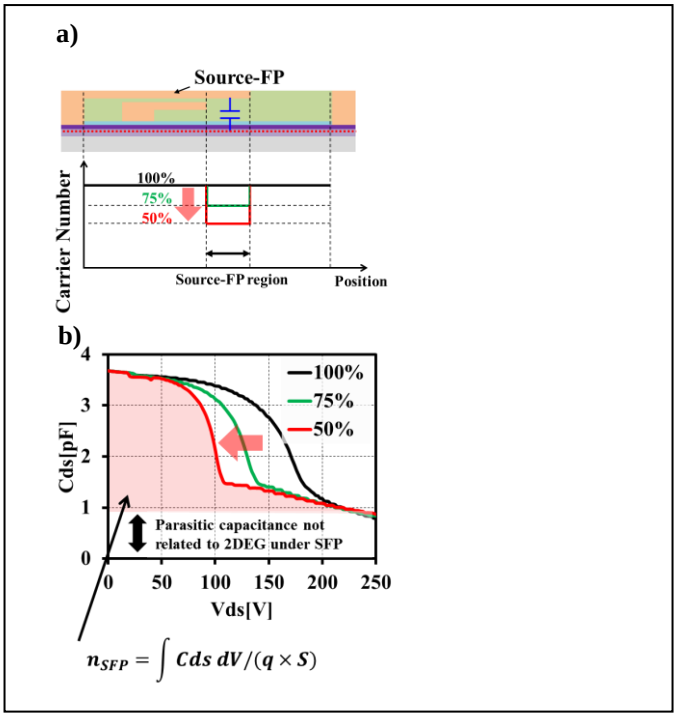

Figure 12. a) Simulated model. b) Simulated C_{ds} results. Carrier number under the source-FP decreases as indicated in a), its impact C_{ds} is seen in b).

The large change in capacitance C_{ds} after L load switching indicates the decrease in the 2DEG under the source-FP as determined from the capacitance relation $Q=CV$. Simulations have been performed (Fig. 12). When the electron number in the 2DEG under the source-FP decreases, the depletion voltage for C_{ds} becomes smaller. The sheet carrier density(n_s) under the FP can be derived using $n_s=\int C(V)dV/(q\times S)$ where S is the area of the FP. A strong correlation is observed between R_{on} and $\int C(V)dV$ after L load switching (Fig. 13) [11]. Hence the direct measurement method for the carrier number is useful to evaluate the C/C phenomenon excluding self-heating effects.

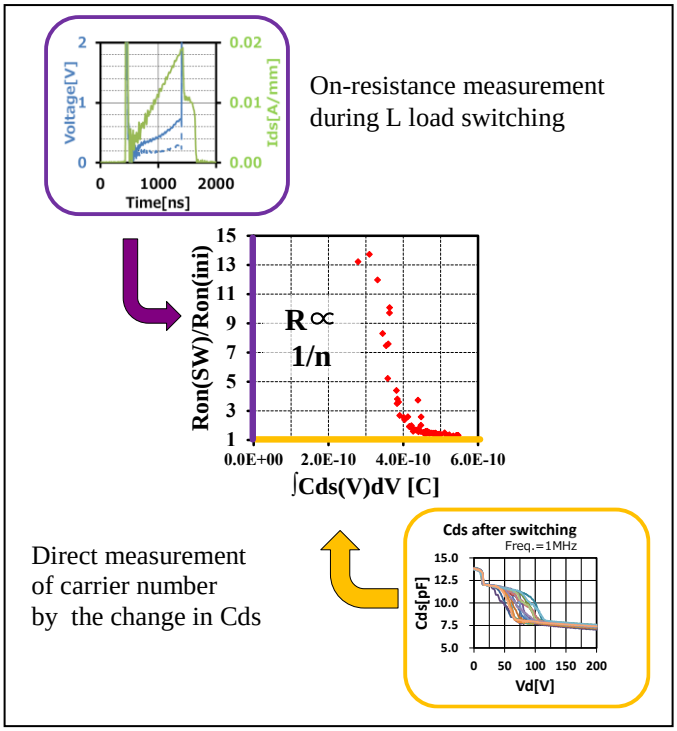

Figure 13. Comparison between the conventional R_{on} ratio and the direct measurement of the carier number.

VI. Conclusion

We proposed, as a guideline, methods of evaluation and analysis of C/C in GaN HEMTs. The stress voltage must be determined by the device application because the C/C depends on voltage. In the first step, the DC stress test is effective in evaluating many devices at once and provides the quality of epitaxial structure and the surface process. In the second step, the L load switching test imposing a severe condition than just the DC voltage stress is required because this condition is close to that of actual applications. It is that if the device passes the harsher test, namely L load switching test, it will also cover the case of the more mild tests. Moreover, if the device passes L load switching test, then it will be good for both hard and soft-switching applications. The new method of evaluation using the FP capacitance measurements is useful in determining the location and carrier number in a 2DEG layer during C/C.

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