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Cu Double Side Plating Technology for High Performance and Reliable Si Power Devices

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***Abstract*— In this work, we have developed vertical Si power MOSFETs with high performance and high reliability by using Cu double side plating technology. 20 µm thick Cu plating layers are formed on both sides of devices with 50 µm thick Si substrate. In this structure, even though Si substrate is thinner, Safety Operating Area (SOA) is wider and the warpage of chip is smaller thanks to front and back side Cu plating layers.**

Keywords—Cu, Double side, plating, warpage, SOA, Ron

I. INTRODUCTION

In order to realize lower on-resistance (Ron) of vertical Si power MOSFETs [1,2], thinner Si substrate is desirable to reduce the Si substrate resistance [3,4]. Safety operating area (SOA) [5-9], however, degrades due to lower heat content and warpage of chip becomes larger. So, it was required to introduce a novel technology to achieve both lower Ron and wider SOA with small warpage of chips. In this paper, Cu double side plating process with thinner Si substrate is introduced as a novel technology.

II. SAMPLE FABRICATION

As shown in Fig. 1 we have developed Cu double side plating structure [10,11]. This consists of 20 µm thick Cu plating layers on both sides of devices with 50 µm thick Si substrate.

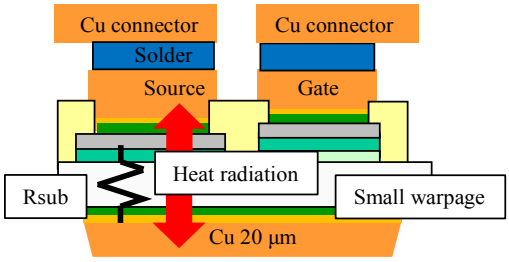


Fig. 1 The effect of vertical Si power MOSFETs with thin Si substrate and Cu double side plating.

Fig. 2 shows the estimation of wafer warpage for various Si substrate and Cu plate thickness. In the case of double side plating with the same Cu thickness, the warpage becomes significantly small. Then we have considered simultaneous both sides Cu plating to prevent wafer warpage caused by thick Cu film stress. And also as means of suppression of thinner wafer warpage, backside grinding for wafer thinning is provided only inner side of Si wafer and the rim region of Si wafer remains thick. This structure enables simultaneous both sides plating because there're no support materials on silicon surfaces for maintaining wafer strength. Thus simultaneous both side Cu plating on thinner substrate is accomplished.

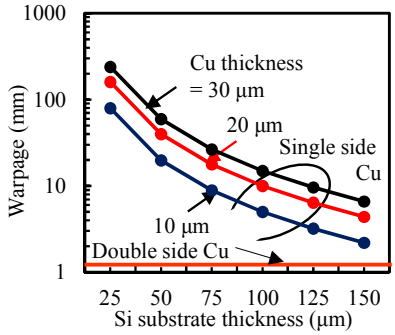


Fig. 2 The estimation of wafer warpage for various Si substrate and Cu plate thickness.

- MOSFETs formation for power device
- Backside grinding for wafer thinning
- Patterning for front side Cu plate
- Cu plating on both sides of Si wafer
- Patterning and etching off back side Cu film on dicing line
- Dicing and assembly

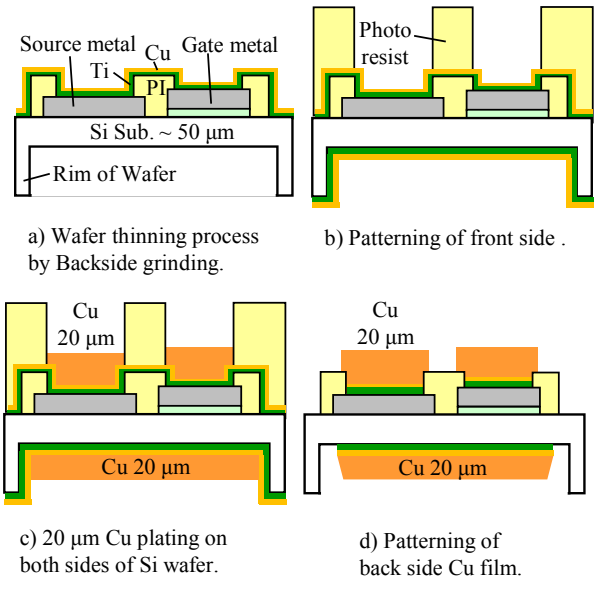


Fig. 3 Process flow of Cu double side plating for vertical Si power MOSFETs.

Fig. 3 shows process flow of Cu double side plating. After formation of MOSFETs, wafer thinning by backside grinding

down to 50 µm is processed. Then, lithography process on front side is performed for Cu electroplating. It is ideal to process both sides patterning before simultaneous electroplating, but such a both sides lithography is difficult from the point of handling. Therefore front side patterning is processed at first. After that simultaneous both sides Cu plating is done by double side plating equipment. The thickness of both plates is about 20 µm. After that back side patterning is processed in order to get rid of Cu plates in dicing region.

To implement above process flow, both sides lithography and electroplating are the key points. Features of those processes in this fabrication are shown as below.

A. Requirements for patterning process

As stated above, back side surface of the thinning wafer has a rim structure. So front side lithography must be processed without touching with the rim as shown in Fig. 3-b). Therefore stage structure of exposure equipment must be compatible to rim part. Also in case of back side patterning it is necessary to align with front side patterning. And exposure equipment must be able to see front side alignment mark facing exposure stage because there are no alignment mark on back side of Si wafer. And also thick Cu plating has already been formed on back side surface. Therefore it is difficult to see front side alignment mark by infrared from upward of exposure equipment. So we'd have to see front side alignment mark facing exposure stage from downward of stage. An adopted exposure machine in this fabrication is MEMS Stepper NES2W-i06 (Nikon Engineering). This machine meets above requirements.

B. Requirements for Cu plating process

Another process point for this fabrication is double side electroplating. To suppress wafer warpage due to Cu film stress it is necessary to be able to process simultaneous both sides plating and also it is desirable to be able to adjust plating thickness on each side of wafer surface. Thereby we can control wafer warpage due to different surface coverage of Cu plates on each side. And also electroplating equipment is required to be compatible to thinner wafer, for example gentle handling, little damage wafer drying like IPA drying (Maragoni drying). An adopted Cu plating equipment in this fabrication is Multiplate (Atotech). This equipment meets above requirements.

Fig. 4 shows the cross-sectional view of the device with double side Cu plating fabricated by our introduced process flow. As shown Fig. 4 about 20 µm thickness Cu plates are formed on both sides of thinner wafer which is about 50 µm thickness.

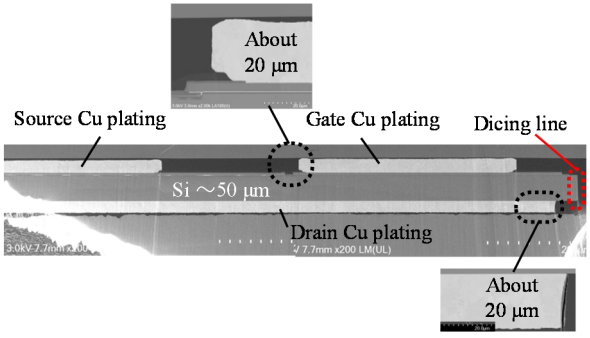


Fig. 4 The cross-sectional view of Si power MOS device with double side Cu plating. The thickness of both front and back is about 20 µm.

III. RESULTS AND DISCUSSION

A. Warpage suppression of the chip

Fig. 5-a) shows temperature dependences of chip warpage with single side and double side Cu plating, comparing to a chip with conventional metal. In single side Cu plating and conventional metal cases, the warpage becomes larger toward convex upward with increasing temperature from 50 to 360 degrees and that becomes smaller toward convex downward with decreasing from 360 to 70 degrees because the stress and thermal expansion are not equivalent. On the other hand, the warpage is extremely small and no dependence of temperature in double side Cu plates case thanks to good stress balance. Fig. 5-b) shows the temperature dependence of warpage when the front side and back side Cu plate thickness are 20 and 10 µm, 10 and 20 µm. In the case of different Cu plate thickness for front and back sides, the warpage has dependence on temperature which is almost same as single side Cu plate case. These results show the controllability of Cu plate thickness is important to suppress the warpage during thermal process.

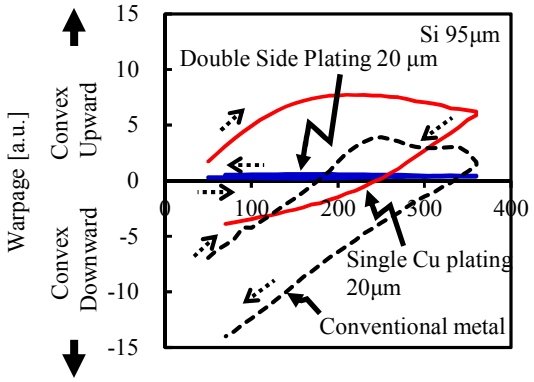


Fig. 5-a) Temperature dependence of warpage with single side and double side Cu plating.

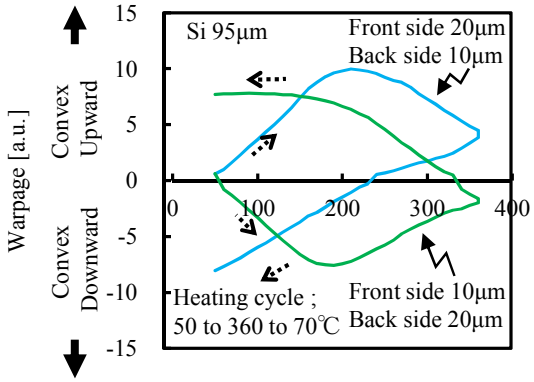


Fig. 5-b) Temperature dependence of warpage when the front side and back side are 20 and 10 µm, 10 and 20 µm.

Fig. 5-c) shows the X-ray observation of chip at 350 and 150 degrees for single Cu plate and double side Cu plating. The larger voids in solder layer are observed in single Cu plate case because of the chip with larger warpage. It is important to reduce the void for wider SOA because the voids are smaller thermal conductivity (0.02 W/m•k). In the double side Cu plates structure, the voids become smaller thanks to smaller warpage.

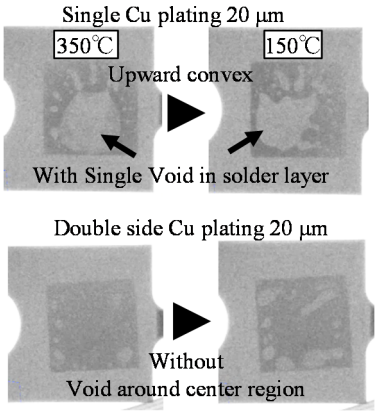


Fig. 5-c) X-ray observation of chip at 350 and 150 degrees for single Cu plate and double side Cu plating.

B. *Superior on-resistance (Ron)*

Fig. 6 shows the resistance ratio of some elements related to Ron of vertical 40 V Si power MOSFETs. The thinning of Si substrate has a great role for lower Ron because the ratio of Si substrate is about 25 %. The Ron is decreased by 10 % by thinning Si substrate from 95 μm to 50 μm as shown in Fig. 7. Superior Ron in Si 50 μm and Cu 20 μm is obtained comparing to that in Si 95 μm and no Cu plate. This result is good agreement with our estimation as shown in Fig. 7.

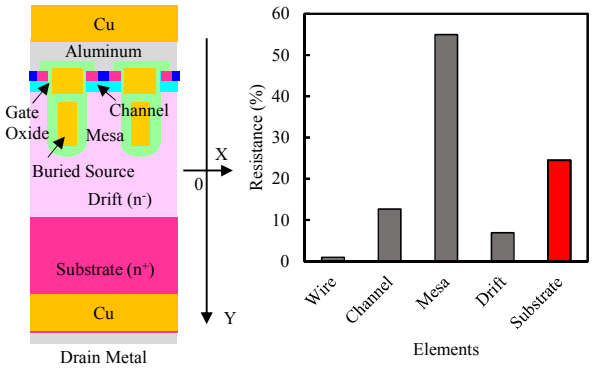


Fig. 6 The resistance ratio of some elements related to on-resistance (Ron) of vertical 40V Si power MOSFETs with buried source.

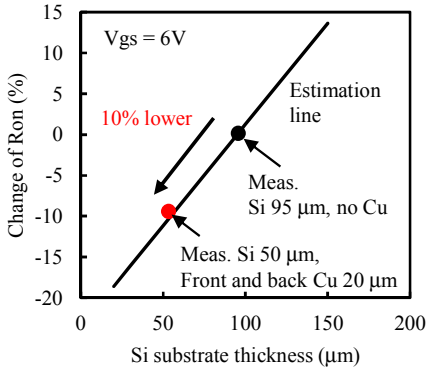


Fig. 7 The comparison of on-resistance between Si power MOSFETs with Si 95 μm and no Cu, and Si 50 μm and 20 μm Cu plate on both sides. The estimation line is calculated by the ratio as shown in Fig. 6.

C. *Improvement of Safety operating area (SOA)*

As shown in Fig. 8, in order to evaluate SOA, the change of forward-bias at drain before and after power applying is observed when Ids is a fixed value [12]. The operating time (Tpulse) is 100 μs. The Ids is controlled by gate bias.

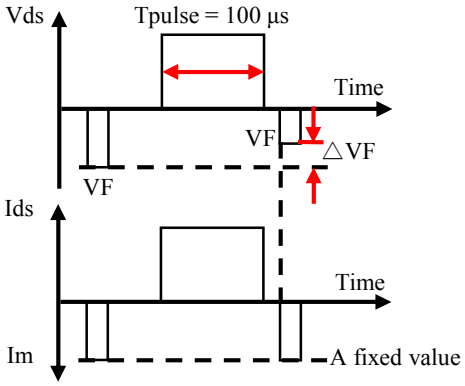
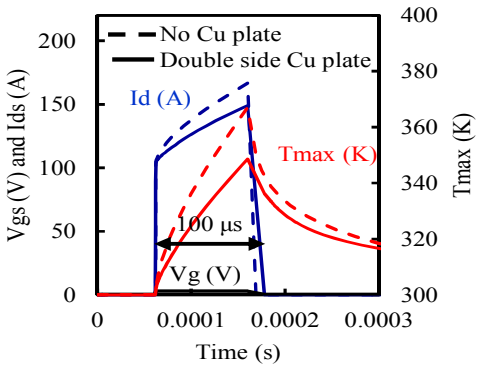
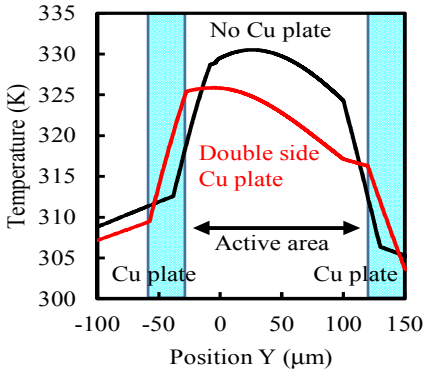


Fig. 8 Procedure of SOA evaluation.

Fig. 9-a) shows the simulation result of time dependence of the maximum temperature and Fig. 9-b) shows temperature profile in the device with and without double side Cu film. In this simulation, Id and Tmax are calculated at a fixed Vg. Id increases with temperature because the Vth decreases. That of active area with double side Cu plating becomes lower compared with no Cu plate structure after power applying because thicker Cu plate has larger heat content. Accordingly, SOA has been improved as below. Fig. 10-a) shows the definition of SOA in our experiments. The SOA is defined as Id when a fixed value in ΔVF becomes larger than the reference line. Fig. 10-b) shows the ratio of SOA (ΔId/Id1) of devices with and without double side Cu film. That becomes larger with increasing of Vds. As a result, 100 % larger SOA at Vds = 32 V is observed thanks to 20 μm Cu plate with larger heat content.

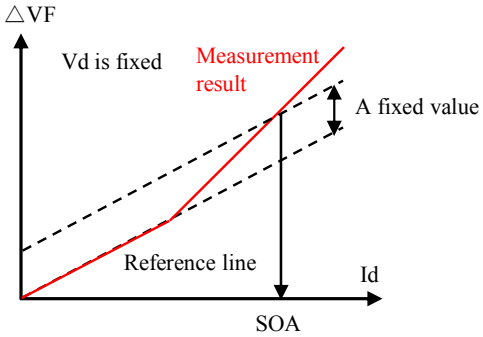


a) Time dependence of the maximum temperature.

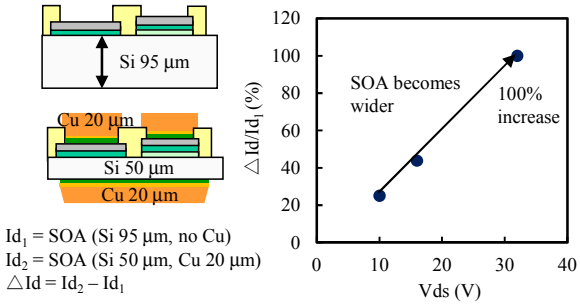


b) Temperature profile in the device.

Fig. 9 The simulation results of temperature with and without double side Cu film.



a) Definition of SOA in our experiments.



b) The results of SOA with and without double side Cu film.

Fig. 10 Definition and the results of SOA.

IV. CONCLUSION

The double side Cu plating technology is introduced to Si power MOSFET with thin Si substrate for the first time. This structure has lower on-resistance (Ron) by decrease of substrate resistance, wider safety operating area (SOA) by larger heat content of thicker Cu plate. Additionally larger warpage and larger void in solder layer can be suppressed by double side Cu film.

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