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High Performance and Reliable Si Power Devices with double side Cu plate

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ABSTRACT: In this work, we have developed vertical Si power MOSFETs with high performance and high reliability by using Cu double side plating technology. 20 μm thick Cu plating layers are formed on both sides of devices with 50 μm thick Si substrate. In this structure, even though Si substrate is thinner, Safety Operating Area (SOA) is wider and the warpage of chip is smaller thanks to front and back side thick Cu plating layers because thick Cu film has higher thermal conductivity and larger heat capacity.

KEY WORDS: Cu, Double side, plating, warpage, SOA, Ron

1. INTRODUCTION

In order to realize lower on-resistance (Ron) of vertical Si power MOSFETs [1,2], thinner Si substrate is desirable to reduce the Si substrate resistance [3,4]. Safety operating area (SOA) [5-9], however, degrades due to smaller heat capacity and warpage of chip becomes larger. So, it was required to introduce a novel technology to achieve both lower Ron and wider SOA with small warpage of chips.

2. SAMPLE FABRICATION

As shown in Fig. 1 we have developed Cu double side plating structure [10-12]. This consists of 20 μm thick Cu plating layers on both sides of devices with 50 μm thick Si substrate.

Fig. 2 shows process flow of Cu double side plating. After formation of MOSFETs with Al electrode for source and gate, wafer thinning by backside grinding down to 50 μm is processed (fig.2-a). Then Ti and Cu sputtering are carried out for front and back sides (fig.2-b) and lithography process on front side is performed for Cu electroplating (fig.2-c). It is ideal to process both sides patterning before simultaneous electroplating, but such a both sides lithography is difficult from the point of handling. Therefore, front side patterning is processed at first. After that, simultaneous both sides Cu plating is done by double side plating equipment (fig. 2-d). The thickness of both plates is about 20 μm. After that back side patterning is processed in order to get rid of Cu plates in dicing region (fig.2-e).

To implement above process flow, both sides lithography and electroplating are the key points. Features of those processes in this fabrication are shown as below.

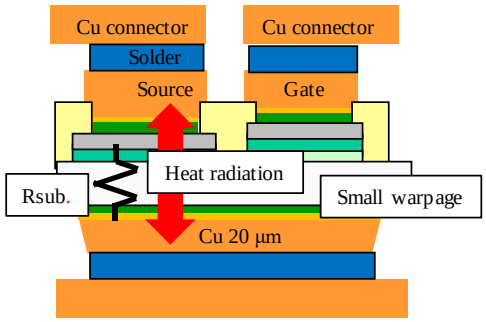


Fig. 1 The effect of vertical Si power MOSFETs with thin Si substrate and Cu double side plating.

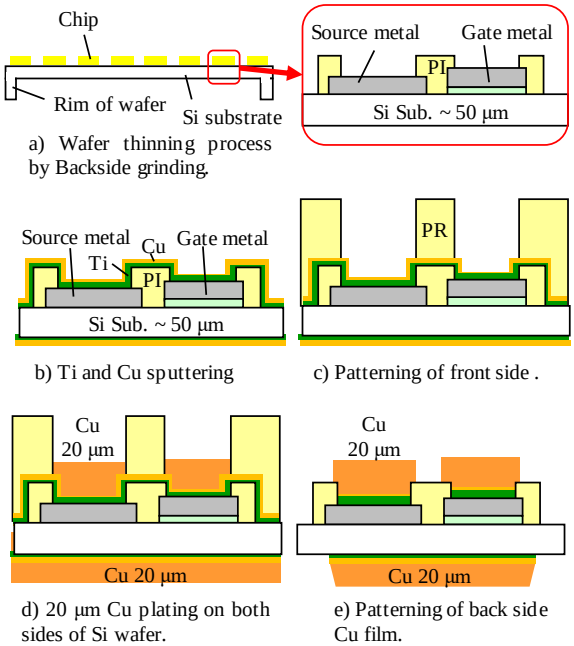


Fig. 2 Process flow of Cu double side plating for vertical Si power MOSFETs

A. Requirements for patterning process

As stated above, back side surface of the thinning wafer has a rim structure. So front side lithography must be processed with downward rim structure as shown in Fig. 2-a). Therefore, stage structure of exposure equipment must be compatible to rim part. Also in case of back side patterning it is necessary to align with front side patterning. And exposure equipment must be able to see front side alignment mark facing exposure stage because there are no alignment marks on back side of Si wafer. And also thick Cu plating has already been formed on back side surface. Therefore, it is difficult to see front side alignment marks by infrared from upward of exposure equipment. So we'd have to see front side alignment mark facing exposure stage from downward of stage. A special exposure machine to meet the requirements is used in our fabrication.

B. Requirements for Cu plating process

Another process point for this fabrication is double side electroplating. To suppress wafer warpage due to Cu film stress it is necessary to be able to process simultaneous both sides plating and also it is desirable to be able to adjust plating thickness on each side of wafer surface. Thereby we can control wafer warpage due to different surface coverage of Cu plates on each side. And also electroplating equipment is required to be compatible to thinner wafer, for example gentle handling, little damage wafer drying like IPA drying (Maragoni drying). An adopted Cu plating equipment in this fabrication is multi plate. This equipment meets above requirements.

Fig. 3 shows the cross-sectional view of the device with double side thick Cu plating fabricated by our introduced process flow. As shown Fig. 3 about 20 μm thickness Cu plates are formed on both sides of thinner Si wafer which is about 50 μm thickness.

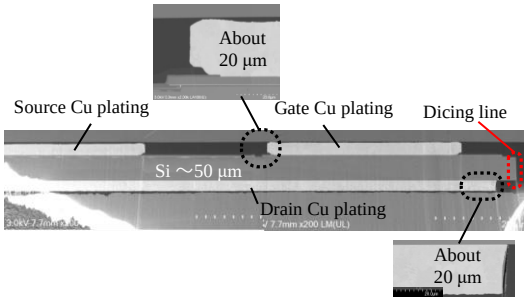


Fig. 3 The cross-sectional view of Si power MOS device with double side Cu plating. The thickness of both front and back is about 20 μm.

3. RESULTS AND DISCUSSIONS

A. Warpage suppression of the chip

Fig. 4 shows temperature dependences of chip warpage with single side and double side Cu plating, comparing to a chip with conventional metal. In single side Cu plating and conventional metal cases, the warpage becomes larger toward convex upward with increasing temperature from 50 to 360 degrees and that becomes smaller toward convex downward with decreasing from 360 to 70 degrees because the stress and thermal expansion are not equivalent. On the other hand, the warpage is extremely smaller and no dependence of temperature in double side Cu plates case thanks to the good stress and thermal expansion balance.

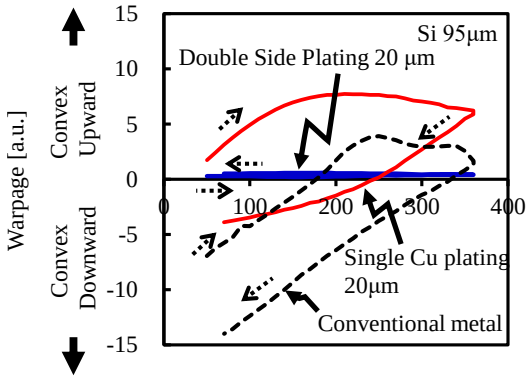


Fig. 4 Temperature dependence of warpage with single side and double side Cu plating.

B. Superior on-resistance (Ron)

Fig. 5 shows the resistance ratio of some elements related to Ron of vertical 40 V Si power MOSFETs. Though the reduction of the resistivity in the mesa region is the most important, the thinning of Si substrate has also a great role for lower Ron because the ratio of Si substrate is about 25 %. Fig.6 shows the change of Ron (%) calculated by measurement results of our

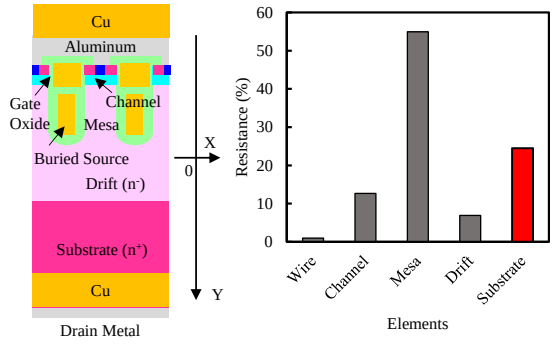


Fig. 5 The resistance ratio of some elements related to on-resistance (Ron) of vertical 40V Si power MOSFETs with buried source.

samples. The Ron is decreased by 10 % by thinning Si substrate from 95 μm to 50 μm. Superior Ron in Si 50 μm and Cu 20 μm is obtained comparing to that in Si 95 μm and no Cu plate. This result is good agreement with our estimation as shown in Fig. 5 and 6.

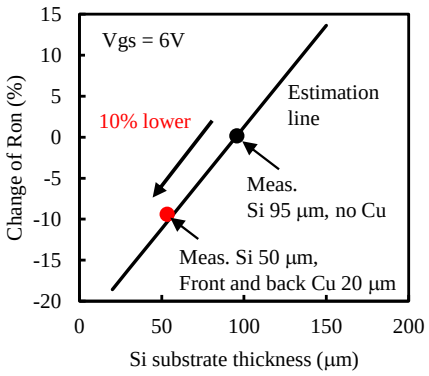


Fig. 6 The comparison of on-resistance between Si power MOSFETs with Si 95 μm and no Cu, and Si 50 μm and 20 μm Cu plate on both sides. The estimation line is calculated by the ratio as shown in Fig. 5.

C. Improvement of Safety operating area (SOA)

As shown in Fig. 7, in order to evaluate SOA, the change of forward-bias at drain before and after power applying are observed when Ids is a fixed value (Im) [13].

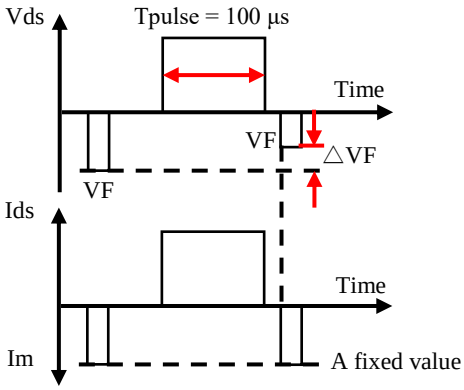


Fig. 7 In order to evaluate SOA, the change of forward-bias at drain when Ids is a fixed value is observed before and after power applying. The operating time (Tpulse) is 100 μs. The Ids is controlled by gate bias.

Fig. 8 shows the simulation results of temperature profile in the device with and without double side 20μm Cu film after one pulse (100μs) operation. The maximum temperature (T_{MAX}) of active area with the double side Cu plate becomes lower compared with no Cu plate structure because thick Cu film has higher thermal conductivity and larger heat capacity. Accordingly, SOA has been improved as below. Fig. 9 shows the ratio of SOA (△Id/Id1) of devices with and without double side 20μm Cu film. That becomes larger with increasing of Vds and 100 % larger SOA at Vds = 32 V is observed.

Fig. 10 shows the one pulse time dependence of the T_{MAX} calculated by simulation for these samples. The temperature

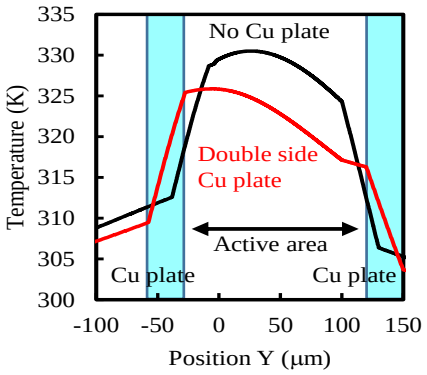
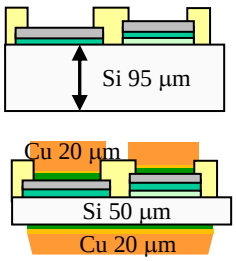


Fig. 8 The simulation results of temperature profile in the device with and without double side Cu film.



Id_1 = SOA (Si 95 μm, no Cu)
Id_2 = SOA (Si 50 μm, Cu 20 μm)
$\triangle Id = Id_2 - Id_1$

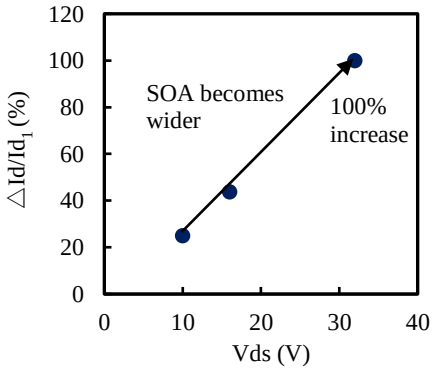


Fig. 9 The results of SOA with and without double side Cu film. The ratio of SOA ($\triangle Id/Id_1$) becomes larger with increasing of Vds. 100 % larger SOA at Vds = 32V is observed thanks to 20μm Cu plate with larger heat capacity.

difference of the T_{MAX} between with and without Cu plate becomes larger as the time becomes shorter because the thicker Cu has a great role to suppress temperature increase as the power occurred during device operation becomes lower. These results show the effectiveness of double side thicker Cu plating technology is significant for short pulse operation in order to wider SOA.

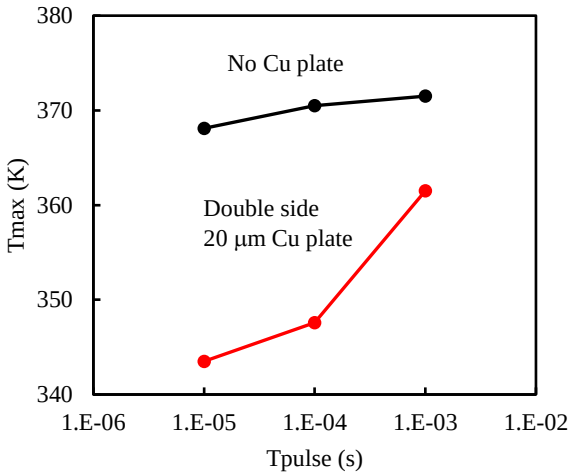


Fig. 10 The one pulse time dependence of the T_{MAX} for samples with and without double side 20 μm Cu plate.

4. CONCLUSIONS

The double side Cu plating technology is introduced to Si power MOSFET with thin Si substrate. This structure has lower on-resistance (Ron) by decrease of substrate resistance, wider safety operating area (SOA) by larger heat capacity of thicker Cu plate. The temperature difference in the device after one pulse operation between with and without Cu plate becomes larger as the pulse time is shorter because thicker Cu plate has larger heat capacity.

Additionally, larger warpage and larger void in solder layer can be suppressed by double side Cu film. Bias test results shows the no degradation in Si power MOSFET performance occurs by double side Cu plating.

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