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Gate drive techniques of Gate-connected Trench Field Plate Power MOSFETs to reduce both switching and conduction losses

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***Abstract*— We proposed new gate drive techniques of Gate-connected Trench Field Plate (Gate FP) Power MOSFETs. Compared with a Source-connected Trench Field Plate (Source FP) device, the Gate FP is hardly used for high speed switching applications because large feedback capacitance (Crss) prevents high speed Turn-ON / OFF and causes shoot-through. We propose gate driving method which realizes pseudo independent Gate and FP driving by using a conventional gate driver with small number of additional components. The concept was verified by TCAD mixed-mode simulation. The results demonstrated the proposed method showed almost as the same switching performance as the Source FP and suppressed shoot-through successfully.**

Keywords—Trench Field Plate MOSFET, Gate-connected FP, Gate FP, Buried-Gate, Gate driving technique, shoot-through

I. INTRODUCTION

Since Trench Field Plate or Split Gate [1] Power MOSFETs were invented, On-resistance of these devices have been reduced drastically by increasing of cell density (reducing cell pitch). Regarding the Split Gate structure, which has a Gate and a buried FP electrode in its trench, two connection types of a buried FP electrodes are known, namely, Source-connected FP (Source FP) and Gate-connected FP (Gate FP) as illustrated in Fig. 1. The Gate FP connection, which include united Gate and FP electrode (one electrode in the trench) [2], can further reduce drift layer resistance compared with the Source FP by accumulation effect of the Gate FP (Fig. 2). However, it is believed that the Gate FP structure is hardly used for high speed switching applications because large feedback capacitance (C_{rss}) prevents high speed Turn-ON / OFF as shown in Fig. 3. This causes large switching loss as we can see from loss analysis in Fig. 4 and induces shoot-through phenomena [3] . In order to overcome this difficulties, the independent driving of the Gate and the Gate FP was discussed [4]. In addition, some double Gate driving method are demonstrated especially in IGBTs [5-7]. However, this independent driving of these two electrodes needs dedicated gate drivers and controllers. In this study, we propose simple and low switching loss driving techniques of the Gate and the Gate FP, which are expected to be driven by conventional gate drivers.

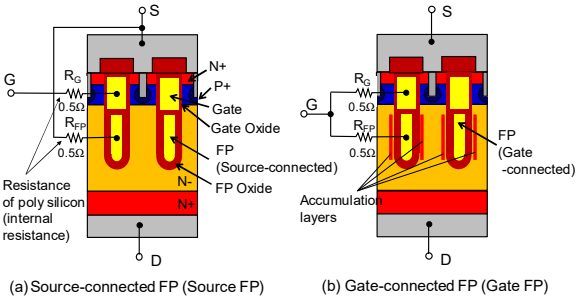

Fig. 1. Conventional gate connection variations of Trench Field Plate power MOSFET. The Gate resistance (R_G) and the FP resistance (R_{FP}) originate from resistance of poly silicon.

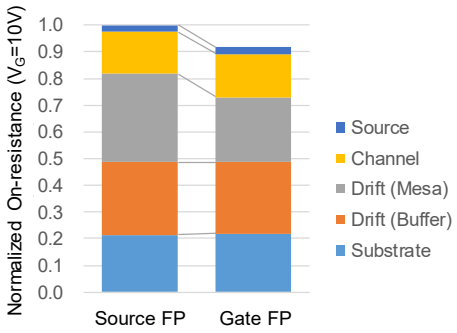

Fig. 2: On-resistance comparison between the Source FP and the Gate FP of 40V class.

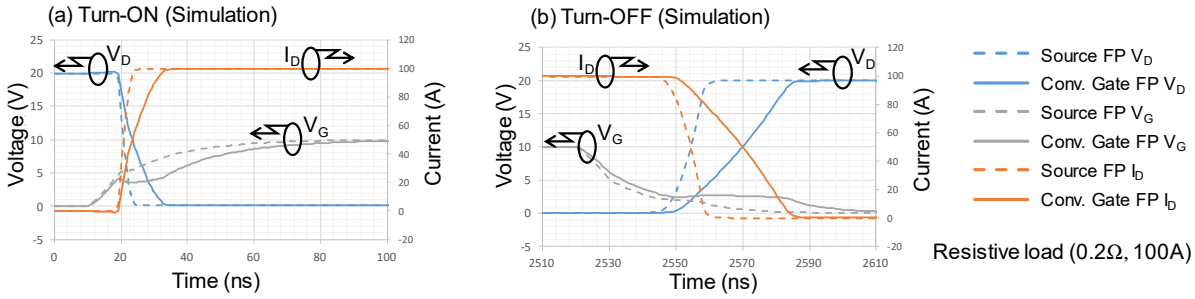

Fig. 3. Simulated Turn-ON / Turn-OFF waveforms comparison between the Source FP (dashed lines) and the conventional Gate FP (solid lines).

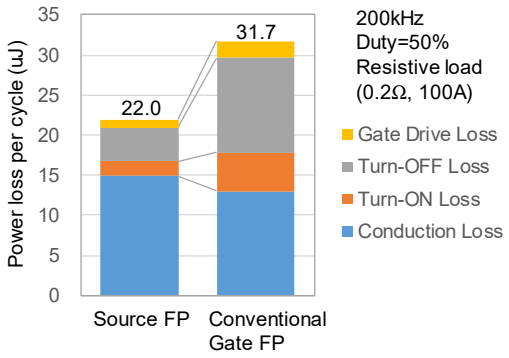

Fig. 4. A loss comparison between the Source FP and the conventional Gate FP connection.

II. Proposed Gate Driving Technique

The proposed drive circuit configurations are illustrated in Fig. 5. Here, we introduced an original circuit symbol of the FPMOS cell as shown in Fig. 5(b) in order to illustrate proposed connections simply. We propose two types of connections. In these connections, additional components of a P-channel MOSFET (Pch MOS), a diode (D_{FP}) and an inductor (L_{FP}: connection 1) or an external series resistor ($R_{FP(ext)}$: connection 2) are introduced. Internal Gate resistance (R_G) and FP resistance (R_{FP}) originated from the Gate and the FP poly silicon resistance and metal resistance on a chip. Although the circuits contain such additional components, overall these connections behave like a three terminals conventional power MOSFET. We found that the appropriate inductance of the L_{FP} in connection 1 is about 50nH or appropriate resistance of the $R_{FP(ext)}$ is about 10Ω for input capacitance C_{iss} of 8600pF of the FPMOS. We use C_{iss} of 860pF and several amperes current rating of Pch MOS for simulation. The inductor or the external resistor can be implemented on the silicon. For example, expected size of the inductor on the silicon is calculated as 200um square, 18 turns by using line/space = 2/2um Cu metal. The diode and the Pch MOS also could be integrated into a single package. By introducing these proposed connections, independent timing driving of the Gate and the Gate FP is realized easily. In the next paragraph, we described the Turn-ON and OFF operation mode of these specifically.

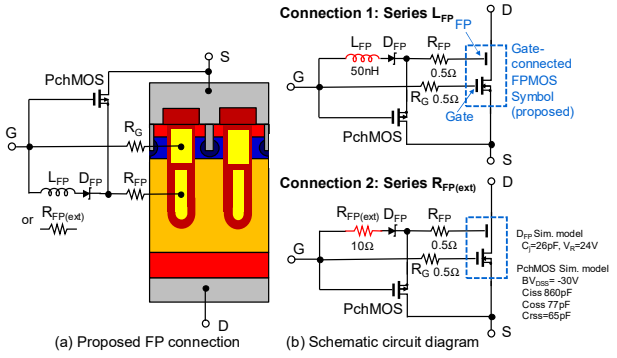

Fig. 5. Proposed gate drive techniques and schematic circuit diagrams. Additional components of a Pch MOS, a diode (D_{FP}) and an inductor (L_{FP}) or an external series resistor ($R_{FP(ext)}$) are connected to the Gate and the FP. These circuits behave like a 3-terminal Power MOSFET.

A. Turn-ON operation

Turn-ON operation mode of the proposed connections are illustrated in Fig. 6. On the Turn-ON phase, charging of the Gate FP is delayed in both connection 1 and 2. In the case of connection 1, the inductor L_{FP} and the FP capacitance works like a LC low pass filter. In the same manner, the external resister $R_{FP(ext)}$ and the FP capacitance behaves as a RC low pass filter. In both cases, the FP voltage (V_{FP}) lamp up occur after channel open. This delay decouples the Gate FP from the Gate terminal transiently, therefore, Turn-ON period reduction is expected.

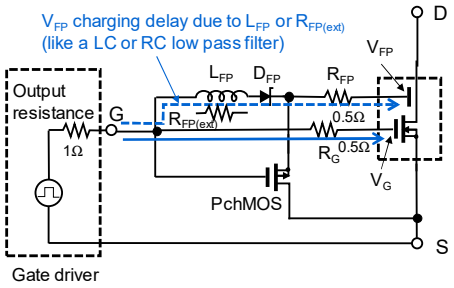

Fig. 6. A schematic of Turn-ON operation mode. The inductor L_{FP} or external resistor $R_{FP(ext)}$ decouple the field plate electrode from gate transiently and increase Turn-ON speed.

B. Turn-OFF operation

On the Turn-OFF phase, the Gate FP discharge current toward the Gate is blocked by the diode D_{FP}. In the same time, the Pch MOS turns-on because voltage of the FP is higher than the gate terminal. The ON-state Pch MOS extract discharge current rapidly as indicated in Fig. 7. This current bypass action shortens Turn-OFF time and suppress the shoot-through. In addition, this operation is able to suppress driving loss because large FP charge current do not flow into the gate driver.

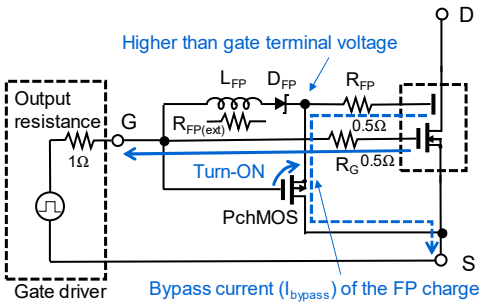

Fig. 7. A schematic of Turn-OFF operation mode. The bypass circuit of D_{FP} and Pch MOS increase Turn-OFF speed and suppress shoot-through.

III. Simulation Results

A. Turn-ON/OFF analysis in resistive load switching

Simulated Turn-ON Gate and FP voltage waveforms of the propose connection are shown in Fig. 8 and 9. As we expected, the L_{FP} or the $R_{FP(ext)}$ delayed the V_{FP} rise then Gate voltage (V_G) rise time became firster than the conventional Gate FP connection. The V_{FP} rise time of connection 1 was bit faster than that of connection 2 under the same V_G rise time condition (L_{FP}=50nH vs. $R_{FP(ext)}$=10Ω) as shown in Fig. 9. Although these waveforms are seemed slight different

behavior due to the different nature of inductance and resistance, both connections worked well as we intended.

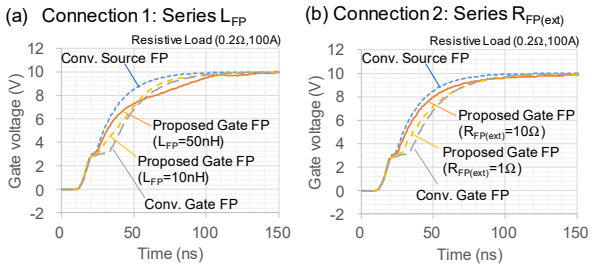

Fig.8. Simulated Turn-ON Gate voltage (V_G) waveforms of the proposed two Gate FP connections, series L_{FP} (connection 1) and series $R_{FP(ext)}$ (connection 2). Both connection reduced Turn-ON period compared to conventional Gate FP.

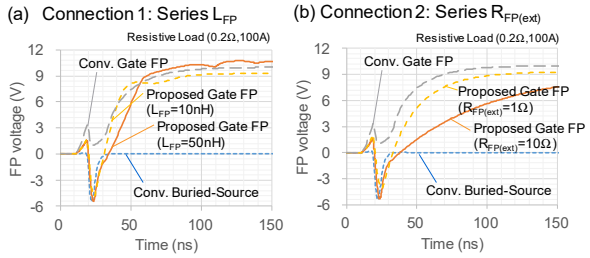

Fig.9. Simulated Turn-ON FP voltage (V_{FP}) waveforms of the proposed two Gate FP connections, series L_{FP} (connection 1) and series $R_{FP(ext)}$ (connection 2). Compare with conventional Gate FP, the V_{FP} rise of proposed Gate FPs are delayed by the L_{FP} or the $R_{FP(ext)}$.

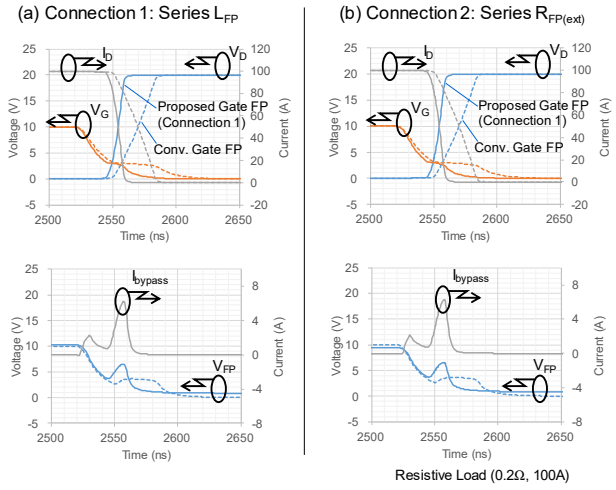

Fig.10. Simulated Turn-OFF waveforms of two proposed Gate FPs and conventional Gate FP. The bypass current I_{bypass} which extract buried FP charges is confirmed in the simulation.

In addition, Turn-OFF period was also reduced successfully as demonstrated in Fig. 10. Charges in the buried FP – drain capacitor were extracted quickly by contribution of the bypass action of the Pch MOS and D_{FP} as described in section II. Almost the same waveforms were observed in both the proposed Gate FP connection 1 and 2 because Turn-OFF action is determined by the D_{FP} and the Pch MOS.

By these Turn-ON and Turn-OFF speed-up techniques, the proposed Gate FP connections showed almost as the same resistive load switching performance as the Source FP as shown in Fig. 11. Loss comparison of the Source FP and the proposed two Gate FP connections are demonstrated in Fig. 12. Compared with the Source FP, these two types of Gate FP connections achieved lower total losses even in high speed switching (200kHz). This is due to the low conduction loss feature of the Gate FPs. Switching losses and Gate drive loss of the two Gate FPs were slightly larger than the Source FP but they were suppressed enough to reduce total losses.

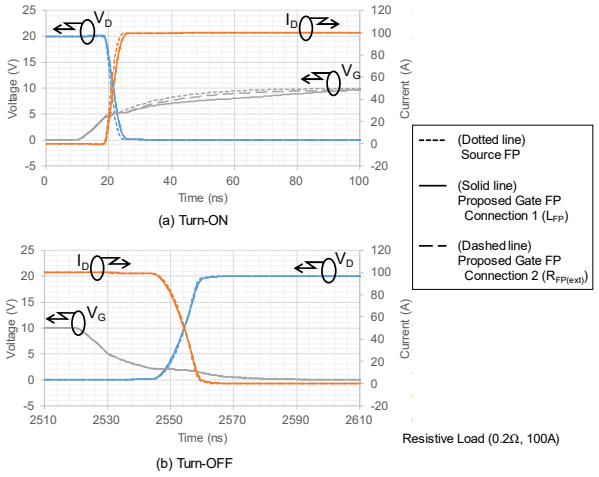

Fig. 11. Simulated waveforms comparison of the proposed Gate FP connection 1 (solid line), connection 2 (dashed line) and the Source FP (dotted line). The switching speed of both proposed connections improved nearly the same as the Source FP.

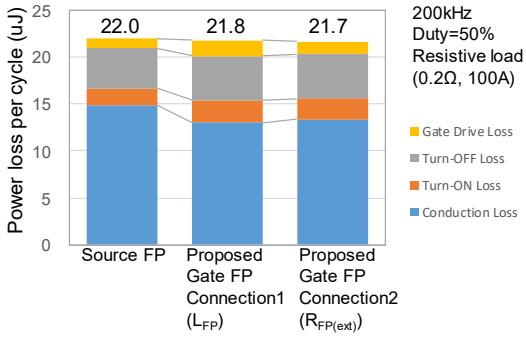

Fig.12. Loss comparison of the Source FP and the proposed Gate FPs of connection 1 and connection 2 in resistive load switching.

B. Loss analysis in high speed buck converter topology

Next, we evaluated low-side MOSFET power loss in typical buck converter topology by TCAD mixed-mode simulation. A schematic circuit of a simulated buck converter is illustrated in Fig. 13. We compared the proposed Gate FP (connection 1, using L_{FP} case), the conventional Gate FP and the Source FP of 40V class device into low-side MOSFET. On the other hand, we utilized the conventional Source FP model for high-side MOSFET in all cases. Gate driving voltage was set to +10V/0V and 2.0mΩ output resistance of gate driver was assumed. The switching frequency of this circuit was set to 250kHz.

In this topology, we concern shoot-through phenomena in the low-side device when high-side device turns-on. Figure 14 demonstrated simulated low-side waveform of the conventional Gate FP and the proposed Gate FP (connection 1 case). Large shoot-through current was observed in the case of the conventional Gate FP whereas the proposed Gate FP suppressed the shoot-through successfully. As shown in Fig.

15, the proposed Gate FP reduced low-side MOS conduction loss and realized lower total loss than the Source FP.

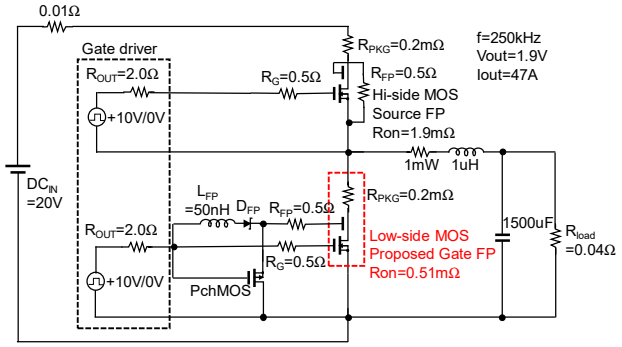

Fig.13. A schematic simulated circuit of buck converter.

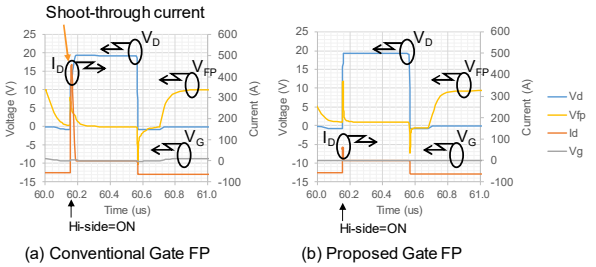

Fig.14. Simulated low-side waveforms of the conventional Gate FP and the proposed Gate FP (connection 1, L_{FP} case) in a buck converter. The proposed connection suppressed shoot-through I_D current.

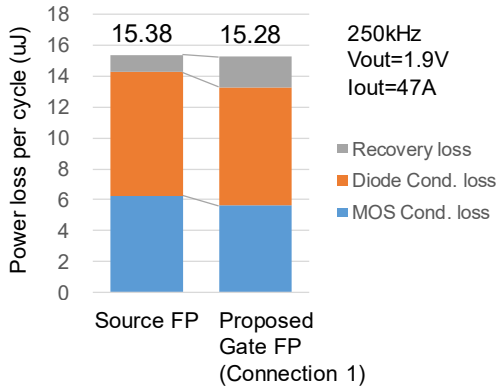

Fig.15. Simulation analysis of low-side MOS loss comparison between the Source FP and the proposed Gate FP in the buck converter.

C. *Application fields of the prposed driving technique*

So far, we estimated typical driving condition (operating frequency 200-250kHz and gate drive voltage 10V) for 40V voltage class device, however, if we operate lower switching frequency than this condition, power loss difference between the Source FP and the proposed Gate FP is expanded as shown in Fig. 16(a). This is because the conduction loss become more dominant in lower switching frequency. Therefore, the proposed Gate FP might become more advantageous. In addition, if we drive higher gate drive voltage than 10V, the conduction loss of the Gate FPs further decrease due to accumulation effect increase of the buried FP as also shown in Fig. 16(b). The drawback of this is gate drive loss increase, therefore, there is some limitations of switching frequency. However, the proposed approach expands operating frequency range of Gate FPs to over 100kHz. This must expand application field of the Gate FPs.

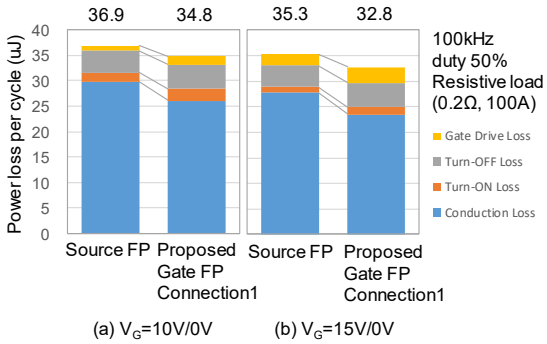

Fig.16. Influence estimation of operating frequency and gate drive voltage. The frequency was reduced to 100kHz from 200kHz.

IV. Conclusions

We proposed novel gate drive technique for Gate-connected FP MOSFET. The proposed connections consist of a diode, a Pch MOS and an inductor or an external gate resistor. This connections realize pseudo independent Gate and FP driving by using a conventional gate driver. TCAD simulation results demonstrated that the proposed Gate FP connection operated almost as the same switching performance as the Source FP and less conduction loss than that in resistive switching. In addition, this connection suppressed shoot-thorough and achieved lower power loss at low-side device in buck converter topology. These results suggested that this driving technique expands operation frequency range of the Gate-connected FP and reduces power conversion loss.

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