Stacked chip of Si power device with double side Cu plating for low on-resistance

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***Abstract*—Stacked chip is the one of the candidate structure to realize low on-resistance, small package. In order to minimize the chip size, it is required to overlap two gate and two source electrodes between two stacked chips, respectively. However, it is impossible to overlap them when wire bonding are used. We completely overlapped these electrodes between two chips by Cu clips. Additionally, double side 20μm Cu plating was applied to the device in order to obtain higher avalanche capable current density of the stacked chip. In this paper, the demonstration results of the chip by using new process are described.**

Keywords—Si power MOSFET, Stacked chip, Cu plating

I. INTRODUCTION

The application of vertical Si power MOSFETs has been spread in some power electrical systems such as electric vehicle and household electric appliance, which require both lower on-resistance (R_{on}) and small packaged size (S) for reduction of system size and high power efficiency. We have made the cell pitch narrower and the Si substrate thinner to reduce the on-resistance of the Si power MOSFET with keeping the breakdown voltage [1-4]. However, recently it has not been easy to achieve the purpose by the same ways. As other way, the stacked chip structure is attractive for lower R_{on} and small package size. The various technology to realize the stacked chip of power semiconductors are proposed for these requirements [5,6]. However, it is impossible to overlap two gate and two source electrodes between two chips when wire bonding is used. For the first time, we stacked two chips with same size by Cu clip in order to minimize the stacked chip size and applied double side 20μm Cu plating to each chip to obtain higher avalanche capable current density. Actually, we demonstrated the fabrication of the stacked chip and measured R_{on} and the current density.

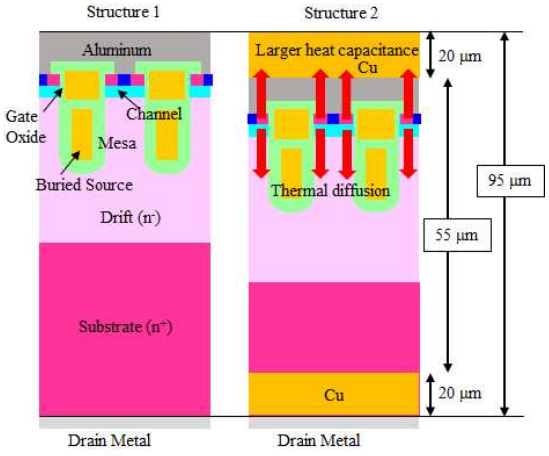


Fig.1 Two kinds of Si power MOSFET which are used for stacked chip. The thickness of each device is 95μm. No Cu is applied to structure 1 and double side 20μm Cu plating is applied to structure 2.

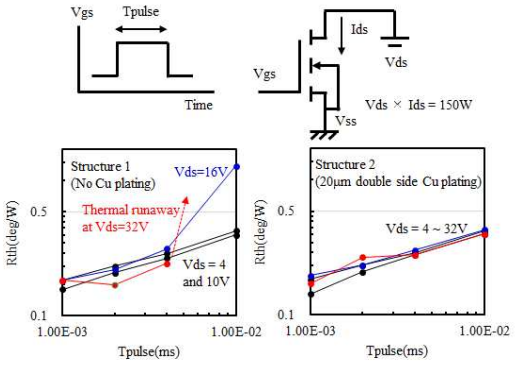


Fig.2 Time of pulse (T_{pulse}) dependence of thermal resistance for 40V Si power device with structure 1 and 2 when $V_{ds} \times I_{ds}$ is fixed at 150 W.

II. ELECTRICAL CHARACTERITICS OF CHIPS

In this experience we have two kinds of 40V Si power MOSFET used as the stacked chip (The chip size is 5mm × 5mm). One has Si substrate of 95μm and no Cu plating (structure 1). Another has thinner Si substrate of 55μm and double side 20μm Cu plating (structure 2) as shown in fig.1 [7-9]. Fig.2 shows time of pulse (T_{pulse}) dependence of thermal resistance for the device with and without Cu plating. The resistance monotonically increases with T_{pulse} in Cu plating case. On the other hand, the abrupt increase of the resistance at V_{ds} = 16V is observed and the thermal runaway occurs at V_{ds} = 32V when the T_{pulse} is 0.1ms in no Cu plating sample. These results show the thicker Cu can suppress to increase the local temperature and thermal runaway during the device operation due to larger heat capacitance. Fig.3 shows comparison of R_{on} between structure 1 and 2. That of structure 2 is 27% and 30% lower at V_{gs} = 6V and 10V than structure 1, respectively, because thinner Si substrate realize lower R_{on} due to reduce the substrate resistance. Fig.4 shows the configuration of the stacked chip. Two chips are set in parallel to reduce R_{on} and are overlapped to realize the small area of stacked chips.

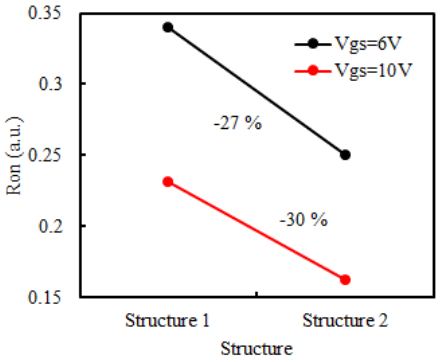


Fig.3 Comparison of R_{on} between structure 1 and 2. That of structure 2 is 27% lower at V_{gs} = 6V and 30% lower at V_{gs} = 10V than structure 1 due to thinner Si substrate.

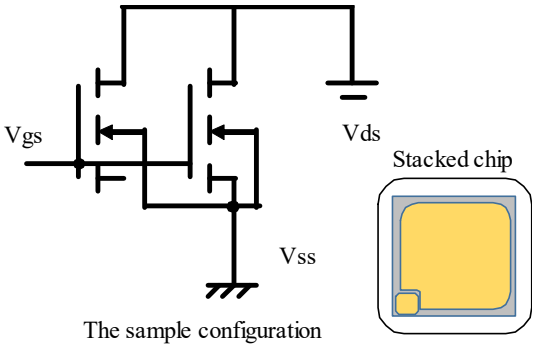


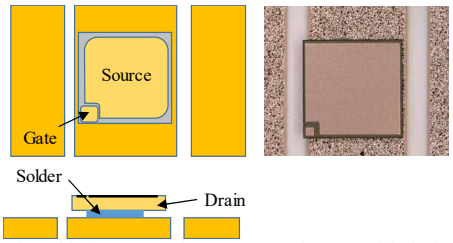
Fig.4 The sample configuration for setting two chips in parallel to reduce R_{on}. These chips are overlapped to realize the small area of stacked chips.

III. SAMPLE FABRICATION FOR THE STACKING

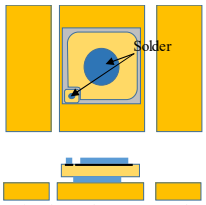
Fig.5 shows the process flow of the stacked chip structure by using Cu clips and DBC substrate.

After solder is deposited on a DBC substrate, first device chip is mounted on DBC substrate with the drain down (fig.5-a). After solder is deposited on gate and source electrode of first device chip (fig.5-b), two Cu clips are set on the gate and source electrode, respectively (fig.5-c). After solder is deposited on these Cu clips which connect to the gate and source (fig.5-d), second device chip with the same structure as the first device chip is stacked on a bottom chip with the drain on top. At this stage, each gate and source electrode of two device chips are connected by solder and Cu clip (fig.5-e). After solder is deposited on the drain electrode of the second device chip, a Cu clip is set on the electrode in order to connect drain of the first device chip. This Cu clip is connected to DBC substrate which connects to the drain of first device chip (fig.5-f). After that melting process is carried out to melt the solder and to strengthen adhesion force between each electrode and Cu clips.

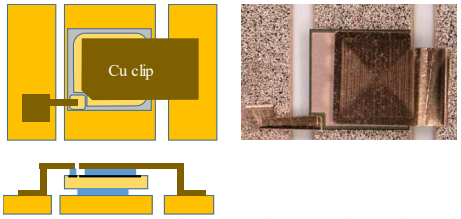
In this process, it is possible to overlap two gate and two source electrodes between two chips completely because not wire bonding but Cu clips are used. As a result, the minimum size of the stacked chip can be realized.



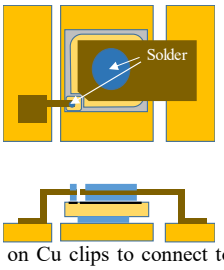
a) A device chip is mounted on a DBC substrate with drain down.



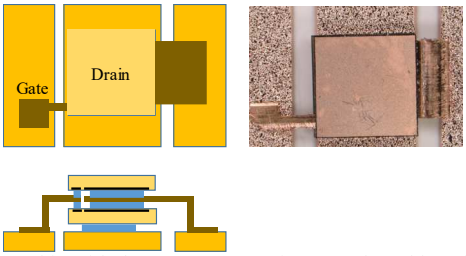
b) Solder is deposited on the gate and source electrode.



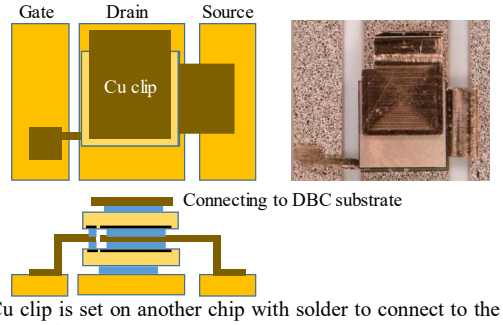
c) Two Cu clips are set on the gate and source electrode with solder.



d) Solder is deposited on Cu clips to connect to the gate and source electrode



e) Another chip with the same structure is set on the solder with drain on top. Each gate and source of two chips is connected.



f) A Cu clip is set on another chip with solder to connect to the drain of mounted device.

Fig.5 The process flow to fabricate stacked chip structure.

IV. ELECTRICAL CHARACTERITICS

A. *On resistance (R_{on})*

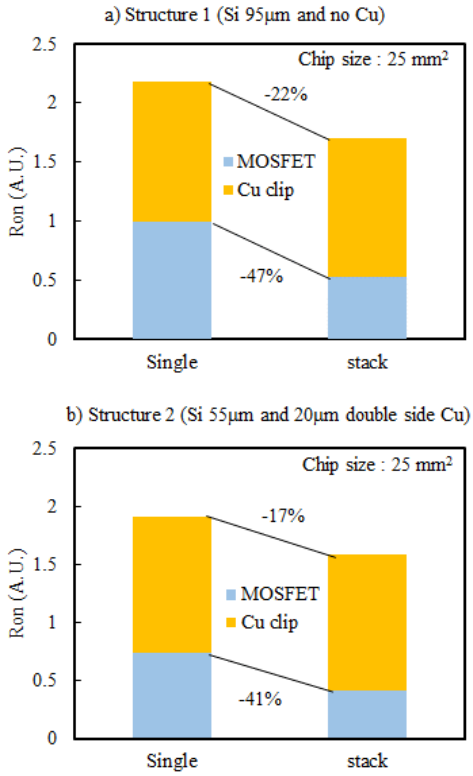


Fig.6 R_{on} measurement results of single and stacked chip for structure 1 and 2. Each value is normalized by MOSFET's R_{on} of structure 1. The calculated Cu clip resistance is used to estimate MOSFET's R_{on}

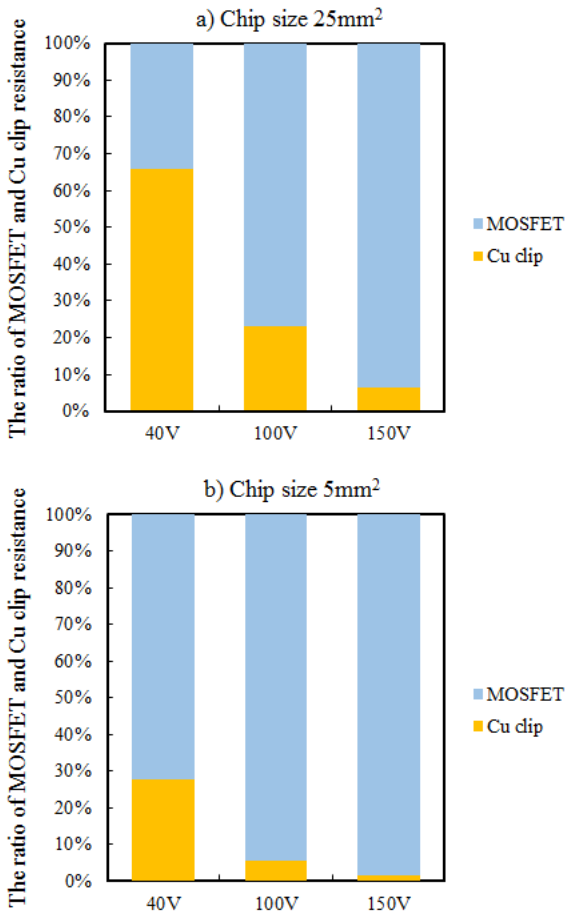


Fig.7 The ratio of MOSFET and Cu clip resistance of assembled single chip for various breakdown voltage when the Si substrate is 95μm and the chip size is 25mm² and 5mm².

Fig.6 shows R_{on} measurement results of the stacked chip fabricated by process flow as show in fig.5. We also measured R_{on} of a single chip fabricated by using the same Cu clips used in the stacked chip fabrication. Each value of R_{on} is normalized by intrinsic R_{on} of the MOSFET of structure 1 and the calculated Cu clip resistance is used to estimate the MOSFET's R_{on}. The MOSFET's R_{on} is 47% and 41% lower than that of single chip for structure 1 and 2, respectively. However, the total resistance of stacked chip is only 22% and 17% lower for structure 1 and 2 because the ratio of Cu clip resistance is larger comparing with the intrinsic R_{on} in 40V Si power MOSFET. Fig.7 shows the ratio of MOSFET and Cu clip resistance of single chip for various breakdown voltage MOSFETs when the Si substrate is 95μm, no Cu plating (Structure 1) and the chip size is 25mm² and 5mm². The resistance occupied by Cu clip is a large proportion for 40V Si power MOSFET with 25mm² chip size. However, the ratio of the Cu clip resistance decreases as breakdown voltage becomes larger or the chip size becomes smaller because the MOSFET's R_{on} increases. Fig.8 shows the ratio of decrease of total resistance in from a single chip to stacked chip. The ratio is only -22% for 40V Si power MOSFET, while that is -48% for 150V power device in 25mm² chip size. Additionally, the ratio is -33% and -49% for 40V and 150V Si power MOSFETs, respectively in 10mm² chip size. These results indicate the stacking technology is significantly useful for larger breakdown voltage device or small chip size in order to reduce R_{on}.

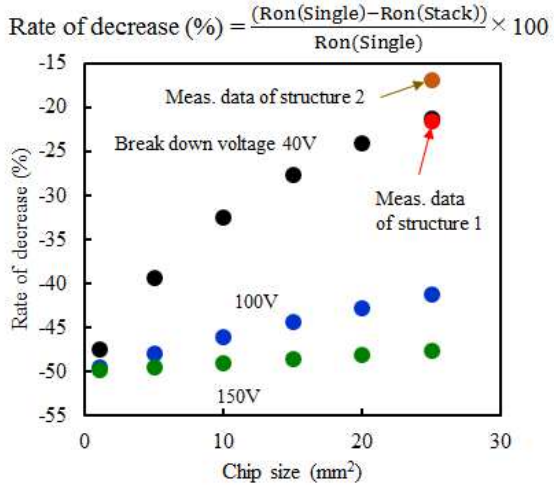


Fig.8 The ratio of decrease of total resistance in from a single chip to stacked chip. These results indicate the stacking technology is significantly useful for larger breakdown voltage device or small chip size in order to reduce R_{on}.

B. *Avalanche capable current density*

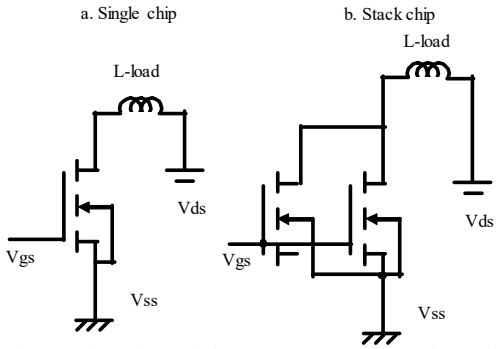


Fig.9 The configuration of the system to measure the avalanche capable current density of the single and stacked chip.

Fig.9 shows the configuration of the system to measure the avalanche capable current density of the single and stacked chip. The energy is charged into the inductance during on-state of device and the energy is discharged to the device during off-state. The maximum current before breakdown is measured as the avalanche capable current density. Fig.10 shows the current density for the single and stacked chip of structure 1 and 2. The current density of the stacked chip is 49% larger than the single chip in structure 1. Additionally, the density becomes 59% larger by stacked chip with thicker Cu plating (structure 2) comparing with the single chip without Cu plating (structure 1). The simulation was carried out to analyze the origin of the higher density of the stacked chip with double side 20µm Cu plating. Fig.11 shows the simulation results of temperature profile of stacked chip of structure 1 and 2 after the operation with V_{ds} = 16V and T_{pulse} = 0.1ms. The origin is at the junction between base (P-type) and mesa (N-type). T_{max} of stacked chip with thicker Cu plating is lower than no Cu plating due to larger heat capacitance.

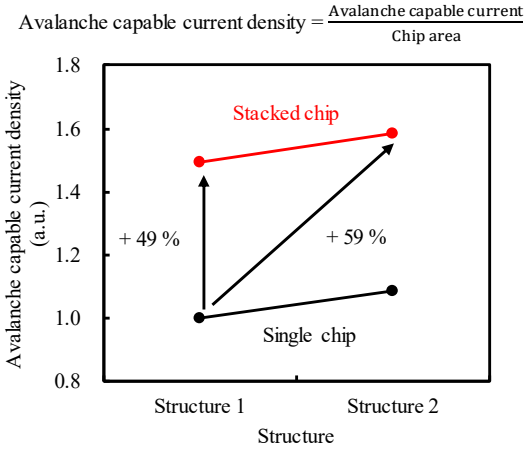


Fig.10 The avalanche capable current density for the single and stacked chip of structure 1 (no Cu plating) and structure 2 (20µm double side Cu plating). This results indicate the density of stacked chip with thicker Cu plating is 58.7% larger comparing with single chip without Cu plating.

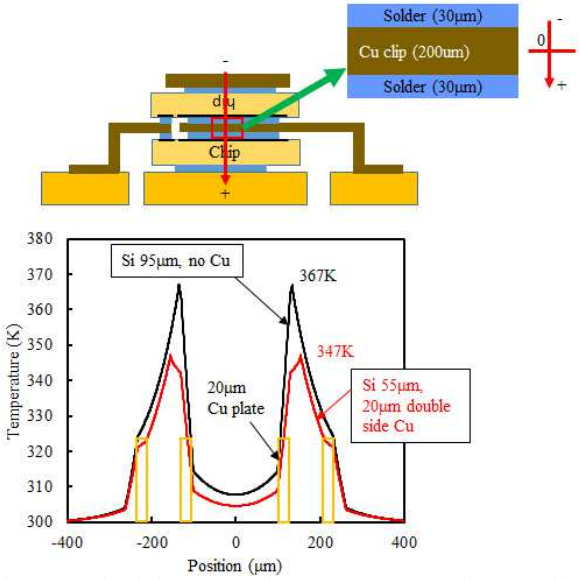


Fig.11 The simulation results of temperature profile of stacked chip of structure 1 (no Cu plating) and structure 2 (20µm double side Cu plating) after the operation with V_{ds} = 16V and T_{pulse} = 0.1ms. The origin is at the junction between base (P-type) and mesa (N-type). T_{max} of stacked chip with thicker Cu plating is lower than no Cu case due to larger heat capacitance.

V. Conclusion

We fabricated the stacked device chip with double side thicker Cu plating by using Cu clips, and obtained 41% lower the MOSFET's R_{on} and 59% larger the avalanche capable current density. According to our estimation, this stacking technology is significantly useful for larger breakdown voltage device or small chip size in order to reduce R_{on}.

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