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Drift Layer Design utilizing Intermediate Boron Ion-implantation for 100-V-class Two-step-oxide Field-Plate Trench MOSFET to Improve Switching Loss

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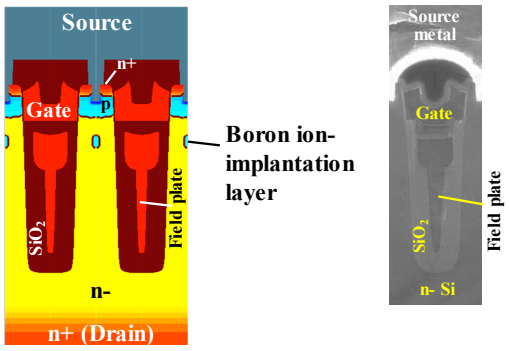
***Abstract*—We studied an advanced drift layer design which has an intermediate layer in mesa region for two-step-oxide field-plate MOSFET. The intermediate layer is formed by a high energy ion-implantation via source contact window. By TCAD simulation, it was confirmed the intermediate layer can decrease depletion layer capacitance in lower drain voltage. There was no change of breakdown voltage, and on-resistance ($R_{ON}A$) increased slightly with increasing the implantation energy. An attractive effectiveness was obtained as gate-drain charge (Q_{GD}) decrease, and output charge and reverse recovery charge were slightly decreased. Evaluated performances showed that the Q_{GD} and $R_{ON}Q_{GD}$ were reduced by 14.1% and 10%, respectively. In power loss estimation of an assumed circuit, it was observed the newly designed FP-MOSFET can improve total power loss, especially in high-speed switching.**

Keywords—field plate, RESURF, shielded gate, gate-drain charge, output charge, power loss.

I. Introduction

Field-plate trench MOSFETs (FP-MOSFETs) have been continuously developed for high efficiency electronics [1]–[7], in particular, 100-V-class devices are applied to 48-V input power converters and 48-V battery automobile systems. Commercially, conventional FP-MOSFETs having a straight poly-silicon field-plate inside trench have been constructed by a fairly uniform thick oxide in a view point of the fabrication process. In contrast, a gradient field-plate oxide structure has been proposed to improve an electric field distribution in a drift layer [8]. We have demonstrated a multiple-stepped-oxide FP-MOSFET to improve a tradeoff between breakdown voltage (V_B) and specific on-resistance ($R_{ON}A$) [9]. Subsequently, we have developed a two-step-oxide (2-step) FP-MOSFET which can enhance RESURF (Reduced Surface Field) effect as simplified structure and process [10].

However, in order to realize a better system efficiency, we have to continuously explore room to be able to improve the device performance. Therefore, we study an advanced drift layer design which has a boron ion-implantation layer in an intermediate mesa region in the 2-step FP-MOSFET. A similar structure in the conventional FP-MOSFET has shown previously and a behavior of the V_B was analyzed [11]. In this paper, as a detail study, we validate the device characteristics which influence to circuit power losses by both TCAD simulations and experiments.



(a) (b)

Fig. 1. Cross-sectional views of newly designed 2-step FP-MOSFET having intermediate boron ion-implantation layer in center of mesa region. (a) TCAD simulated image and (b) SEM photograph of fabricated device.

II. Device Structure and Applicable Process

The device structure of newly designed 2-step FP-MOSFET and a fabricated device are shown in Figs. 1(a) and 1(b). The 2-step FP-MOSFET is formed by two steps of thick-oxide and two steps of poly-silicon field plate. This field-plate structure contributes to form an inflection of the electric field distribution in the mesa region and can obtain the high V_B even in the high doping concentration [10]. The intermediate layer in the center of mesa region is formed by a high energy boron ion ($^{11}B^+$) implantation via source contact window. The additional process is only one step. A depth of the intermediate layer can be varied by the implantation energy, e.g., 400–2000 keV. Simulated doping profiles by different implantation doses are illustrated in Fig. 2.

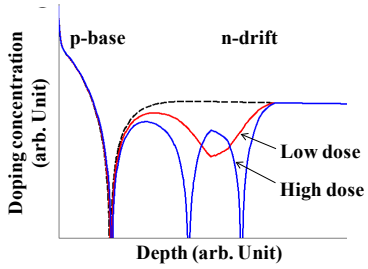


Fig. 2. Simulated doping profiles of center of mesa region in vertical direction, for 2-step FP-MOSFETs. Withiout boron ion-implantation layer (black dashed line) and intermediate boron ion-implantation layer: low dose (red solid line) and high dose (blue solid line) conditions.

III. Device Simulation

Firstly, by using the TCAD simulation, a behavior of the intermediate layer in the 2-step FP-MOSFET was investigated. It was thought that the boron ion-implantation layer gives an influence to parasitic capacitances: reverse transfer capacitance (C_{rss}) and output capacitance (C_{oss}). Therefore, drain-source voltage (V_{DS}) dependences of depletion layer expansion were simulated (Fig. 3). Actually, a difference between two structures (with/without the intermediate boron ion-implantation layer) were recognized and it was confirmed the intermediate layer can decrease depletion layer capacitances (C_{GD2} and C_{DS1}) in the region less than V_{DS} = 30 V (Fig. 4). In addition, the energy and the dose dependences were also observed. This behavior is expected to decrease gate-drain charge (Q_{GD}) and output charge (Q_{oss}).

Figs. 5(a) and 5(b) show simulated implantation energy dependences of the V_B and the $R_{ON}A$. There was no change of the V_B until 1200 keV, and the $R_{ON}A$ increased slightly with increasing the energy or the implantation dose.

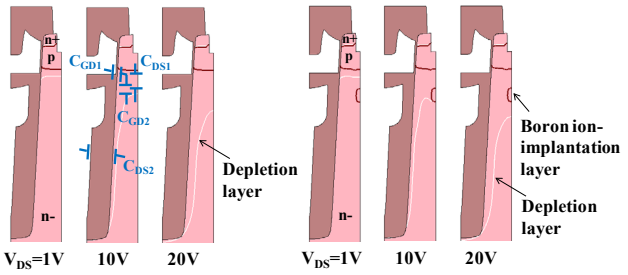


Fig. 3. Simulated (a) 2-step FP-MOSFET, and (b) 2-step FP-MOSFET with intermediate boron ion-implantation layer, which represent V_{DS} dependences of depletion layer expansion: V_{DS} = 1 V, 10 V, and 20 V. Parasitic capacitances are shown in the left-middle figure and they can be expressed as: $C_{rss} = C_{GD1}C_{GD2}/(C_{GD1}+C_{GD2})$, $C_{oss} = C_{rss}+C_{DS1}+C_{DS2}$.

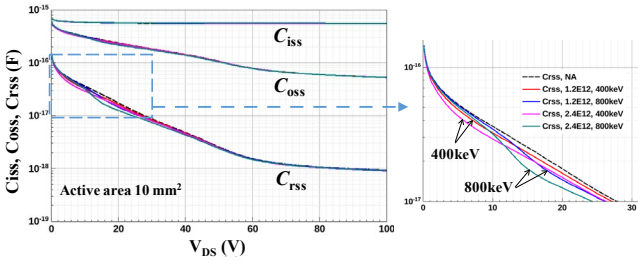


Fig. 4. (a) Simulated V_{DS} dependences of C_{iss}, C_{oss}, and C_{rss}, for 2-step FP-MOSFETs with/without intermediate boron ion-implantation layer. (b) Enlarged view of low V_{DS} region (0–30 V). Implantation dose: 1.2E12 and 2.4E12 /cm^2. Implantation energy: 400 and 800 keV.

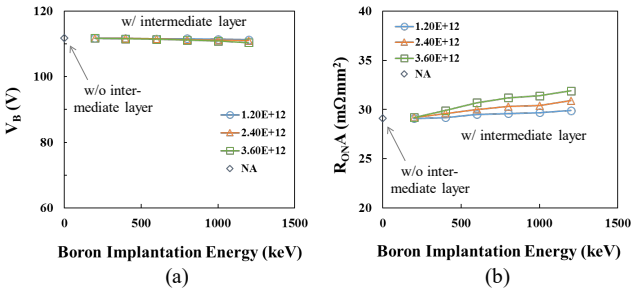


Fig. 5. Simulated implantation energy dependences of (a) V_B and (b) $R_{ON}A$, for 2-step FP-MOSFETs with/without intermediate boron ion-implantation layer. Implantation dose: 1.2E12–3.6E12 /cm^2.

IV. Experimental Results

A. Breakdown Voltage and On-resistance

Subsequently, the newly designed 2-step FP-MOSFETs were actually manufactured applying a relatively low implantation dose condition. The V_B was maintained until the implantation energy of 800 keV as sufficient values of 105–107 V, as shown in Fig. 6(a). The $R_{ON}A$ was measured under the condition of gate voltage V_{GS} = 10 V and drain current I_D = 30 A, and obtained 26.5–27.9 mΩmm^2, as shown in Fig. 6(b). The implantation energy dependence of the $R_{ON}A$ was as same as the simulation results, however, a significant increase was not found by adding the intermediate layer. The measured $R_{ON}A$ was 9–6% smaller than simulated results. This is because a strain effect caused by the thick oxide inside trench was added [12], thus it is considered both channel and drift resistances decreased by the effect.

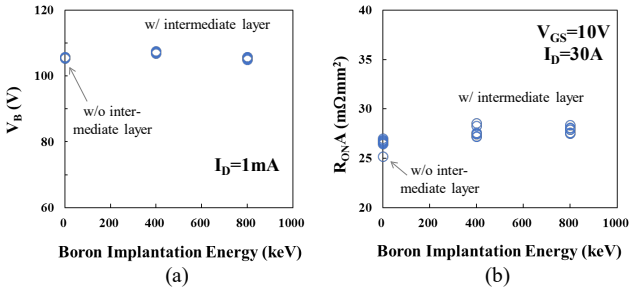


Fig. 6. Measured implantation energy dependences of (a) V_B and (b) $R_{ON}A$, for 2-step FP-MOSFETs with/without intermediate boron ion-implantation layer. Measurement conditions: I_D = 1mA for V_B; and V_{GS} = 10 V and I_D = 30 A for $R_{ON}A$.

B. Gate Charge and Output Charge

An attractive effectiveness of the intermediate layer was found in measured Q_{GD}/A (A means unit area). Those were 1.29 nC/mm^2 and 1.18 nC/mm^2 as average, for the energy of 400 keV and 800 keV, respectively, as shown in Figs. 7(a) and 7(b). The reduction rates by adding the intermediate layer were 7.1–14.4%.

Moreover, it was also confirmed measured Q_{oss}/A was slightly decreased (3.3%), as shown in Fig. 8. The Q_{oss} was calculated by the V_{DS} integral of the C_{oss}. The Q_{oss}/A reduction includes the effect of the Q_{GD}/A reduction.

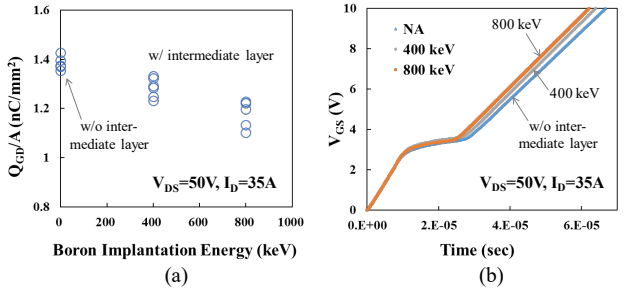


Fig. 7. (a) Measured implantation energy dependences of Q_{GD}/A for 2-step FP-MOSFETs with/without intermediate boron ion-implantation layer. (b) Measured total gate charge waveforms. Measurement conditions: V_{DS} = 50 V and I_D = 35 A.

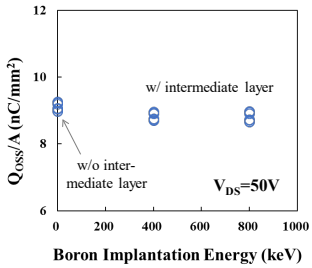
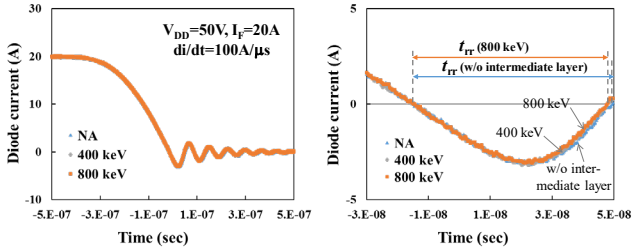


Fig. 8. Measured implantation energy dependences of Q_{oss}/A for 2-step FP-MOSFETs with/without intermediate boron ion-implantation layer. Measurement condition: V_{DS} = 50 V.

C. Body Diode Reverse Recovery

Body diode reverse-recovery waveforms were measured under the condition of forward current I_F = 20 A, supply voltage V_{DD} = 50 V, and di/dt = 100 A/μs. As shown in Fig. 9(a), a significant difference was not observed in between two structures (with/without the intermediate layer) until 800 keV. However, it was also confirmed reverse recovery charge Q_{rr}/A was slightly decreased (4.2%), due to a small reduction of reverse recovery time (t_{rr}), as shown in Fig. 9(b).



(a) (b)

Fig. 9. (a) Measured body diode reverse recovery waveforms for 2-step FP-MOSFETs with/without intermediate boron ion-implantation layer. (b) Enlarged view of reverse current region. Measurement conditions: V_{DD} = 50 V, I_F = 20 A, and di/dt = 100 A/μs.

D. Avalanche Capability

Fig. 10 shows an inductive load switching waveforms before destruction under the condition of V_{DD} = 60 V, V_{GS} = 0–15 V, and inductance L = 100 μH. It was confirmed the intermediate layer did not affect to the avalanche capability.

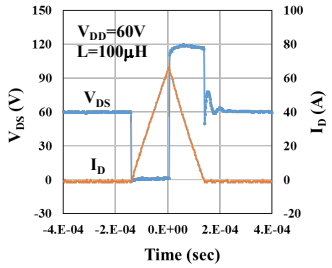


Fig. 10. Measured inductive load switching waveforms before destruction, for 2-step FP-MOSFETs with intermediate boron ion-implantation layer. Measurement conditions: V_{DD} = 60 V, V_{GD} = 0–15 V, and L = 100 μH.

E. Figure-of-Merit

As the device performance comparison, figures-of-merit (FOMs) calculated by the measurement results were shown in Fig. 11. Here, the conventional straight FP-MOSFET which has been described in [10], the 2-step FP-MOSFET without the intermediate layer, and the 2-step FP-MOSFET with the intermediate layer (800 keV condition) are compared.

The $R_{ON}A$ of the 2-step FP-MOSFET with the intermediate layer kept 16% reduction compared with that of the conventional FP-MOSFET, in spite of 5.3% increase compared with the 2-step FP-MOSFET without the intermediate layer.

When the FP-MOSFETs are applied in a high efficiency switching circuit, charge properties, i.e., total gate charge (Q_G), gate-drain charge (Q_{GD}), and output charge (Q_{oss}), are very important. Moreover, as an indicator of the switching property, Q_{SW} is defined by sum of gate-source charge (Q_{GS}) after threshold voltage and the Q_{GD}. As a remarkable result of this study, $R_{ON}Q_{GD}$ was reduced by 10% by only adding the intermediate layer in the 2-step FP-MOSFET.

Moreover, it was confirmed that $R_{ON}Q_G$ was reduced by 27.6% compared with that of the conventional FP-MOSFET (having the straight field plate). However, it includes not only the Q_{GD} reduction but also the effect of a modification of the gate-source insulating film structure, as described in [10].

$R_{ON}Q_{oss}$ of the 2-step FP-MOSFET has become greater than that of the conventional FP-MOSFET because of applying the higher doping concentration in the drift layer [10]. On the other hand, the $R_{ON}Q_{oss}$ increase by adding the intermediate layer was small enough (1.8%), that was contribution of the Q_{oss}/A reduction shown in Fig. 8.

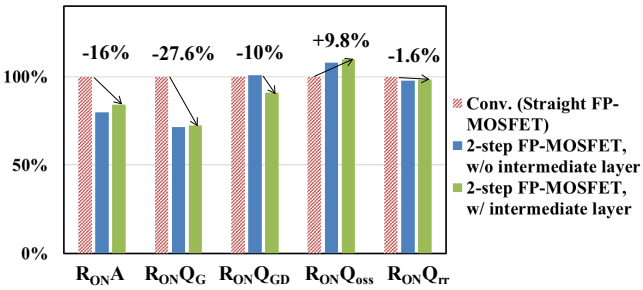


Fig. 11. Comparison of figures-of-merit (FOMs) for conventional FP-MOSFET and 2-step FP-MOSFETs with/without intermediate boron ion-implantation layer (800 keV). Measurement conditions: V_{GS} = 10 V and I_D = 30 A for R_{ON}; V_{DS} = 50 V and I_D = 35 A for Q_G and Q_{GD}; V_{DS} = 50 V for Q_{oss};.and V_{DD} = 50 V and I_F = 20 A for Q_{rr}.

Similarly, in $R_{ON}Q_{rr}$, the decreasing rate of the R_{ON} and the increasing rate of the Q_{rr}, which were confirmed by the intermediate layer, were almost cancelled each other.

V. Power Loss Estimation

In order to evaluate the device performance improvement shown in Fig. 11, we took account of a synchronous buck converter circuit and calculated each component of the power loss: conduction loss (P_{CON}), gate drive loss (P_{GD}), switching loss (P_{SW}), output charge loss (P_{Qoss}) and reverse recovery loss (P_{Qrr}) by general formulas [13].

Generally, the lower R_{ON} is appropriate to the low-side (LS) device, and the lower charge properties are required as the high-side (HS) device. Therefore, in comparison of the two kinds of the MOSFETs, as the low-side, same die size was assumed to achieve the lowest R_{ON} in a same package, e.g., SOP-8. As the high-side, same R_{ON} MOSFETs were assumed with considering a necessary current rating. In addition, we

assumed input voltage V_{IN} = 48 V, output current I_O = 35 A, drive voltage V_{GS} = 10 V, gate current I_G = 1 mA, and duty ratio D of 75%/25% for the low-side/high-side. The switching frequency (f_{SW}) was varied from 100 kHz to 1 MHz.

Fig. 12 shows the power loss estimation for the 2-step FP-MOSFETs with/without the intermediate layer. The small difference of the $R_{ON}A$ shown in Fig. 11 did not influence very much to the P_{CON} even in the low-side use. In addition, the P_{CON} also did not depend on the switching frequency.

On the other hand, the other power loss components increased depending on the switching frequency. Among those losses, the P_{SW} occupies a large part of the total loss in each side, especially in a hard switching circuit. Therefore, in the 1 MHz switching condition, 5.8% improvement of the total power loss was clearly observed in the 2-step FP-MOSFET with the intermediate layer, which effectiveness was corresponding to the lower Q_{GD}.

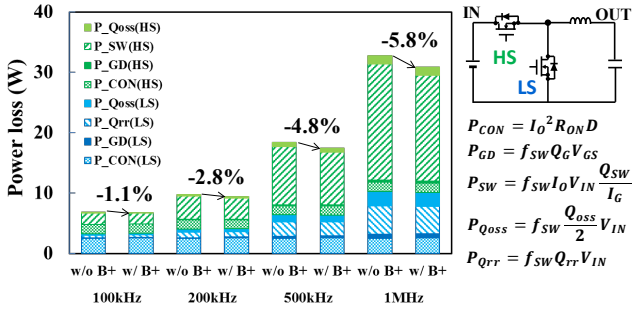


Fig. 12. Comparison of estimated switching frequency dependences of power losses for 2-step FP-MOSFETs with/without intermediate boron (B^+) ion-implantation layer. A synchronous buck converter circuit is assumed under the condition of V_{IN} = 48 V, I_O = 35 A, V_{GS} = 10 V, I_G = 1 mA, f_{SW} = 100 kHz–1 MHz, and 75%/25% duty ratio for low-side (LS)/high-side (HS).

VI. Conclusions

We studied the 2-step FP-MOSFET having the intermediate boron ion-implantation layer in the mesa region, as the advanced drift layer design. This structure can decrease the depletion layer capacitance in lower drain voltage. The V_B was not affected and $R_{ON}A$ increased slightly with increasing the implantation energy. By the real device evaluation, the advantage was confirmed as the 14.1% decrease of the Q_{GD} and 10% decrease of the $R_{ON}Q_{GD}$. In addition, both Q_{oss} and Q_{rr} were also decreased slightly. The power loss of the assumed circuit was estimated by using the FOMs and 5.8% improvement was observed for the 1 MHz switching. We demonstrated that the FP-MOSFET performance can improve sufficiently by adding only one process step.

Acknowledgment

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