T. Suwa et al., "Investigation of TCAD Calibration for Saturation and Tail Current of 6.5kV IGBTs", 2019 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), Udine, Italy, 2019, pp. 101-104. Doi: 10.1109/SISPAD.2019.8870514

Investigation of TCAD Calibration for Saturation and Tail Current of 6.5kV IGBTs

Takeshi Suwa and Shigeaki Hayase
Toshiba Electronic Devices & Storage Corporation,
Kawasaki, Japan
Email:takeshi.suwa@glb.toshiba.co.jp

Abstract—In this work we focus on two calibration methods to clarify a key point of TCAD calibration for turn-off waveforms and IV characteristics including the saturation currents of IGBTs at the same time. Simulated results with the method based on adjustments of the surface N+ and P+ depth ratio reproduce measured results of all calibration targets reasonably in terms of time and accuracy. On the other hand, simulated results by mainly calibrating parameters of the velocity saturation model for saturation currents hardly reproduce all calibration targets simultaneously. We explain the reason using the roughly approximated criteria of the dynamic punch-through oscillation and dynamic avalanche. We also analyze the temperature dependence of the tail current briefly which is one of the important design items of IGBTs.

Keywords—IGBT, tail current, saturation current, calibration

I. INTRODUCTION

When optimizing and designing IGBTs for new products, it is very useful to have well calibrated TCAD tools for that generation that cover the range needed for the design [1], [2]. Here, well calibrated tools means that the tools has good predictability and convergence and it takes only a reasonable calculation time. Good predictability is achieved by selecting suitable calibration targets for the design and calibrating the tools to reproduce the target's measurements well. It is also important that calibration can be performed in a short time and easily.

The key point of the IGBT calibration is that the electrical characteristics crucially depend on the horizontal channel layout on the silicon surface side [3]. Fig. 1 shows schematic IGBT and diode structures for device simulations. The IGBT channel length in the pitch direction of Fig. 1 is shortened to reduce the saturation current so that the IGBT does not break at the time of short circuit. Further, in order to lower the on-resistance by raising the carrier density under the trenches in conduction state, the number of channels in the lateral direction is also reduced. For these reasons, the IGBT is basically a three-dimensional (3D) device, and the number of cells in one unit structure is large unfortunately.

When simulating IGBTs using Sentaurus TCAD tools, we often use following three basic ways:(1) two-dimensional (2D) device simulations using 2D structures made from 2D process simulations, (2) 3D device simulations using 3D structures made from 2D process simulations, and (3) 3D device simulations using 3D structures made from 3D process simulations. Although the method using 2D structures has the shortest calculation time, it is necessary to reproduce the effect of the 3D channel current flow of the IGBT by contriving process and device simulations. For that purpose, a method is generally used that reproduces both the measured on-state voltage and the saturation current by adjusting the model parameters of channel mobility and velocity saturation in the drift region. Making a structure using 3D process simulations is the most correct and interesting way, however for IGBTs the computation time is relatively long and calibration is a little more difficult than the other ways. As high concentration boron and phosphorus diffuse and mix up in narrow silicon regions sandwiched by gate trenches, Secondary Ion Mass Spectrometry (SIMS) data are not effective for calibrations. Further we have to adjust the profile finely, because electrical characteristics are very sensitive to the depth ratio of the each profile. The low temperature process also makes calibration a bit more difficult. This method is often used when we do not need to create many types of structures or when we have a lot of time for calibrations. On the other hand, 3D device simulations have become relatively easy due to improvements in the software, and it is most efficient especially for large structures such as IGBTs to carry out 3D device simulations with 3D structures made by combining 2D process simulation results. When we simulate the reliability of IGBTs by increasing the number of cells, it is preferable to be able to reduce the number of meshes as much as possible [4]. In this work diodes (Free-Wheeling Diodes) are 2D structures, so device simulation carried out using the results of two-dimensional process simulation for diodes.

II. TARGETS AND SIMULATION APPROCH

Calibration targets are the IGBT turn-off waveforms and collector currents Ic as functions of collector-emitter voltage Vce and gate-emitter voltage Vge. To reproduce turn-on and short-circuit waveforms in the future, carrier lifetime dependence of IV-characteristics of diodes and saturation currents of IGBTs are also included in the calibration targets. The calibration ranges are as follows. The ambient temperature ranges from 298K to 398K, and there are three conditions for p base concentration and two N+ width ratios for IGBTs and four carrier life time conditions for diodes. In this work we adopt Shockley–Read–Hall (SRH) model as a model of carrier recombination through deep defect levels for device simulation, and carrier lifetimes of IGBTs in the drift region are obtained by extrapolating from calibrated lifetimes of diodes. We use Spreading Resistance (SR) data to make p collector and n buffer profiles on the back side, and the thickness of the trench oxide film is adjusted with reference to the cross-sectional Scanning Electron Microscope (SEM) image. The threshold voltage characteristics may be calibrated by adjusting the parameters of the segregation model or the work function difference.

In terms of cost and ease, we often adopt a method of mainly adjusting parameters of the velocity saturation model

978-1-7281-0940-4/19/$31.00 ©2019 IEEE

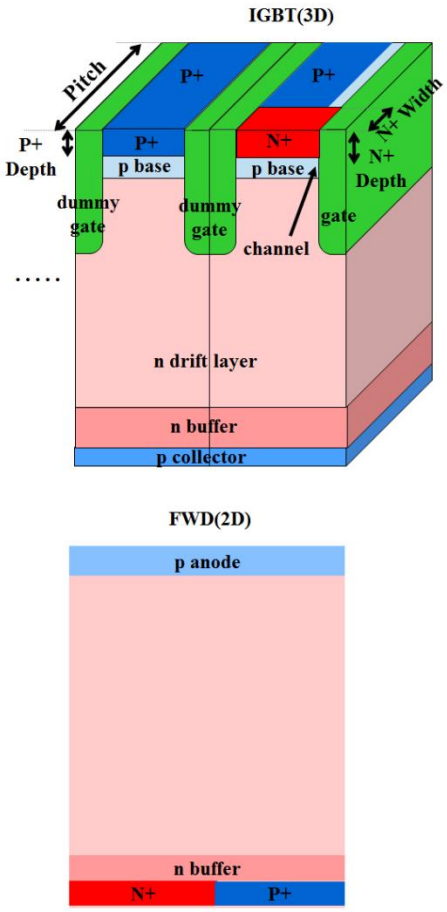

Fig. 1: Schematic view of the simulated structures (IGBT and diode).

without correcting the surface profiles to reproduce the saturation current, even if the process or physical basis are scarce (hereinafter abbreviated as Method-1). Although it is preferable to firstly calibrate the surface profile, it takes time to calibrate many type of structures in the 3D process simulation. We propose another method that we mainly adjust the surface N+ and P+ profiles to reproduce the saturation current. When we create a 3D structure by extending and bonding two 2D impurity profiles in the N+ and P+ regions, we calibrate the acceleration voltage of each surface N+ and P+ implantation of 2D structures and adjust the depth ratio of a 3D structure to reproduce the saturation currents (hereinafter abbreviated as Method-2, newly proposed method). Examples in which each current path spreading is different depending on the depth ratio are shown in Fig. 2. At this time, the on-voltages differ by about 10%, and the saturation currents differ by about three times. As is well known, in on-state calculations using the channel mobility degradation model, it is necessary to pay attention to the mesh of channel interfaces because the effect of the discretization error of the first layer mesh at the interface is large [5].

III. RESULTS AND DISCUSSION

Fig. 3 shows some examples of calibrated IV results with Method-2. These are in good agreement with the measurement results. This is because IV characteristics of IGBTs strongly depend on the 3D current path of the channel region, which is mainly determined by depth and width ratios of surface N+ and P+ profiles. If we sufficiently lower the

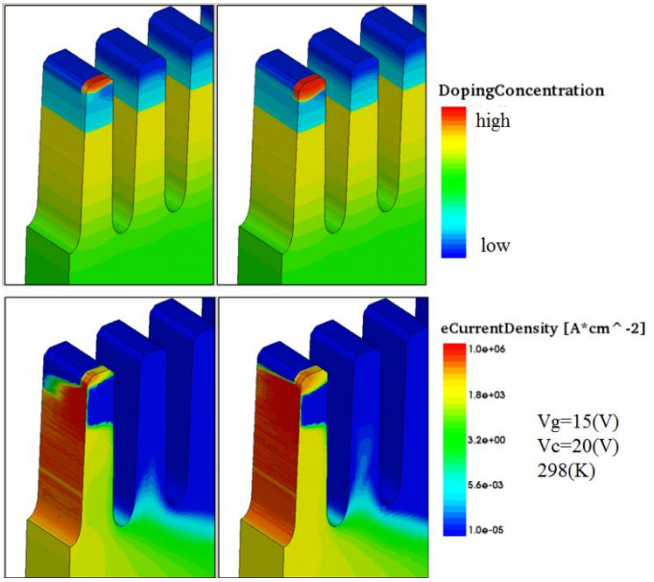

Fig. 2: Examples of the 3D current paths depending on the N+ and P+ depth ratio. The left figure is a current path of a structure having a shallow N + profile compared to P +, and the right figure is a current path of a structure having a deep N + profile.

parameters of carrier velocity saturation model in the drift region and mobility degradation model at channel interfaces without adjustments of N+ and P+ profiles (Method-1), simulated results can also reproduce the measured results of the IV-characteristics to the same extent.

Fig. 4(a) shows comparison between simulated results using Method-1 (IV-characteristics have been well calibrated) and measured results of IGBT turn-off switching waveforms with an inductive load for an example condition. It can be seen that the simulated result of the slope of Vce and the time when tail current suddenly drops are not well reproduced. The timing at which the dynamic avalanche occurs can be calibrated by adjusting the parameters of avalanche model, however then the simulation results of breakdown voltage become unreasonable obviously. The relationship between tail currents and saturation currents is also the same. It is difficult to calibrate all targets at the same time by only adjusting these parameters. As shown in Fig. 4(b) and (c), the tail current suddenly drops when the depletion layer hits the n buffer layer. Although it is difficult to see from the figure, Vce jumps up a little at that time. The main reason why no vibration is seen in the simulation results unlike the measurement results is that the first-order approximation is used in the time discretization and strong numerical damping occurs. The relationship between these phenomena and the physical model parameters becomes clear from following two simple analytical expressions obtained in [6], [7].

$$Ic = qV_S A\left(\frac{2\varepsilon Vce}{qW_B^2} - N_B\right) \quad (1)$$

where q, V_S, A, e, W_B and N_B are electronic charge, saturation velocity of hole, device active area, silicon dielectric constant, n drift thickness and n drift donor concentration, respectively. This equation is derived from a very simple approximation (Poisson equation considering the charge with the hole transportation in the depletion region) and gives a rough indication of the relationship between Ic and Vce when the

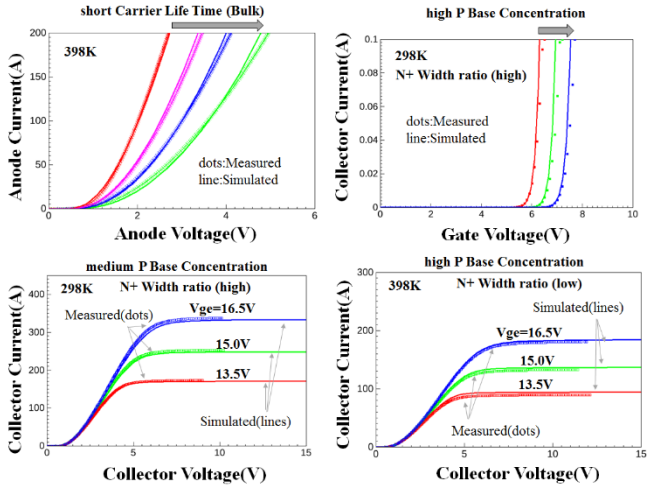

Fig. 3: Some examples of the calibrated IV-characteristics with Method-2.

depletion layer hits the buffer (dynamic punch-through condition).

$$Ic = qV_S A\left(\frac{\varepsilon E_{crit}^2}{2qVce} - N_B\right) \quad (2)$$

where Ecrit is the critical electric field. This equation represents the relationship roughly between Ic and Vce when dynamic avalanche occurs with almost no channel current flowing. The relationships between Ic and Vce represented by these expressions are shown by dashed lines in the Fig. 5(a). Curves in this figure are locus curves created from results of turn-off waveform in Fig. 5(b). The symbols (A) to (C) in the figure correspond to the points on Fig. 5(a). Since carrier saturation velocity is lowered in Method-1, two criteria in Fig. 5(a) indicate that dynamic avalanche occurs from a lower Vce, and the depletion layer reaches n buffer layer later. In other words, the smaller the carrier saturation velocity, the slower the discharge of the carrier. This points to that the calibration method of reproducing the saturation current by mainly adjusting velocity saturation model parameters is not so good for the purpose of this calibration. Fig. 6 shows the results of the turn-off switching waveforms of the IGBT for three example conditions with Method-2. The simulated results reproduce the measured results better than Method-1 with respect to the tail current length and the timing of the dynamic avalanche occurring. Using Method-2, we can reproduce saturation and tail currents of IGBTs simultaneously and easily. Therefore, Method-2 is appropriate for the purpose of this calibration, and we reaffirmed that it is important that calibrations are based on physical considerations as much as possible.

Analyzing the simulated results from the viewpoint of TCAD models, it was found that the temperature dependence of the mobility and band gap models dominate the difference in length between the tail currents of each temperature (approximately the turn-off time difference). Specifically, in this device and condition, the lattice temperature dependence of phonon scattering in the n drift region contributes about 70%, the lattice temperature dependence of hole velocity saturation contributes about 13%, and the lattice temperature dependence of the band gap contributes about 13%. On the other hand the temperature dependence of SRH recombination model (carrier lifetimes) is not a dominant

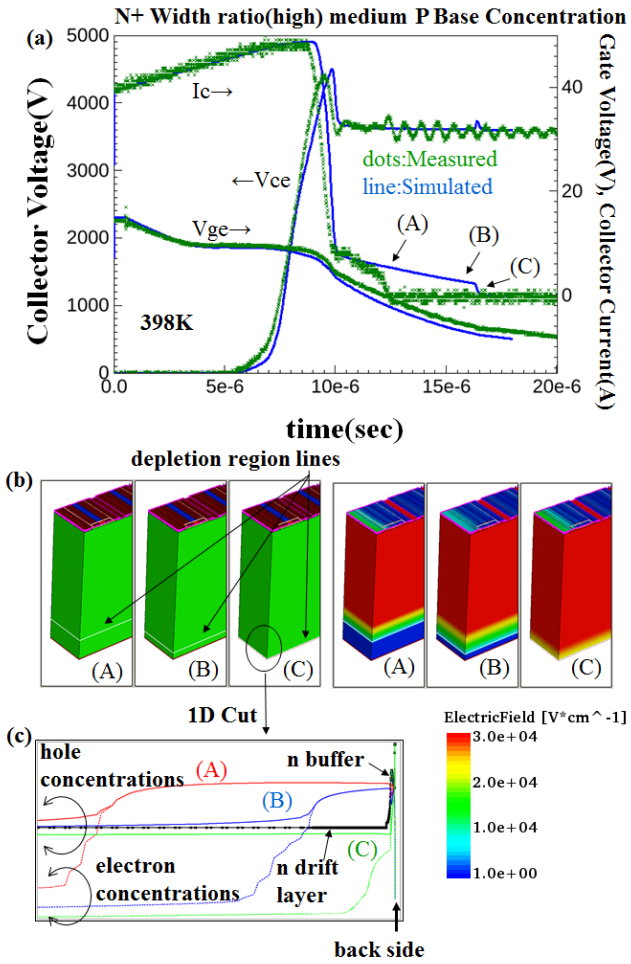

Fig. 4: Results of turn-off simulation with Method-1. (a) Comparison of simulated and measured waveforms. (b) Calculated movement of the depletion region line and distribution of electric field when tail current is flowing. Here, (A)-(C) correspond to the points on Figure (a), respectively. These figures are enlarged in the planar direction. (c) Distributions of carrier concentrations and impurities cut in the vertical direction of the circled area.

effect on the difference because of the low impurity concentrations and very long carrier lifetimes in the n drift layer of 6.5kV IGBTs.

IV. Conclusion

To clarify the key points of calibration for saturation currents and turn-off wave form of IGBTs, we calibrated with two methods and analyzed the results. In particular, using simple analytical equations, we explained that it is difficult to reproduce the electrical characteristics of the target simultaneously by the traditional calibration method of mainly adjusting the parameters velocity saturation model. In IGBT calibrations, the N + and P + profiles on the device surface side are particularly important, and we need to properly determine these profiles in 3D structures for simulations. To simplify calibration and reduce the number of meshes, we recommend a method to create 3D structures by adjusting the each depth of the N + and P + profiles in 2D process simulations so that the saturation currents reproduce the measured values. Of course, when there are obvious process or physical causes, it is also necessary to properly adjust the model parameters of channel mobility and velocity saturation.

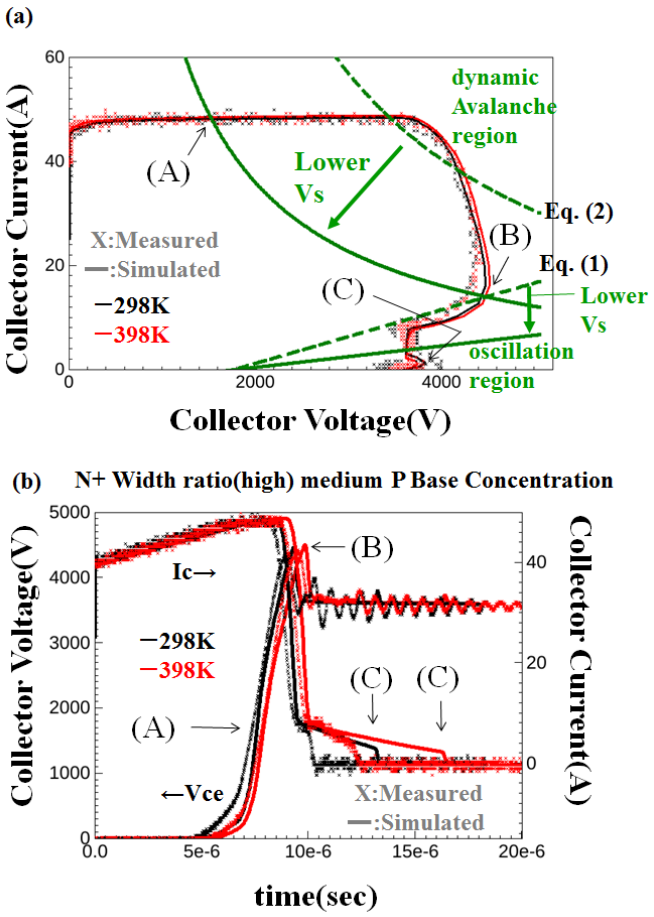

Fig. 5: (a) Locus curves of the collector current vs. the collector voltage are plotted to analyze the simulated turn-off results with Method-1 by the criteria of Ref. 1. Here, Vs represents saturation velocity of holes. (b) Turn-off waveforms that are the source of the locus curve.

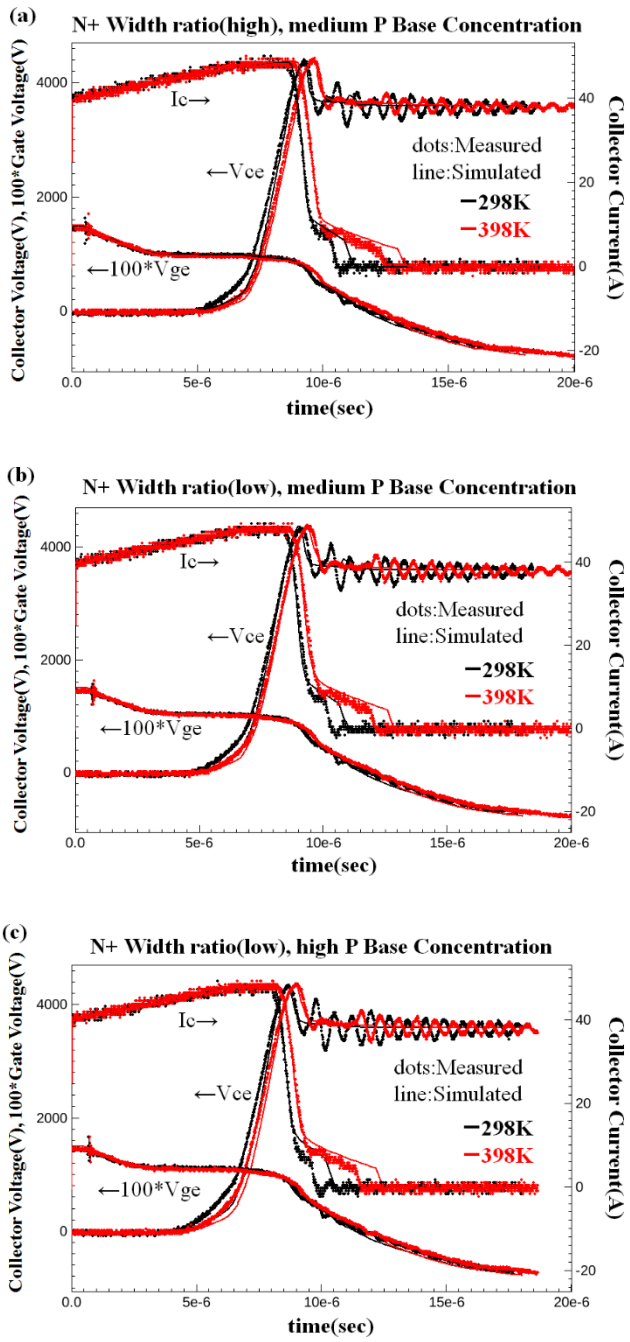

Fig. 6: Examples of turn-off simulation results with Method-2 in three conditions. The simulated results well reproduce the measured results with respect to the lengths of tail currents and the timing of dynamic avalanche occurring at each temperature compared to Method-1.

REFERENCES

[1] A. Philippou, M. Bina and F.-J. Niedernostheide, "Automated Vertical Design Optimization of a 1200V IGBT," Proc. SISPAD, 2015, pp. 72-75.

[2] M. Bina, A. Philippou, M. Hauf, Ch. Sandow and F.-J. Niedernostheide, "Automated Vertical Design Co-Optimization of a 1200V IGBT and Diode," Proc. SISPAD, 2016, pp. 185-188.

[3] M. Watanabe et al., "Impact of three-dimensional current flow on accurate TCAD simulation for trench-gate IGBTs," Proc. ISPSD 2019, pp. 311-314.

[4] M. Tanaka and A. Nakagawa, "Growth of short-circuit current filament in MOSFET-Mode IGBTs," Proc. ISPSD 2016, pp. 319-322.

[5] T. Enda and N. Shigyo, "Grid size independent model of inversion layer carrier mobility," Proc. SISPAD, 1997, pp. 319-321.

[6] T. Ogura, H. Ninomiya, K. Sugiyama and T. Inoue, "Turn-Off Switching Analysis Considering Dynamic Avalanche Effect for Low Turn-Off Loss High-Voltage IGBTs," IEEE Transactions on Electron Devices, Vol. 51, No.4, April 2004, pp. 629-635.

[7] M. Tsukuda, I. Omura, Y. Sakiyama, M. Yamaguchi, K. Matsushita and T. Ogura, "Critical IGBT Design Regarding EMI and Switching Losses," Proc. ISPSD 2008, pp. 185-188.