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Process Optimization of Trench Field Plate Power MOSFETs with Sequential Phosphorus-Doped Silicon

Kota Tomita
Advanced Discrete Development Center
Toshiba Electronic Devices & Storage Corporation
Nomi, Ishikawa, Japan
kouta.tomita@toshiba.co.jp

Tatsuya Shiraishi
Advanced Discrete Development Center
Toshiba Electronic Devices & Storage Corporation
Nomi, Ishikawa, Japan
tatsuya.shiraishi@toshiba.co.jp

Hiroaki Kato
Advanced Discrete Development Center
Toshiba Electronic Devices & Storage Corporation
Nomi, Ishikawa, Japan
hiroaki1.katou@toshiba.co.jp

Hiroyuki Kishimoto
Advanced Discrete Development Center
Toshiba Electronic Devices & Storage Corporation
Nomi, Ishikawa, Japan
hiroyuki2.kishimoto@toshiba.co.jp

Katsura Miyashita
Advanced Discrete Development Center
Toshiba Electronic Devices & Storage Corporation
Nomi, Ishikawa, Japan
katsura.miyashita@toshiba.co.jp

Kenya Kobayashi
Advanced Discrete Development Center
Toshiba Electronic Devices & Storage Corporation
Nomi, Ishikawa, Japan
kenya.kobayashi@toshiba.co.jp

***Abstract*—Sequential phosphorus doping process is expected to form decent silicon electrodes in narrow and deep trenches. We performed process optimization of FP-MOSFETs with sequential phosphorus-doped silicon. We succeeded in reducing processing variations in field plates and decreasing wafer warpage by processing phosphorus-doped silicon without activation annealing. In addition, inserting 800°C annealing before 1000°C annealing contributes no voids in silicon field plates.**

Keywords*—*sequential phosphorus-doped silicon, field plate depth variation, wafer warpage, voids in silicon electrodes, trench field plate power MOSFETs, process optimization,

I. Introduction

Trench power MOSFETs have been used in a wide variety of electronic devices. In recent years, trench power MOSFETs equipped with field plates (FP-MOSFETs) have been continuously developed in order to obtain higher performance and higher breakdown voltage [1]-[4]. At the ideal FP-MOSFETs structure, the minimum on-resistance per unit area, $R_{on}A$ [5], the breakdown voltage, V_B, and the vertical electric field, E_V, are given by

$$R_{on}A = \frac{3\sqrt{3}{V_B}^2}{4\varepsilon\mu {E_{crit}}^3} \times \frac{1}{\gamma_{FP}}. \quad (1)$$

$$V_B = E_V t_{FP}. \quad (2)$$

$$E_V = \sqrt{\frac{2}{3}}\, E_{crit} \quad (3)$$

where ε is the permittivity, μ is the electron mobility, E_{crit} is the critical electric field (about 0.3MV/cm in Si), γ_{FP} is the cell aspect ratio (t_{FP}/W_{FP}), t_{FP} is the FP thickness and W_{FP} is the lateral cell pitch as shown in Fig. 1.

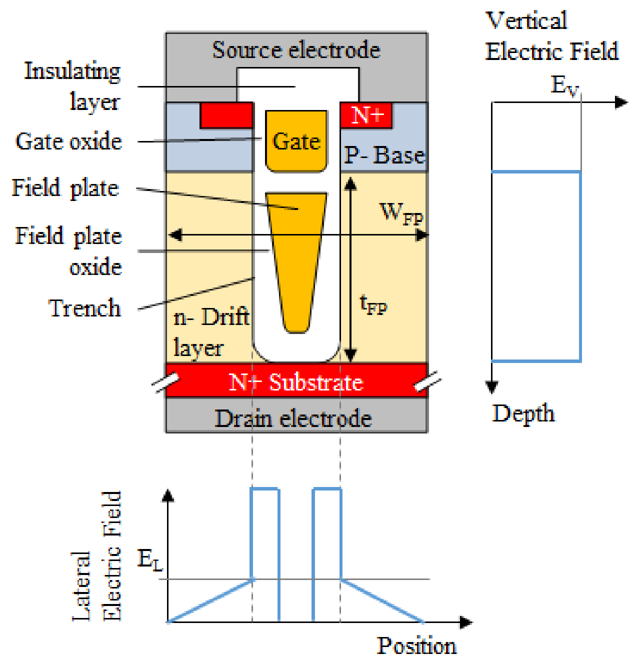

Fig. 1. Schematic cross-sectional structure of trench field plate MOSFETs (unit cell) and electric field distributions.

In order to obtain lower on-resistance, it is important to shrink the cell pitch with narrow the trench width. Improving depth variation of field plate makes it possible to suppress variation of breakdown voltage and capacitance. It is necessary to increase the trench depth in order to obtain high breakdown voltage.

The wafer warpage becomes larger with narrower cell pitch and the deeper trench, which causes manufacturing problems. In addition, it is known that voids are generated in silicon used as field plates and gates [6], which degrades device characteristics. Therefore, process optimization of the doped silicon in trench is crucial for FP-MOSFETs.

There are three methods to form silicon field plates and gates. One of the formation methods is **phosphorus diffusion**, where phosphorus is added on un-doped silicon film. After field plate oxidation (Fig. 2(a)), un-doped silicon is deposited

(Fig. 2(b)), phosphorus is diffused (Fig. 2(c)), and generated phosphate glass is removed by post-treatment finally (Fig. 2(d)). When the trench depth is deep, it is difficult to uniformly diffuse phosphorus to the bottom of field plate.

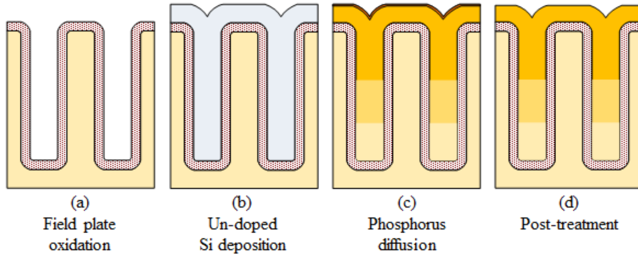

Fig. 2. Process steps of phosphorus diffusion. Schematic cross-sectional structure after (a) field plate oxidation, (b) un-doped silicon deposition, (c) phosphorus diffusion, and (d) post-treatment.

Another method is **in-situ phosphorus doping**, where phosphine gas is added together to form silicon. After field plate oxidation (Fig. 3(a)), phosphorus-doped silicon is deposited (Fig. 3(b)). In this method, however, trench filling property gets worse due to the difference of adsorption factors between source gases of silicon and phosphorus (Fig. 3(c)).

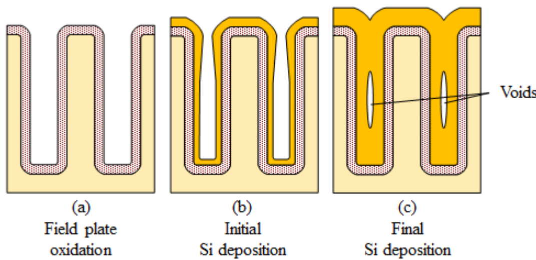

Fig. 3. Process steps of in-situ phosphorus doping. Schematic cross-sectional structure after (a) field plate oxidation, (b) initial silicon deposition, and (c) final silicon deposition.

Sequential phosphorus doping is the third method where un-doped silicon layers and phosphorus adsorption layers are deposited repeatedly (Fig. 4). This process is expected to form decent silicon electrodes in narrow and deep trenches [7][8].

In this paper, we report the process optimization of FP-MOSFETs with sequential phosphorus-doped silicon.

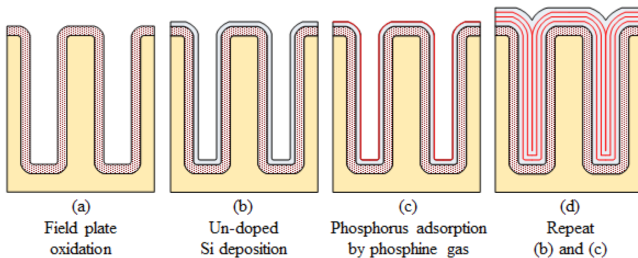

Fig. 4. Process steps of sequential phosphorus doping. Schematic cross-sectional structure after (a) field plate oxidation, (b) un-doped silicon deposition, (c) phosphorus adsorption by phosphine gas, and (d) depositing (b) and (c) repeatedly until the desired film thickness.

II. Process Overview of Sequential Phosphorus-Doped Silicon

Fig. 4 shows the process steps for sequential phosphorus-doped silicon. After field plate oxidation (Fig. 4(a)), un-doped amorphous silicon is deposited by low pressure chemical vapor deposition (Fig. 4(b)). Next, phosphine gas forms an adsorption layer on the amorphous silicon surface (Fig. 4(c)). These steps are repeated until the desired film thickness is obtained (Fig. 4(d)). In this way, by separately performing the step of forming the silicon film and the step of doping phosphorus separately, it is possible to keep the doping concentration constant up to the bottom of field plate without degrading trench filling property.

III. Process Optimization and Results

A. Depth variation of field plates

The depths of the field plate were measured for phosphorus diffusion and sequential doping with and without activation annealing by Scanning Microscope (SEM). Fig. 5(a) shows the definition of the depth and the cross-sectional images after silicon etching. Compared with phosphorus diffusion (Fig. 5(b)), sequential doping without annealing gives smoother surface roughness (Fig. 5(c)).

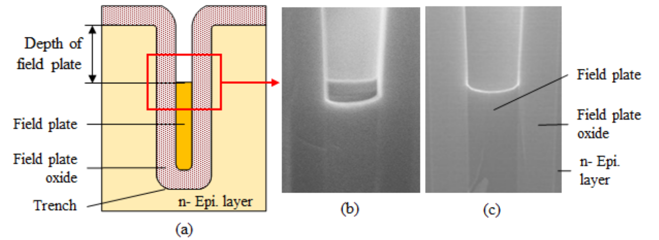

Fig. 5. (a) Definition of depth of field plate. Cross-sectional SEM images of field plate with (b) phosphorus diffusion, and (c) sequential doping without annealing.

Fig.6 shows measured depth of field plate in 100 trenches for phosphorus diffusion and sequential doping with and without annealing. Compared with phosphorus diffusion, sequential doping with annealing does not improve depth variation. On the other hand, sequential doping without annealing enables three times tighter depth variation.

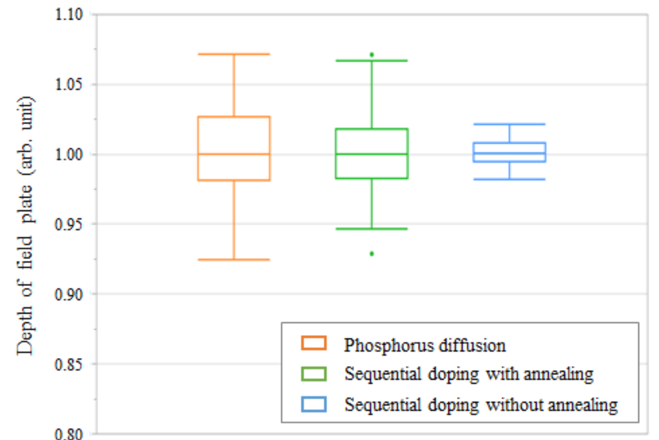

Fig. 6. Measured depth of field plate for phosphorus diffusion and sequential doping with and without annealing.

Fig.7 shows (1) cross-sectional TEM images, and (2) EDX phosphorus mapping images, for (A) phosphorus diffusion and (B) sequential doping without annealing. In phosphorus diffusion as well as sequential doping with annealing (not shown), silicon becomes polycrystalline (Fig. 7(A-1)), where poly grain worsens dry etching variation. On the other hand, silicon remains amorphous for sequential doping without annealing (Fig.7(B-1)), which improves dry etching variation. And results of EDX conforms silicon difference with difference of phosphorus atom location (Fig.7(A-2) and Fig.7(B-2)). From the viewpoint of dry etching process variation, sequential doping without activation annealing is superior for silicon field plate electrodes.

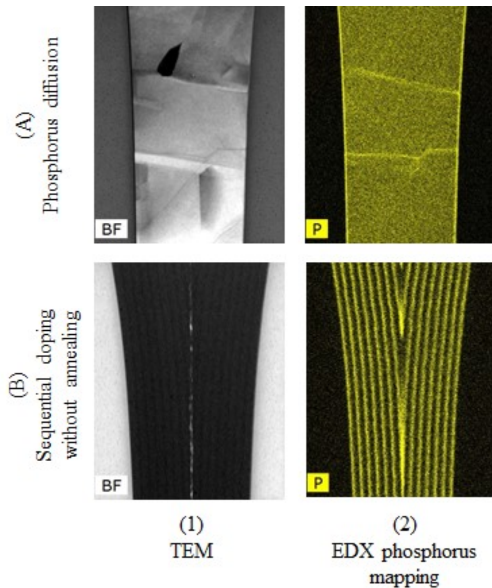

Fig. 7. (1) Cross-sectional TEM images and (2) EDX phosphorus mapping images, for (A) phosphorus diffusion and (B) sequential doping without annealing.

B. *Wafer warpage*

Definition of wafer warpage is shown in Fig. 8. In the FP-MOSFETs wafer, stripe trench patterns are extended in X-direction, and are arrayed periodically in Y-direction. The wafer warpage was measured by FLX-2320-S that is a non-contact reflection goniometry method with the laser.

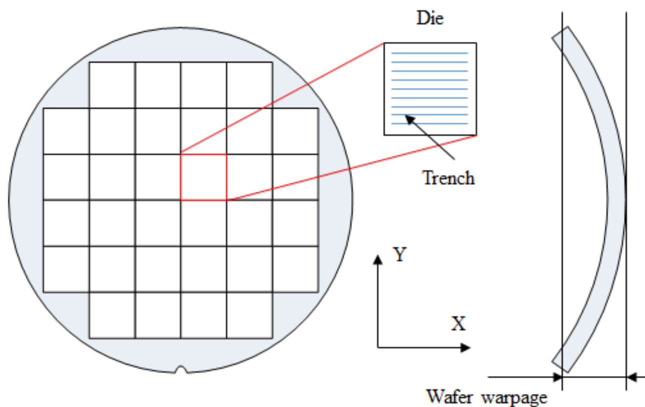

Fig. 8. Definition of wager warpage for X- and Y- directions

The wafer warpage of the Y direction, perpendicular to trench, at each process step is shown for sequential doping and phosphorus diffusion in Fig. 9. In phosphorus diffusion process, the wafer warpage crosses over convex limit for manufacturing just after field plate phosphorus diffusion (step 7 of Fig. 9(a)) and gate phosphorus diffusion (step 11 of Fig. 9(a)). On the other hand, the warpage of sequential doping sample remains within convex and concave limits through process flow (Fig 9(b)). It is because the growth of silicon crystal, resulting in increasing the expansion stress, is suppressed by lower annealing temperature [9].

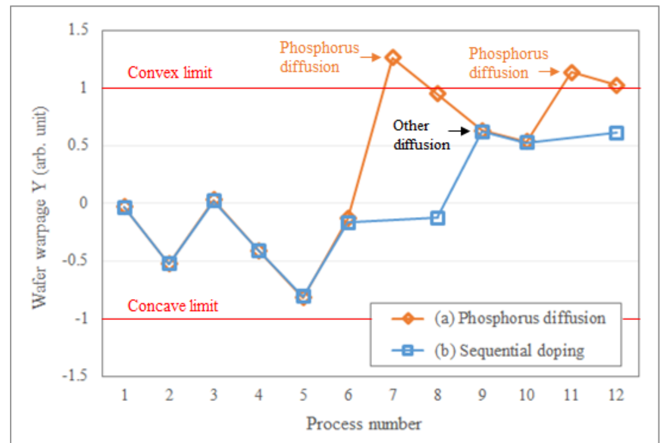

Fig. 9. Wafer warpage results for Y-direction at each process step of phosphorus diffusion or sequential doping.

C. *Voids in silicon field plates*

Finally, we also considered to optimize the annealing process for void reduction of the field plate. Based on the previous studies [10], phosphorus-doped silicon grains grow at high temperature annealing over 1000°C and contributes to decrease voids dramatically [11]. As we anticipated, the voids of the field plate after 1000°C annealing were confirmed (Fig. 10(a)). Therefore, we tried to insert 800°C annealing before 1000°C annealing, resulting in void reduction (Fig. 10(b)).

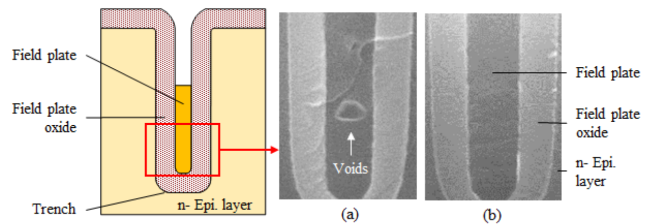

Fig. 10. Cross-sectional SEM images of field plate (a) after 1000°C annealing, and (b) with inserting 800°C annealing before 1000°C annealing.

We counted the number of trenches including voids among 100 trenches the samples with 1000°C annealing, or inserting 800°C annealing before 1000°C annealing in cross sectional SEM pictures, shown in Fig. 11. There are no voids for the sample inserting 800°C annealing before 1000°C annealing, while there are four voids for the samples with 1000°C annealing. It is considered that crystallization at intermediate temperature annealing enhances silicon atom's mobility at subsequent 1000°C annealing.

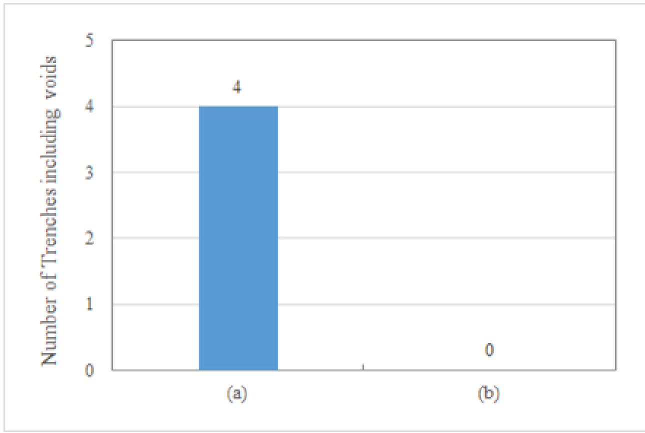

Fig. 11. Number of Trenches including voids in silicon field plates (a) after 1000°C annealing and (b) with inserting 800°C annealing before 1000°C annealing.

IV. Static Characteristics

We measured *Id-Vd* curves of FP-MOSFETs with phosphorus diffusion and sequential doping, shown in Fig. 12. The *Id-Vd* characteristic with sequential phosphorus doping matched well to conventional phosphorus diffusion. By process optimization, we demonstrated to fabricate FP-MOSFETs with sequential phosphorus doping.

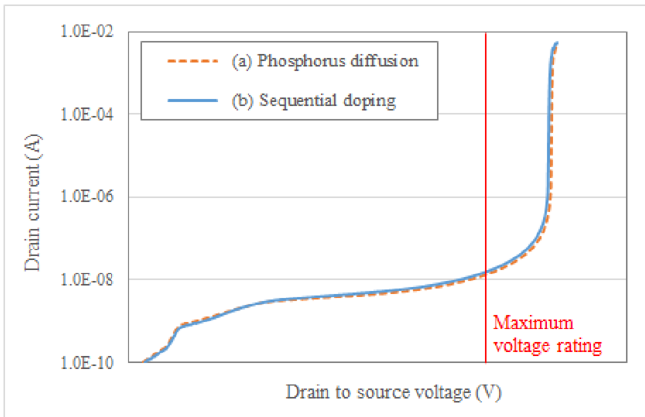

Fig. 12. Measured *Id-Vd* curves of FP-MOSFETs with (a) phosphorus diffusion and (b) sequential phosphorus doping.

V. Conclusions

Process optimization of trench FP-MOSFETs are studied with sequential phosphorus-doped silicon process. We have succeeded in reducing processing variations in field plates, and in suppressing wafer warpage and void generation with this process. The optimum conditions are processing the sequential doping without activation annealing and intermediate temperature annealing insertion before high temperature annealing. Good electrical characteristics is demonstrated with the optimized process. The new process opens the pathway to the next-generation FP-MOSFETs.

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Author Biography

Kota Tomita received master degree in engineering from Kyoto Institute of Technology in 2007, and joined Toshiba Corp. He has been an engineer of the development of power MOSFETs process integration technology.