

Automotive Semiconductor Technologies Contributing to Downsizing of Electric Power Steering Systems

The dissemination of electric power steering (EPS) systems, which use electric motors to assist the driver of a vehicle in operating the steering wheel, has progressed because of their ability to both reduce the burden on drivers and enhance the stability of automobiles running at high speed.

Moreover, since the EPS system achieves an approximately 5% reduction in fuel consumption compared with traditional hydraulic power steering systems, the number of large-sized vehicles equipped with EPS systems has been increasing as a countermeasure for global warming. In the fields of advanced driver-assistance systems (ADAS) and automated driving, the steer-by-wire system is attracting attention as a next-generation EPS system for steering control without mechanical linkage between the steering wheel and steering gear. In particular, it is important to enhance the reliability of steer-by-wire systems so as to avoid the risk of failures by ensuring redundancy of the electronic control units (ECUs). This redundancy, however, leads to a reduction in fuel consumption improvement and imposes constraints on ECU placement due to increases in the number of parts and the size of the ECUs.

To achieve the miniaturization of EPS systems, Toshiba Electronic Devices & Storage Corporation has developed a power metal-oxide-semiconductor field-effect transistor (MOSFET) for driving automotive brushless DC (BLDC) motors that achieves a reduction in on-resistance by means of a state-of-the-art field plate (FP) structure, as well as efficient heat dissipation through installation of the chip on a double-side-cooling DSOP Advance package. Furthermore, this product complies with the AEC (Automotive Electronics Council)-Q101 automotive reliability standard. We are also promoting the development of compact power MOSFET gate driver intelligent power devices (IPDs) and transient voltage suppressor (TVS) diodes for surge and electrostatic discharge (ESD) protection.

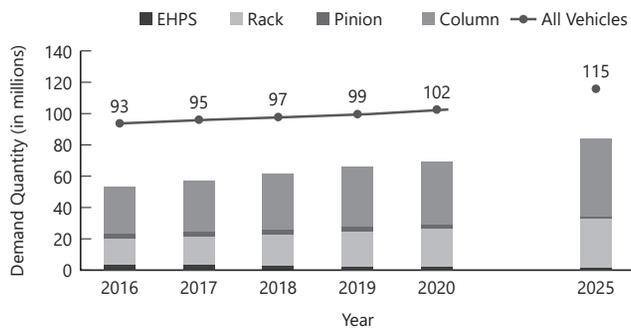
1. Introduction

Hydraulic power steering systems, which appeared in the 1960s, provided steering assistance to the driver of a vehicle and controlled the level of assistance based on the vehicle's speed. They became commonplace since they reduced the steering effort of the driver and improved cruising stability at high speed.

In the late 1980s, subcompact cars were equipped with electric power steering (EPS) systems in response to the trend in fuel economy. Till the 2000s, column-assisted EPS systems suitable for compact cars were the main stream. Following

column-assisted EPS systems came rack-assisted EPS systems whose steering assistance mechanism is integrated with the steering rack housing on the wheel axle to reduce mechanical friction and thereby improve steering performance⁽¹⁾. In addition, conventional brushed DC motors were replaced by BLDC motors, which eliminated the need for a brush and a commutator. BLDC motors that excel in service life, maintainability, quietness, and controllability came into increasingly widespread use in medium-sized and heavier vehicles.

In the 2010s, regulations concerning global warming and fuel economy have been tightened worldwide. Since an EPS system provides an approximately 5% reduction in fuel consumption, the percentage of vehicles equipped with an EPS system, which currently stands at roughly 60%, is expected to increase (Figure 1)⁽²⁾.



EHPS: Electric hydraulic power steering

*Based on *Electric Power Steering Systems Market 2017*⁽²⁾ Yano Research Institute Ltd.

Figure 1. Trends in number of automobiles and automobiles equipped with EPS systems

The percentage of automobiles equipped with an EPS system, which provides an approximately 5% reduction in fuel consumption, is expected to increase from 61% in 2017 to 73% in 2015.

Furthermore, accompanying the progress of advanced driver assistance system (ADAS) technology and automated driving, EPS systems are becoming increasingly sophisticated, incorporating steering angle and vehicle behavior controllers. In addition, as coordination of a steering system with propulsion, braking, and integrated vehicle control systems becomes important, the uptake of linkless steer-by-wire systems, which also help expand the cabin space, is expected to increase⁽³⁾.

As ADAS and automated driving become more sophisticated, an electrical disconnection from system power or a failure to provide steering assistance could have serious consequences. According to the definitions of the Automotive Safety Integrity Level (ASIL) of the International Organization for Standardization (ISO) 26262 standard, an international standard for functional safety of electrical and/or electronic systems in production automobiles, EPS systems are assessed as having a severity of S3 (life-threatening injuries), an exposure of E4 (high probability), and a controllability of C3 (difficult to control or uncontrollable). Consequently, EPS systems are classified as ASIL D for which the highest integrity is mandatory.

To reduce risk, dual redundancy is used for electronic control units (ECUs) and BLDC motors so that, in the event of a failure of the main system, the backup system steps in to maintain the steering ability and allow the driver to safely stop the vehicle (Figure 2). Moreover, as the automotive industry works toward the realization of fully automated driving, discussion has begun on triple redundancy that is the norm for safety-critical systems in aircraft (Table 1).

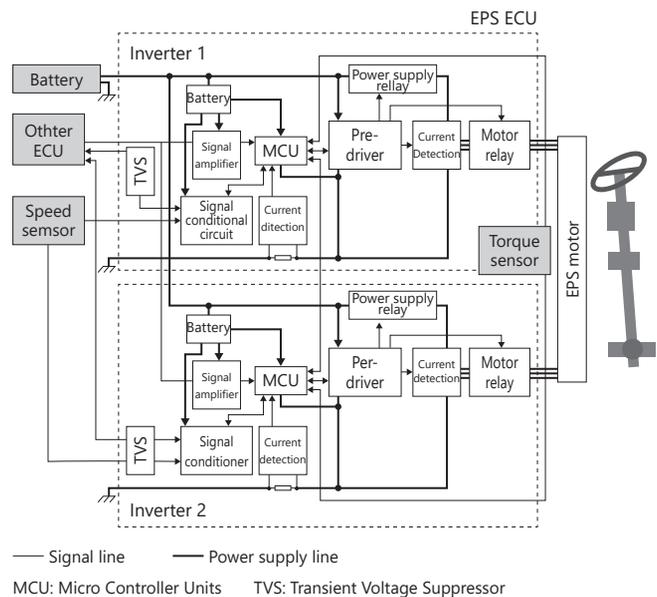


Figure 2. Configuration of EPS system with redundancy

The EPS system provides functional safety since it maintains the cruising performance of a vehicle by activating a backup inverter if the main inverter fails.

Table1. Future outlook for EPS systems

Item		2015 to 2020	2020 to 2025	2025 to 2030	
Environment	Fuel efficiency restrictions (g/km)	Europe	130	95	70
		U.S.	146	101	89
		China	159	116	93
		Japan	136	114	→
EPS	Assist system	EPS			
	Type	Column or Rack			
	Motor	Brushed or brushless	Brushed	Brushed	
Safety	Automated Driving	Level2 (partial)	Level3 (conditional)	Level4 (high)	
	EPS Redundancy system	Two inverters One MCU ^(*)	Two inverters Two MCUs	N inverters N MCUs	

N : Number of redundancy systems

*In the use of brushless DC motors

2.Semiconductor technologies supporting EPS systems

An increase in the output power and current ratings of a motor and the need for redundancy cause an increase in the number of components required, resulting in an increase in the size of an ECU for an EPS system. However, the quantity of in-vehicle electronic equipment is increasing because of the need for powertrain, in-vehicle and out-of-vehicle communication, and other advanced automotive electronics systems, making it difficult to allow sufficient space for an EPS system.

To resolve this conflict, mechanical-electronic integration of a motor and an ECU is proceeding for EPS systems, spurring demand for small, high-density surface-mount devices (SMDs).

In response, Toshiba Electronic Devices & Storage Corporation has developed small SMDs of power MOSFETs for EPS ECU applications, with up to 22 pcs at the output stage, and MOSFET pre-drivers.

2.1 MOSFET chip technology

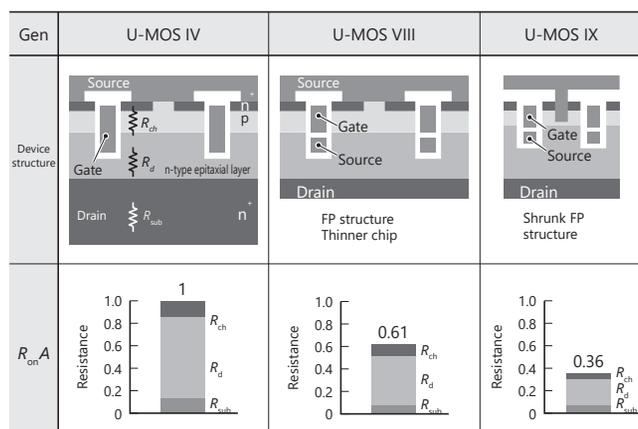
For power MOSFETs that are used as switching devices at the output stage, it is necessary to reduce conduction loss in the on-state and transient switching loss. Typical silicon power MOSFET chips have a vertical structure. Their on-resistance (R_{onA}), which causes conduction loss, consists of channel resistance on the chip surface (R_{ch}), drift resistance (R_d), and substrate resistance (R_{sub}) (Figure 3).

Up until the U-MOS VII-H generation, we had reduced R_{ch} by shrinking our proprietary trench-gate structure based on LSI and memory process technologies.

The U-MOS VIII and subsequent processes use a field plate (FP) structure that allows the drift layer resistance to be reduced through heavy doping because of the effect of electric field relaxation on the bottom of the trench, considerably reducing R_d . In addition, to reduce R_{sub} , we have reduced the chip thickness of the U-MOS VIII process to roughly 50 μm , more than 50% thinner than that of the U-MOS IV process. As a result, the on-resistance (R_{onA}) of U-MOS VIII is 39% lower than that of U-MOS IV.

To further shrink the FP structure, the latest U-MOS IX process uses a self-aligned trench contact structure and tungsten filling technology, which help optimize multiple design

factors, including oxide thickness, a wafer's specific resistance, and trench depth. As a result, the on-resistance (R_{onA}) of U-MOS IX is 64% lower than that of U-MOS IV (Figure 3).

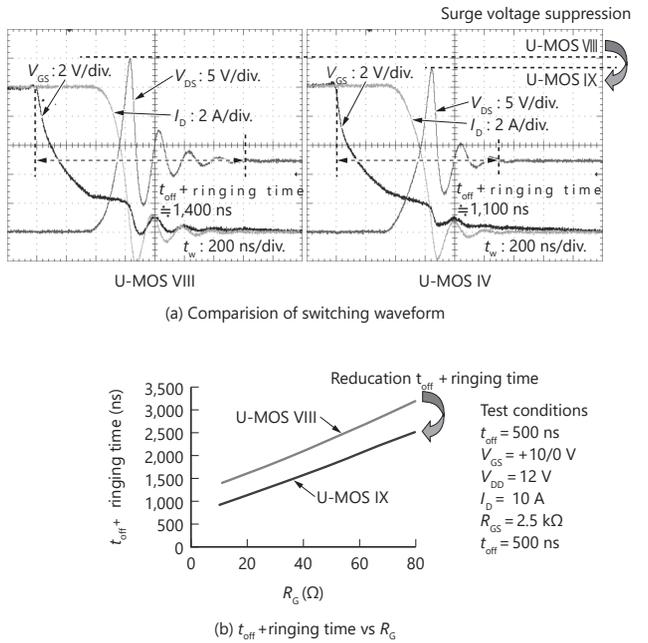


p : p-type semiconductor n : n-type semiconductor
 * R_{onA} values are normalized such that the R_{onA} of U-MOS IV is equal to one

Figure 3. Changes in structure and on-resistance of MOSFETs

The latest U-MOS IX process provides 64% less R_{onA} than the U-MOS IV process through a shrank FP structure, optimized design factors, and chip thinning.

However, a reduction in R_{onA} causes an increase in junction capacitance as the chip size and integration levels increase. An increase in junction capacitance not only causes an increase in the switching loss of a motor controller circuit for an EPS system, but also leads to motor torque ripples if a long dead time is inserted to avoid the cross conduction of the upper and lower arms of a bridge circuit. In other words, to reduce the dead-time period, it is necessary to reduce junction capacitance that has a trade-off with R_{onA} . Furthermore, transient voltage surges and ringing (signal oscillation) during switching cause electromagnetic interference (EMI), increasing radio noise and other interfering factors. The U-MOS IX process optimizes design factors to suppress the surge voltage and ringing time during switching so as to achieve low noise (Figure 4).



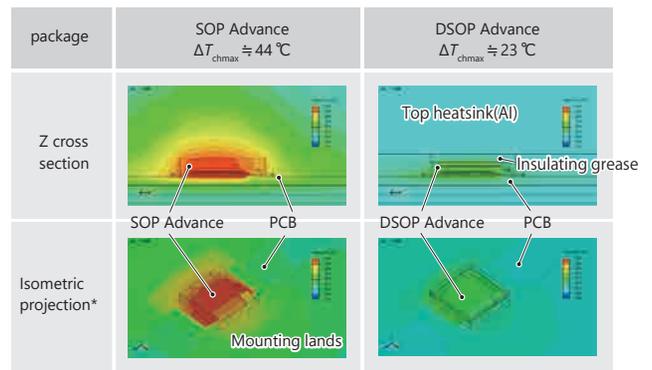
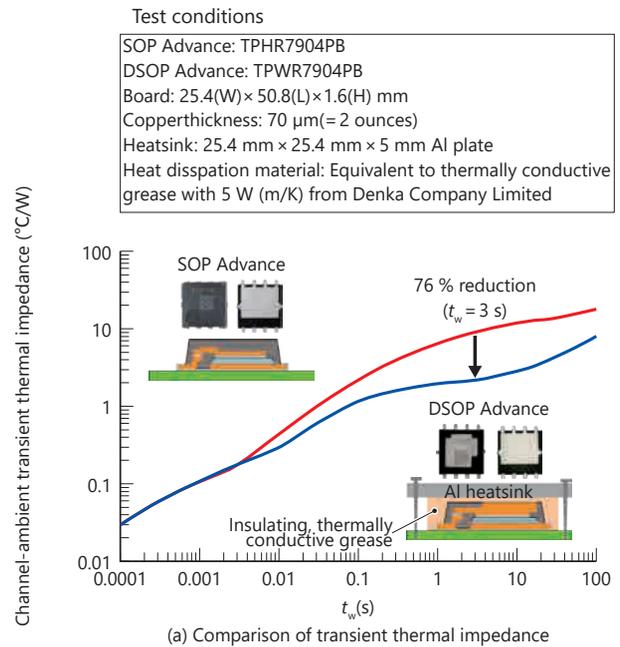
div: division
 V_{GS} : Gate-source voltage
 t_{off} : Turn-off time
 V_{DD} : Supply voltage
 V_{DS} : Drain-source voltage
 R_{GS} : Gate-source resistance
 I_D : Drain current
 R_G : Gate series resistance

Figure 4. Switching characteristics of U-MOS IX

U-MOS IX provides lower noise levels than U-MOS VII because of more effective surge voltage suppression and shorter ringing time.

2.2 MOSFET packaging technology

We have changed the source wiring material of the package from a conventional aluminum (Al) ribbon for ultrasonic bonding to a low-resistivity copper (Cu) connector for soldering. Consequently, the new 8-pin small-outline package (SOP) with a Cu connector measuring 5 × 6 mm has resistance 0.35 m Ω lower than that of the conventional package. We have also developed the 8-pin DSOP (double-sided-cooling SOP) Advance package of a similar size with a thicker Cu connector exposed on top, which provides heat dissipation paths not only from the package bottom to a printed circuit board (PCB) but also from the package top to a heatsink via an insulating material. The structure and manufacturing process of the DSOP Advance package have been optimized so that application of stress to the interior of the package during the



Applied power dissipation=2W, steady state
 Ambient temperature: $T_a = 25^{\circ}\text{C}$
 PCB size: 100(L) × 70(w) × 1.6(H)mm
 Cu interconnect layers: 4 layers (70 μm thick par layer)
 DSOP Advance package with top heatsink (Al)
 Top heatsink size: 100(L) × 70(w) × 5(H)mm
 Difference in size between package and top heatsink: 0.5mm
 Thermally conductive grease: 5W/(m/K)

* Top heatsink and thermally conductive grease of DSOP package are hidden

(b) Comparison of thermal simulation results

Figure 5. Thermal characteristics of Advance package

DSOP Advance exhibits roughly 76% less transient thermal impedance than SOP Advance. In addition, thermal shows that DSOP Advance resulted in roughly 21 $^{\circ}\text{C}$ reduction in ΔT_{chmax} .

manufacturing process will not damage a chip because of the exposed Cu connector.

Consequently, the transient thermal impedance of the DSOP

Advance package is approximately 76% lower than that of the SOP Advance package for a stationary steering time (t_w) of three seconds expected for an EPS system (Figure 5(a)). A thermal simulation of an on-board DSOP Advance package assuming the use for an EPS system indicates that it helps reduce a rise in channel temperature (ΔT_{chmax}) by roughly 21°C at a steady-state power dissipation of 2 W (Figure 5(b)).

2.3 MOSFET reliability technology

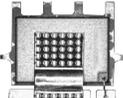
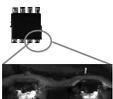
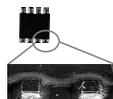
As ECUs are installed throughout a vehicle, semiconductor devices may be used in an engine compartment. It is therefore necessary to guarantee the operation of semiconductor devices at a storage temperature (T_{stg}) of up to 150°C and a peak channel temperature (T_{ch}) of up to 175°C. These temperature requirements must be satisfied to achieve compliance with the AEC-Q101-REV-D1 standard of the Automotive Electronics Council (AEC), an organization based in the United States that sets reliability qualification standards for automotive electronic components. To comply with AEC-Q101-REV-D1, we prioritize robust design, validation of the regulated characteristics, and detailed product conformance testing.

We also verify long-term reliability beyond AEC-Q101 and have specifications for the level of resin delamination on the chip surface at major milestones of reliability testing. The power MOSFET measuring 5 × 6 mm described in Section 2.2 has a unique resin adhesion structure, which did not show any resin delamination above a chip after a temperature cycling test (TCT) of 1,000 cycles (Figure 6).

Furthermore, this power MOSFET is compatible with automated optical inspection (AOI) systems for PCB-component soldering because of its wettable flank (WF) plated leads. The WF leads provide increased soldering strength. A TCT for soldering joints (2,500 cycles, -40 to 125°C) shows an improvement in their solderability.

2.4 Pre-drivers

We choose an optimum device structure according to the intended applications and required specifications. Two process platforms are currently available: a 0.13-μm BiCD

Characteristics	DSOP Advance	Conventional package	Benefit
External appearance			-
Internal structure			0.35 mΩ reduction in package resistance
Pin appearance			WF structure ⇒ Improved AOI visibility
PCB mounting examples			
SAT image after 1,000 temperature cycles*1	 No delamination	 Partial deamination	Reduced delamination
SAT image after 2,500 temperature cycles*2	 Percentage of crack length ≈ 30%	 Percentage of crack length ≈ 80%	Improved PCB mounting length

SAT: Scanning acoustic tomography

*1: TCT in unmounted condition: Ta = -55 to 150 °C

*2: TCT in mounted condition: Ta = -40 to 125 °C

Figure 6. Comparison of features of conventional and DSOP Advance packages

The low-resistivity Cu connector, WF structure, and proprietary resin adhesion structure provide the DSOP Advance package with high performance and high reliability.

process platform (that integrates bipolar, complementary metal-oxide-semiconductor (CMOS), and lateral double-diffused MOS (LDMOS) processes) and a 0.13-μm CD process platform (that integrates CMOS and LDMOS processes)⁽⁴⁾.

The TPD7212F, a newly developed six-channel MOSFET gate driver for EPS applications, is fabricated with the 0.13-μm BiCD process. Incorporating short-circuit protection and diagnostic functions, the TPD7212F is housed in the WQFN32 package that is roughly 75% smaller than the conventional

package and AEC-Q100 qualified. We have also released the TB9081FG, an 11-channel pre-driver with a built-in self-test (BIST) circuit fabricated with the 0.13- μm CD process that helps achieve the ASIL-D functional safety level. These devices allow designers to select a suitable pre-driver according to functional requirements.

We will continue to develop semiconductor processes that satisfy various environmental and market requirements for automotive applications. In the next phase of this work, we intend to incorporate protection against parasitic operation under negative voltage surge and other negative voltage conditions and develop a low- R_{on} A double-diffused MOS (DMOS) process to further improve performance.

2.5 Protection devices

TVS diodes are used to protect automotive high-precision ECUs from noise and electrostatic discharge (ESD) so as to

prevent system malfunction and semiconductor device destruction. To enable the use of TVS diodes for automotive applications, it is necessary to optimize their total capacitance (C_t) to meet the requirements of in-vehicle LAN standards, including Controller Area Network (CAN), Local Interconnect Network (LIN), FlexRay, and Low-Voltage Differential Signaling (LVDS). It is also necessary to improve the trade-off between the dynamic resistance (R_{dyn}) and ESD immunity (V_{ESD}) of TVS diodes to protect downstream devices and the whole system. In response, we have successively improved our proprietary ESD Array Process (EAP) to improve this trade-off for low-capacitance TVS diodes. The R_{dyn} of the fifth-generation EAP-V is 0.5 Ω , roughly 70% lower than that of the second-generation EAP-II with an R_{dyn} of 1.5 Ω whereas EAP-V provides a V_{ESD} of 20 kV, roughly 1.7 times higher than that of EAP-II with a V_{ESD} of 12 kV. Consequently, EAP-V has higher protection performance and signal integrity than Level 4 of IEC 61000-4-2.

3. Conclusion

The progress of power devices and integrated circuits (ICs) is essential to support EPS systems that are becoming increasingly sophisticated owing to the progress of ADAS and automated driving.

Power supply systems are also becoming increasingly

diverse, as typified by 48-V systems and electric vehicle (EV) batteries with different voltages. We will continue to provide semiconductor technologies in a timely manner while following the trend in EPS systems that work increasingly closely with various ECUs.

References

- (1) Matsuoka, H. 2015, "Development and Future Outlook of Steering Systems." JTEKT Engineering Journal (1013): 10-15
- (2) Yano Research Institute Ltd. 2017. Electric Power Steering Systems Market 2017: 188
- (3) MARKLINES. "JSAE Exposition 2017: Advances in electric power steering" Accessed July 13, 2018.
https://www.marklines.com/en/report/rep1602_201706.html.
- (4) Yamaguchi, M. et al. 2017. "Trends in and Future Outlook for Semiconductor Devices with Enhanced Energy Efficiency." Toshiba Review: 72(5): 2-7. Accessed July 13, 2018.
https://www.toshiba.co.jp/tech/review/2017/05/72_05pdf/a02.pdf.