Reliability and Analysis Technologies to Improve Quality of Automotive Semiconductor Products

The increasing sophistication of in-vehicle electronic equipment resulting from the progress of technologies for automotive electronics and electroactuation in recent years has given rise to the need for automotive semiconductor products with high quality aimed at achieving zero defects. It is therefore necessary to implement quality and reliability improvement activities at the stage of development and design as well as at the mass-production stage.

In the development of automotive semiconductor products, Toshiba Electronic Devices & Storage Corporation is applying the following technologies to attain high quality at the design stage: device structure optimization to improve the reliability of each product, advanced technology to estimate reliability using a test element group (TEG) pattern, and a screening method to detect potential defects. In order to improve upstream design quality, we have also been focusing on development using operating analysis technologies, including lock-in thermography (LIT) and time-resolved emission (TRE) microscopy, as well as improvement of the defect position identification method, taking into consideration the effect of X-ray irradiation.

1.Introduction

Increasingly sophisticated in-vehicle systems are driving the need for automotive semiconductor devices with zero-defect quality. To achieve zero defects, it is essential not only to improve quality management in the production process but also to build quality and reliability into semiconductor devices early at the stage of development and design so as to facilitate the detection and analysis of defects. As outsourcing of silicon (Si) wafer fabrication, assembly, and test processes increases, it is also necessary to require subcontractors to maintain high-quality and high-reliability management systems matching the automotive grade. Furthermore, by engaging with customers throughout the entire flow from development to quality management in the production process, it becomes possible to provide them with highly reliable automotive semiconductor devices and thereby help improve the functionality of their in-vehicle systems.

Toshiba Electronic Devices & Storage Corporation uses the Internal Quality System (IQS) incorporating quality gates for the development of semiconductor devices[1]. Based on IQS, we conduct design reviews at each milestone of the development process and reduce iterations due to mistakes so as to assure high quality and reliability levels.

This report describes our reliability and analysis technologies to further improve the quality and reliability of automotive semiconductor devices.

2. Initiatives to improve reliability technology

Manufacturers of automotive semiconductor devices commonly refer to AEC-Q100 (for integrated circuits)[2] and AEC-Q101 (for discrete semiconductors)[3] from the Automotive Electronics Council (AEC), an organization based

in the United States that sets qualification standards for the supply of automotive electronic components. The reliability of automotive semiconductor devices is generally qualified in accordance with these standards. To obtain satisfactory results in reliability qualification tests, it is essential to identify reliability requirements for a product at the stage of development and design of its constituent technology elements, devise test plans based on such requirements, and realize a product that satisfies the required specifications, including those for service life corresponding to each failure mode.

2.1 Development initiatives to improve reliability of devices for power ICs

One concern is that electromigration could degrade the reliability of lateral double-diffused metal-oxide -semiconductor field-effect transistors (FETs)(hereinafter referred to as "LDMOS") mounted on power ICs that drive large currents. Electromigration is the diffusion and movement of atoms caused by the collision of electrons with metal atoms at high temperature. As shown in **Figure 1**, by using a design that suppresses the overlap of the lower layer (Layer 1 and Layer 2) of the laminated wiring, the number of required through-hole connections (vias) whose current density tends to increase can be reduced, thereby increasing the allowable current density of the entire LDMOS[4].

We have clarified the mechanism of why hot-carrier injection [*1] in an LDMOS causes an increase in off-leak current, resulting in an increase in power consumption or a circuit malfunction.

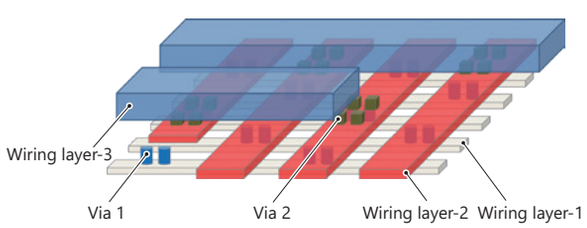
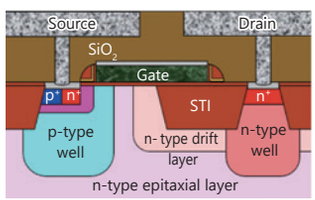


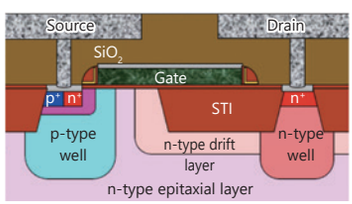
Figure 1. Layout of wiring layers in power integrated circuit (IC) with LDMOS

A design that avoids current concentration by reducing the overlap between wiring layer-1 and 2 suppresses the partial increase in current density on upper layers.

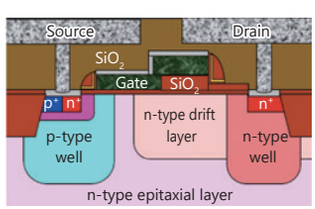
We have also verified that, in the case of an n-channel 0.13-μm LDMOS, an increase in off-leak current can be reduced by using new device structures such as an extended shallow-trench-isolation (STI) structure having a wider STI region above the n-type drift layer or a stepped-oxide structure having a stepped gate dielectric above the n-type drift layer (**Figure 2**)[5]. These newly developed structures help improve the reliability of an LDMOS and thus prolong its useful life.



Conventional structure

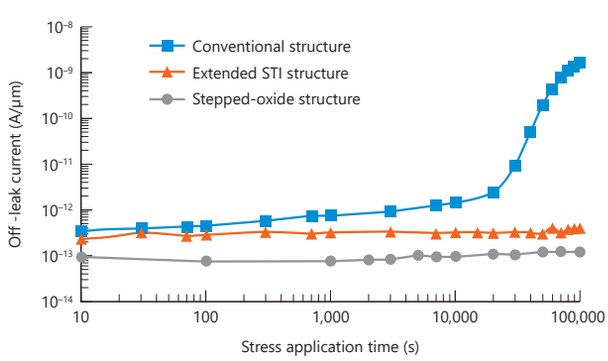


Extended STI structure



Stepped-oxide structure

(a) LDMOS structure



(b) Off-leak current curves

SiO_2 : Silicon oxide

Figure 2. Improvement in off-leak current of LDMOS devices with different structures

LDMOS devices with newly developed extended STI and stepped-oxide structures exhibit lower off-leak current than those with the conventional structure.

2.2 Mission profile and reliability estimation

In recent years, automotive electronics manufacturers have been using a mission profile that specifies various mission segments with different environmental conditions, making it necessary to tailor reliability test schemes for semiconductor devices to the mission profile. The reliability of a semiconductor device can be estimated based on the results of tests using accelerated models. However, the automotive mission profile covers a temperature range of up to 150°C whereas silicon wafer fabrication plants (foundries) generally specify the reliability test conditions at 125°C. It is true that the reliability of a semiconductor device at higher temperature can be estimated based on a temperature-time relationship, but to determine device reliability more accurately, it is essential to verify the suitability of acceleration conditions based on the results of an actual stress test. It is therefore necessary to obtain additional reliability data from silicon wafer foundries or evaluate device reliability using a TEG, a collection of test elements formed on semiconductor wafers. This is the background to our establishment of an environment for the evaluation of a TEG so as to accommodate increasingly complicated reliability estimation conditions.

2.3 Example of enhanced test screening

Semiconductor devices that have passed their final manufacturing test exhibit an early failure in the market in rare cases. To avoid early failures, it is crucial to screen silicon wafers and finished semiconductor devices.

Burn-in is one of the typical major screening methods. It is a testing process in which certain failures are forced to occur in a short period of time through application of excessive burn-in stress. The purpose of a burn-in test is to remove particular devices subject to an early failure.

However, there are types of failures that do not exhibit a simple change in electrical characteristics under stress. If a device satisfies its specifications as a result of both low-temperature and high-temperature burn-in tests, it cannot be rejected as a defective device. However, a temperature gradient test (TGT), which evaluates sample-to-sample variations in the results of measurement at different temperatures, helps detect potentially defective devices that exhibit behavior different from that of other samples. **Figure 3** shows an outline of a screening method using temperature gradients. TGT is capable of detecting defective devices caused by local flaws that occur as a result of an inadequate lithography or etching process[6].

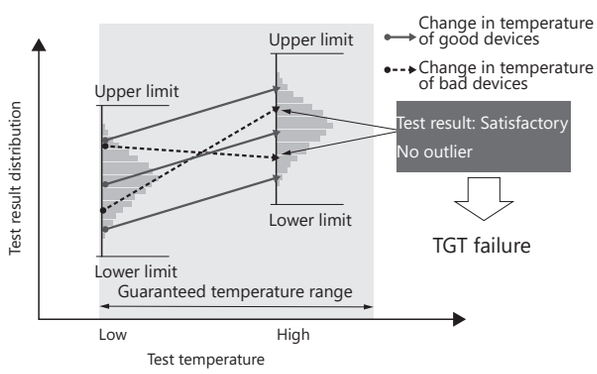


Figure 3. Example of screening by means of temperature gradient test (TGT)

Nonconforming devices can be identified by detecting samples that do not exhibit linear changes in electrical characteristics under both low-temperature and high-temperature test conditions.

3. Analysis improvement efforts: Analysis method of operating devices and concept of improvement of design

If a failure occurs in a semiconductor device during development or after shipment, a failure analysis is generally conducted to identify its cause, with the goal of determining corrective actions. A failure analysis is performed as follows.

First, a failure mode is identified based on electrical characteristic data and past cases. Next, a sample is disassembled and the details are adjusted. Furthermore, the failure mechanism is inferred and verified from this result.

Finally, fundamental measures are taken, including design changes.

However, since semiconductor devices for automotive applications may be used in new ways and their operating environment is continually changing, it may be difficult to find similar past incidents or make rational inferences. When it is difficult to infer a failure mechanism based on past incidents, simulation is a way of determining a solution[7]. When developing devices, simulation may be useful for elucidating faulty operations that are attributable to defects in the device structure or that occur under certain usage conditions. However, to conduct sufficient verification, simulation requires a physical model that provides an explanation of a failure phenomenon.

Power devices for automotive applications consist of many basic structural elements connected in parallel. It is therefore difficult to detect an imbalance among these elements based only on electrical characteristics. In the case of a power device, it is effective to perform in situ observation during operation. It becomes possible to recreate physical models once a faulty operation is sufficiently analyzed. Eventually, we use the flow shown in **Figure 4** to improve the design quality at an early stage. As described above, efforts to improve analysis technology will lead to an improvement in the ultimate reliability of semiconductor devices.

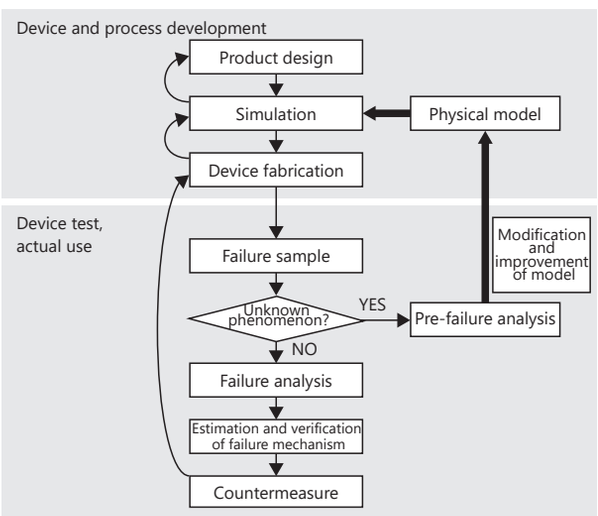


Figure 4. Flow of product development quality improvement using Pre-failure analysis

Quality improvement flow that reconstructs the physical model using the method of Pre-failure analysis improves the quality early at the stage of development and design.

3.1 Example of analysis of heating and photon emissions

Figure 5 shows an example of the results of LIT observations of an n-channel power metal-oxide-semiconductor field-effect transistor (MOSFET) designed with a target withstand voltage of 600 V or greater that exhibited a leakage defect [8]. Each image in Figure 5 is a color-coded signal map showing temperature change on the surface area of the same chip. At a drain-source voltage (V_{DS}) of 300 V, hot spots began to appear as dots at the upper right portion of the chip, as highlighted by a dashed red circle. At 639 V, two heating patterns were observed to cross the chip diagonally. From these LIT observations, we inferred that leakage defects resulted from two causes.

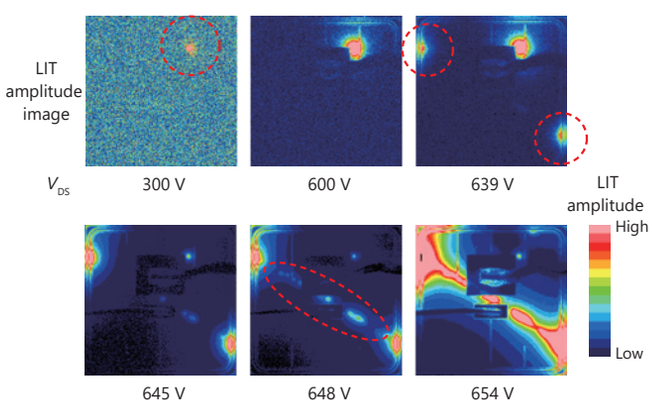


Figure 5. LIT observation of MOSFET with leakage defects

The MOSFET leak defects were investigated using LIT.
Two heat generation points were found as V_{DS} increased, showing that there were two kinds of abnormalities.

Figure 6 shows an example of the results of TRE microscopy observations of photon emissions caused by an avalanche breakdown current in an insulated-gate bipolar transistor (IGBT)[9]. TRE imaging was performed for a period of 0.25 µs at an interval of 0.75 µs to observe a corner of the chip. Figure 6 shows that the photon-emitting area moved with time. As indicated by many simulation reports, observations of an actual device also verified that the region of current concentration moves as time advances.

We have been continually studying analysis technologies and evaluation environments that allow us to determine whether a device operates properly for new applications and under different bias conditions.

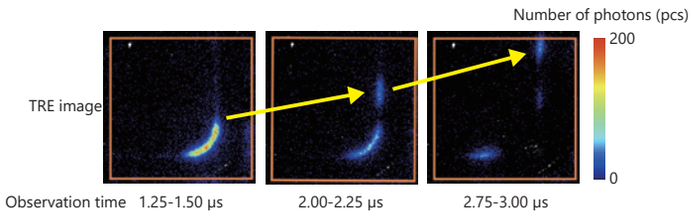
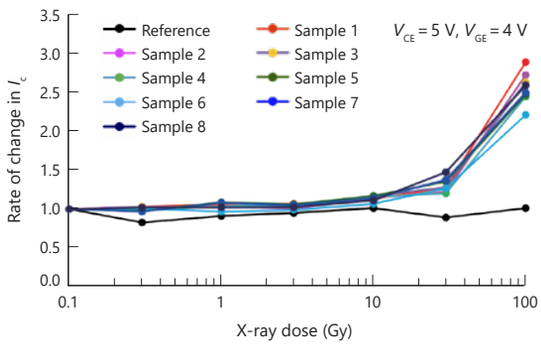


Figure 6. Results of TRE microscopy observations of photon emissions caused by avalanche breakdown current in IGBT

Photon emissions caused by avalanche breakdown current in an IGBT were observed using a TRE microscope. TRE images revealed that the location of current concentration moved after it occurred.

3.2 Effect of X-ray irradiation

X-ray computed tomography (CT) is effective in examining internal abnormalities of a semiconductor device without decapsulating its package. In particular, an X-ray CT system with a micro-focus X-ray tube provides transmission images at a magnification of up to several thousand times. It is used in combination with LIT and other systems to identify the causes of device failure. However, there is concern about the effect of X-ray irradiation on a semiconductor device. Since irradiating samples of a semiconductor device from a short distance or for an extended period of time affects their electrical characteristics, it is necessary to minimize X-ray-induced damage.



V_{CE} : Collector-emitter voltage
V_{GE} : Gate - emitter voltage

Figure 7. Changes in collector current of IGBT by X-ray irradiation

When IGBTs were irradiated by X-rays, I_c began to increase at 30 Gy and increased more than twofold at 100 Gy.

Figure 7 shows the changes in the collector current of IGBT samples when they were irradiated by X-rays. Collector current (I_c) began to increase at 30 Gy and increased more than twofold at 100 Gy. In addition, a change in the MOSFET threshold voltage occurred at 100 Gy whereas a change in flatband voltage was observed at 1,000 Gy. When performing a failure analysis, we determine whether there is a need to reduce the effect of long X-ray irradiation so as not to affect the electrical characteristics of a semiconductor device and we select appropriate analysis procedures and conditions so that the causes of device failure are not compromised.

4. Conclusion

As reported herein, reliability and analysis technologies for automotive semiconductor devices encompass a wide variety of techniques, including a reliability evaluation prior to development; reliability estimation tailored to the requirements of a mission profile; temperature-gradient screening; analyses of device operation using LIT and TRE; reviews of an analysis flow aimed at improving a device design; and an evaluation of the effect of X-ray irradiation on an analysis. By using these technologies, we have succeeded in building quality into semiconductor products early at the stage of development and design and improving our capability of identifying failure locations.

As automotive electronics become increasingly sophisticated, new silicon process and packaging technologies are being developed for automotive semiconductor devices. To achieve the zero-defect quality required for these devices, it is essential to further improve reliability and analysis technologies.

References

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(*1)Process in which hot carriers accelerated by the source-drain electric field are injected into the gate dielectric, degrading the characteristics of a transistor