Understanding MOSFET Current and Thermal limitations

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Power MOSFETs are key elements in almost all power devices. As engineers try to squeeze ever more power and efficiency from each design, then MOSFETs are pushed to their limit. However, there is no single means to define the limitations.

In this whitepaper, Toshiba Electronics Europe looks at the various limitations that can apply to MOSFETs used in power applications and then shares some useful techniques for calculating values and making valid comparisons between suppliers.

Introduction

In general, MOSFETs with lower on-resistance (R_{ON}) can operate with higher currents. Currently, there are devices available with R_{ON} values lower than 1mΩ that can theoretically operate with currents up to 500A in a small 5mm x 6mm package. However, this is not realistic in practice as there are several parametric limitations within any MOSFET.

Toshiba datasheets show the lowest (e.g. worst case) of several limitations, each of which is calculated or measured. Some datasheets show the silicon limitation in addition to the smallest limitation. The lowest value always defines the limit for the device. For low-resistance devices, the current limitation will mainly depend on the package (including its solder area).

Temperature

Basically, any design incorporating MOSFETs is limited by temperature. Temperature depends on two factors; the ability to radiate heat and the on-resistance, which is proportional to heat generated. It does not depend on the drain current.

Some MOSFET suppliers only show the calculation value for the on-resistance limitation. With this approach, there is little meaning to comparing current specifications.

A key formula that engineers need to be aware of is the thermal limitation equation shown in Figure 1.

$$I_D = \sqrt{\frac{T_{chMax} - 25}{rth_{ch-c} \times R_{ONMax(TchMax)}}}$$

...Formula.1

T_{chMax} : Maximum operation temperature

rth_{ch-c} : Channel-case thermal resistance*

$R_{ONMax}(T_{chMax})$: Maximum on-resistance in maximum operation temperature condition

*Some items' rth_{ch-c} value for calculation are used alternative.

Figure 1 – Thermal limitation formula

It should be noted that package construction – and in particular the way that the package deals with heat – is absolutely critical to understanding how a MOSFET is going to perform.

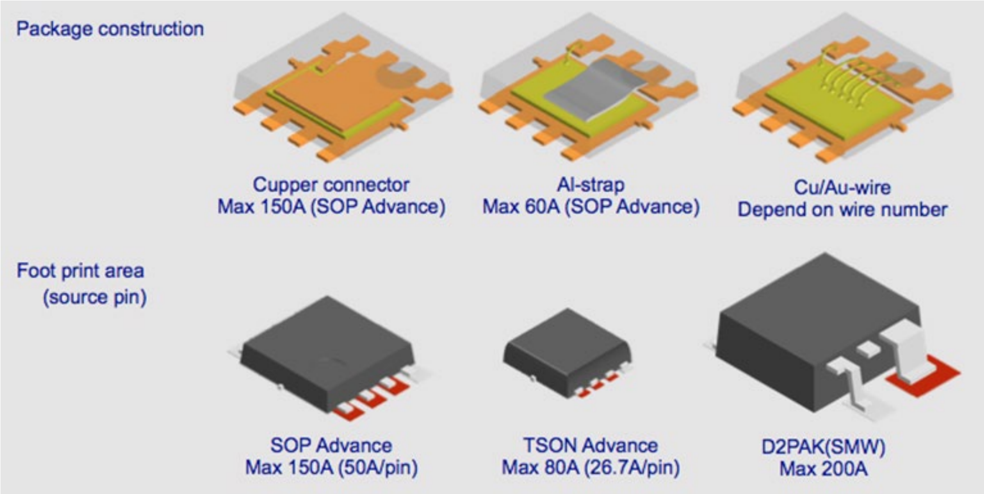

Figure 2 – The package limitation depends on the package footprint and construction

Typically, the maximum permissible current due to package limitation is checked at T_c=25°C as illustrated in Figure 3.

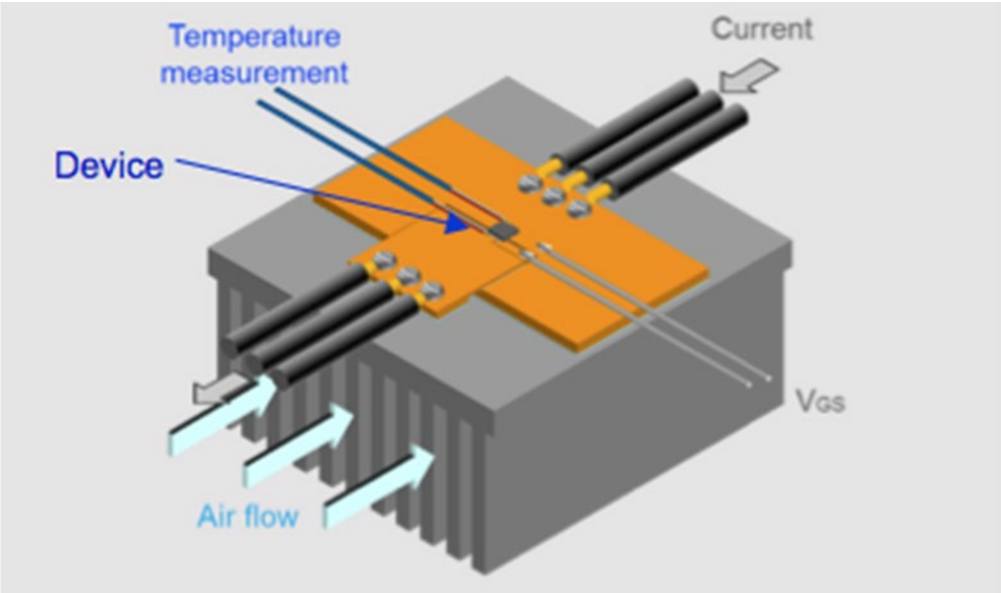

Figure 3 – Package current limitation measurement set-up

Carrier density limitation

Current is saturated by carrier density. Figure 4 shows an ID-VGS curve comparison between an $R_{DS(ON)}$ based calculation and a practically measured curve when V_{GS}=10V. As MOSFETs should only be used in the linear region, I_D is limited by this value.

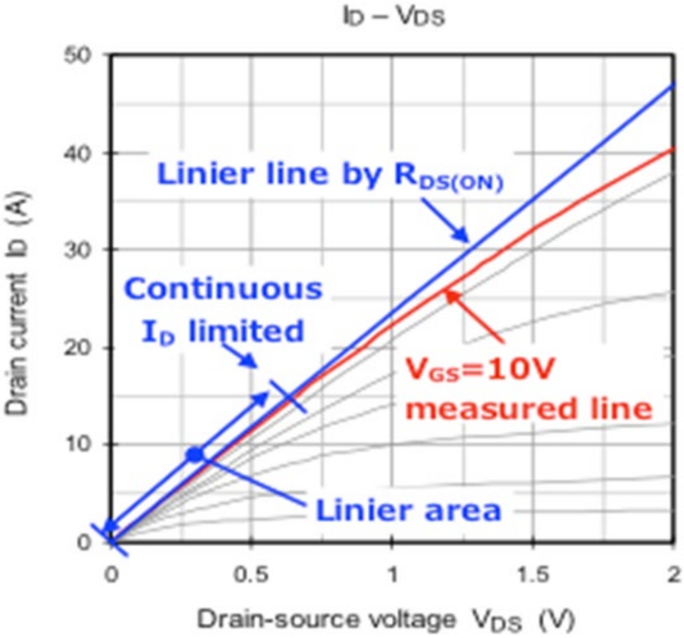

Figure 4 – Carrier density limitation curves - calculated and measured

Avalanche current limitation

MOSFETs occasionally go into avalanche mode during non-standard operating conditions. During this mode, the avalanche current flows through the diode. However, if the avalanche current overflows from the diode, then the equivalent transistor (Bip-Tr) starts to conduct and this damages the device. Therefore, the maximum I_D value of some MOSFETs is constrained by this limitation (it should be noted that this does not apply to all MOSFETs).

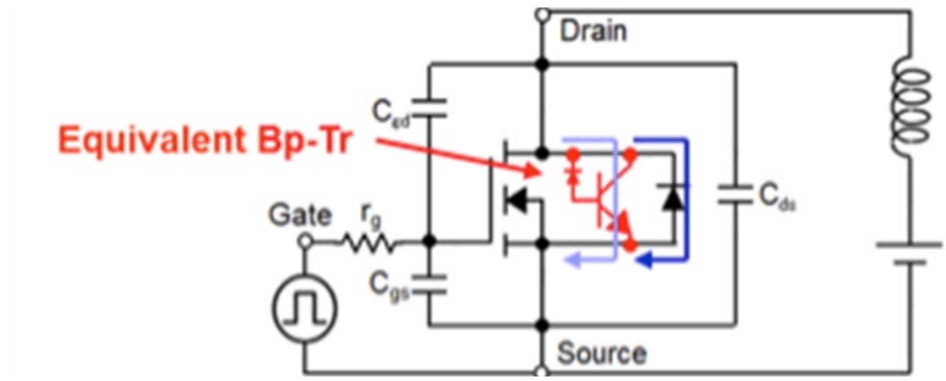

Figure 5 – Equivalent Bip-Tr

When comparing I_D values between suppliers, engineers must check the limitation element to ensure a good comparison. If information relating to the limitation element is not given it should be identified. In the case of Toshiba this information can be found in the longer version of our datasheets.

Example using Toshiba TPHR8504PL

Drain current (DC) (T_c = 25 °C)	(Note 1), (Note 2)	I_D	150	A
Drain current (DC) (Silicon limit)	(Note 1), (Note 2)	I_D	340	A

Note 2: Limited by package limit. Silicon chip capability is 340 A. (T_c = 25 °C)

In this case, 150A is the overall limitation as defined by the lowest value, while 340A is the silicon limitation (including carrier density limitation and avalanche limitation).

Calculation of silicon limitation

Example using TPH1R306PL

Absolute Maximum Ratings (Note) (T_a = 25 °C unless otherwise specified)

Characteristics	Symbol	Rating	Unit
Channel temperature	T_{ch}	175	°C

From the table, $rth_{ch\text{-}c}$ is 0.88°C/W

Using the formula below, $R_{ONMax}(T_{chMax})$ can be calculated:-

$R_{ONMax}(T_{chMax})$ = (R_{ONMax} – PKG resistance*) x a** + PKG resistance = 2.48mΩ

Static Characteristics (T_a = 25 °C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Drain-source on-resistance	$R_{DS(ON)}$	V_{GS} = 4.5 V, I_D = 42 A	—	1.5	2.3	mΩ
		V_{GS} = 10 V, I_D = 50 A	—	1.0	1.34	

* The package value is a non-published value

** 'a' is an approximate value for the thermal coefficient. The value '2' is normally used.

I_D can then be calculated using the formula from Figure 1 above: -

$$I_D = \sqrt{\frac{T_{chMax} - 25}{rth_{ch-c} \times R_{ONMax(TchMax)}}} = \sqrt{\frac{175 - 25}{0.88 \times 2.48}} = 262.1 \neq 260$$

Summary

While the performance of two dissimilar MOSFETs may appear similar based upon datasheet parameters, often this is not the case. Only through understanding the operation of the MOSFET electrically and thermally and applying the appropriate limits can a valid comparison be made.

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