

**TB67S112PG**

**Reference Guide**

**Evaluation Board Manual**

**RD188-RGUIDE1-02-E**

---

Toshiba Electronic Devices & Storage Corporation

## Contents

<b>1. Outline.....</b>	<b>3</b>
<b>2. Evaluation Board Specification .....</b>	<b>3</b>
<b>3. Directions for Use and Notes of Evaluation Board .....</b>	<b>4</b>
3.1. Terminal and Directions for Evaluation Board .....	4
3.2. Power Supply and Notes of Logic Control.....	5
3.3. Notes of Board Design .....	5
<b>4. Circuit Diagram .....</b>	<b>6</b>
<b>5. Reference Documents .....</b>	<b>7</b>

## 1. Outline

This document describes the directions for using the solenoid driver IC TB67S112PG evaluation board, and the notes to be aware of at the time of use. This evaluation board allows the user to connect this IC with the target solenoids for performing evaluation by configuring the power supply and input logic signals.

TB67S112PG is a high-voltage dual-channel solenoid driver IC suitable for driving solenoids and relays. Using the BiCD process, the output voltage of 50V, the output current of 1.5A/ch (absolute maximum rating), and built-in output MOSFET with low ON resistance 0.3Ω (typ.) are realized. Moreover, this IC has various built-in error detection functions like thermal shutdown (TSD), over current detection (ISD), and under voltage lockout (UVLO).

This board is **not for sale**. For evaluating this IC before adoption, kindly contact our distributor or Toshiba's sales representative.

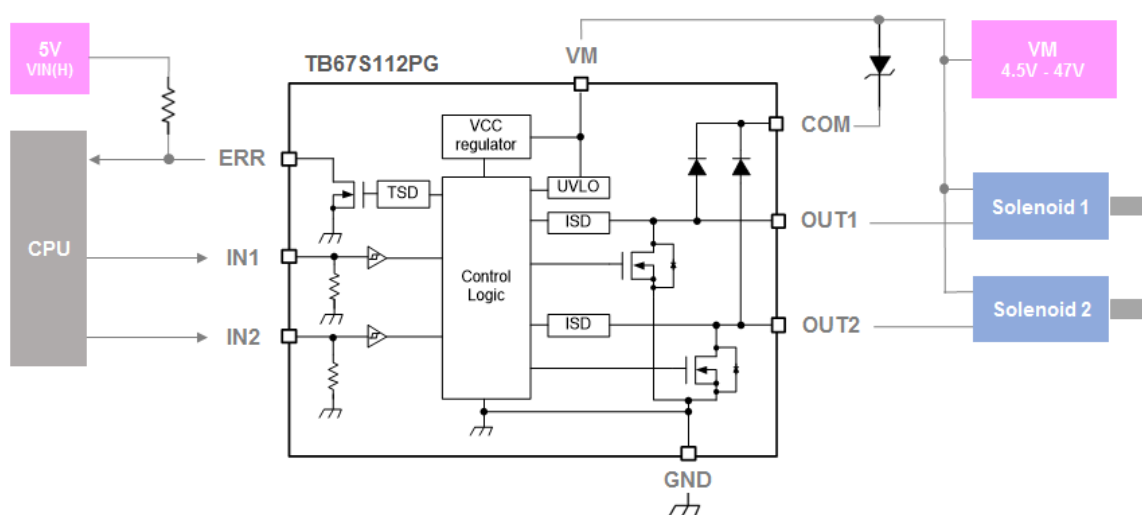
## 2. Evaluation Board Specification

The specification outline of this evaluation board is shown in Table 2.1.

**Table 2.1 Evaluation board specification outline**

Item	Description
IC mounted on board	TB67S112PG (Solenoid driver IC)
VM power supply voltage (VM)	4.5V - 47V (VM power supply voltage of IC)
Output current (IOUT)	1.5A (Ta=25°C, per one channel)
Solenoid control channel	2ch
Evaluation board size	60mm × 60mm
Board thickness, Board material	1.6mm, Glass epoxy board (Both sides)

Internal block diagram of IC TB67S112PG and the example of connection is shown in Figure 2.1.



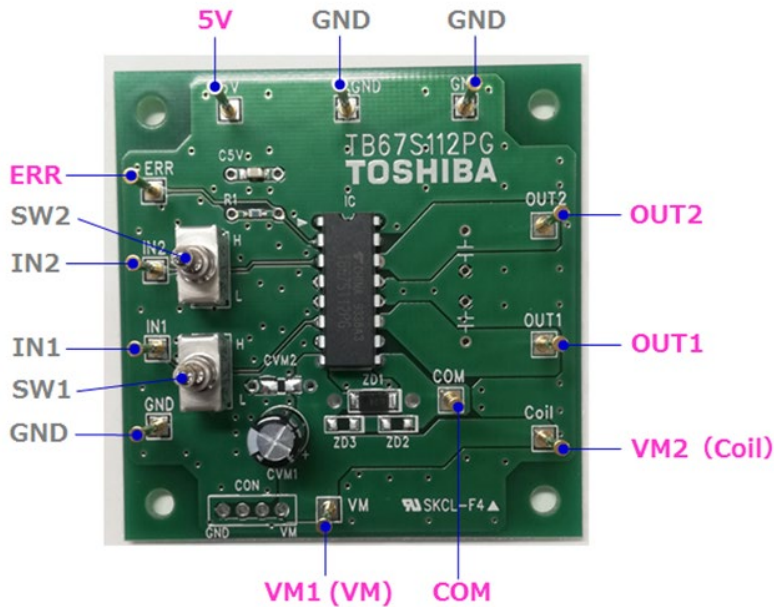
**Figure 2.1 Internal block diagram of IC and the example of connection**

(Note) Some of the functional blocks, circuits, or constants in the block diagram may have been omitted or simplified for explanatory purposes. Refer to the data sheet for the detailed specifications of IC.

### 3. Directions for Use and Notes of Evaluation Board

#### 3.1. Terminal and Directions for Evaluation Board

Each terminal of this evaluation board is shown in Figure 3.1.



**Figure 3.1 Board terminals**

The directions for use and the notes of this evaluation board are shown below.

1. The target solenoid is connected between power supply VM2 (Coil) terminal and OUT1 terminal. While connecting two solenoids simultaneously, the second solenoid connects between power supply VM2 (Coil) terminal and OUT2 terminal.
2. The power is supplied from the outside using VM1 (VM) terminal and GND terminal. By supplying power to VM1 (VM) terminal, the regulator inside IC operates and switch control is enabled. ZD1 (24V zener diode) is mounted between VM1 (VM) terminal and COM terminal. Be careful not to apply a voltage more than absolute maximum rating (50V) to IC with the incoming current at the time of ON, the back electromotive force at the time of OFF, etc.
3. When switching the solenoids ON/OFF using the switch (SW1/SW2) on the evaluation board, or when monitoring an error (ERR), supply voltage (5V) to 5V terminal from the outside. Since the ERR terminal is pulled up to 5V by R1, it becomes "H" at the time of normal operation, and "L" at the time of overheating detection (TSD) functional operation.
4. By applying "H" voltage to IN1 terminal or IN2 terminal, OUT1 terminal or OUT2 terminal can be enabled, respectively. Refer to following table for relation between logic inputs and output MOSFETs. In addition, when controlling IN1/IN2 from outside, please be sure to change SW1/SW2 to the center position (open) state.

Note: This board is **not for sale**. For evaluating this IC before adoption, kindly contact our distributor or Toshiba's sales representative.

Relation between logic inputs and output MOSFETs

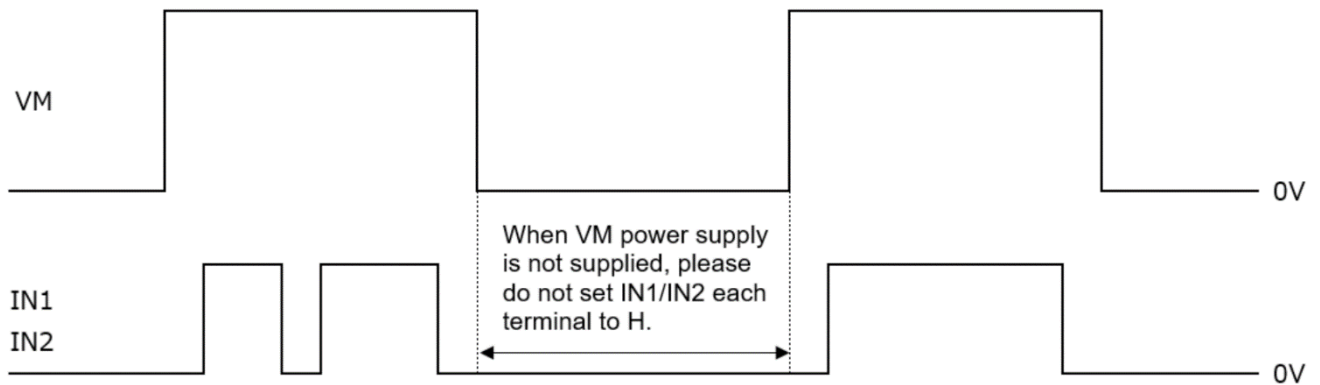
Logic input		Output MOSFET	
IN1	IN2	OUT1	OUT2
L	L	OFF	OFF
H	L	ON	OFF
L	H	OFF	ON
H	H	ON	ON

Output pin for thermal shutdown signal (ERR output function)

ERR	Function
H	Normal operation
L	Thermal shutdown (TSD): active

### 3.2. Power Supply and Notes of Logic Control

The setting conditions of a power supply (VM) and switch logic (IN1/IN2) are shown in Figure 3.2.



**Figure 3.2 Setting conditions of VM and IN1/IN2**

(Note) Timing chart may have been simplified for explanatory purposes.

It is necessary to supply power to VM (VM1) terminal before switching logic via IN1/IN2 terminals. Even if a logic (IN1/IN2) signal is input when power is not supplied to the VM (VM1) terminal, the circuit is designed so that no electromotive force or leakage current is generated due to the signal input.

Before re-supplying voltage to VM (VM1) terminal, please control logic input signals so that the solenoid does not malfunction (Set IN1/IN2 to "H" after VM power is supplied).

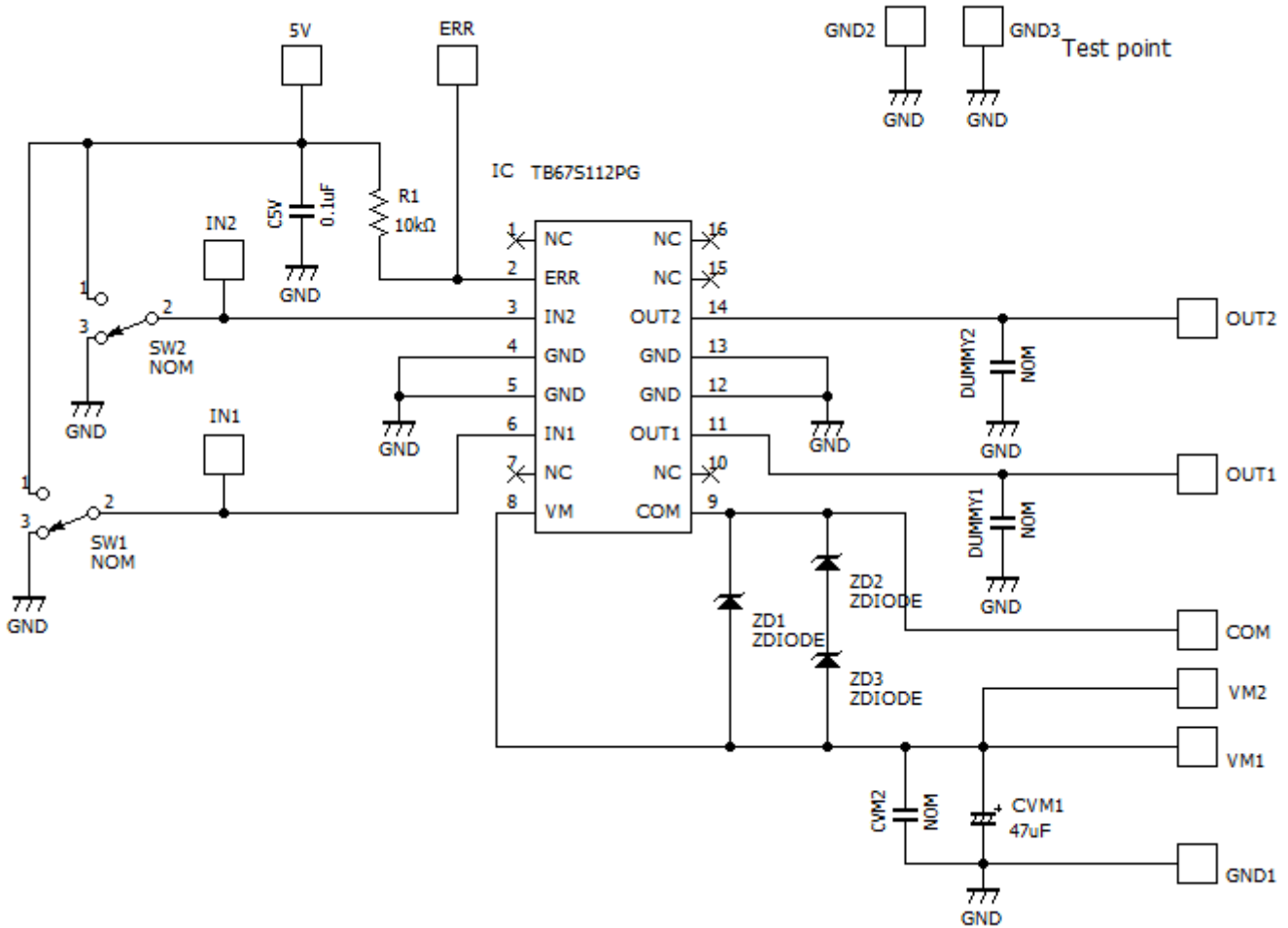
### 3.3. Notes of Board Design

Please consider the following, when designing the board layout pattern with solenoid driver IC TB67S112PG.

- The GND pattern of PCB should be as wide as possible (solid pattern) and be externally terminated at only one point. Also, a grounding method should be considered for efficient heat dissipation.
- Careful attention should be paid to the layout of the output, VM, COM, and GND traces, to avoid short circuits across output pins or to the power supply or ground. If such a short circuit occurs, the device may get permanently damaged.
- The utmost care should be taken for pattern designing and implementation of this device (TB67S112PG) since it has power supply pins (VM, COM, OUT1, OUT2, and GND) through which a particularly large current may run. If these pins are wired incorrectly, an operation error may occur or the device may get destroyed.
- The logic input pins must also be wired correctly. Otherwise, the device may get damaged owing to a current running through the IC that is larger than the specified current. Careful attention should be paid to design patterns and mountings.

### 4. Circuit Diagram

The circuit diagram of this evaluation board is shown below.



**Figure 4.1 Circuit diagram of TB67S112PG evaluation board**

(Note) This circuit diagram is a reference example and does not guarantee operation including protection features or reliability. Thorough evaluation of the board and peripheral parts is required, especially at the mass production design stage.

## 5. Reference Documents

Refer to the data sheet of solenoid driver IC TB67S112PG for the detailed specifications.  
The data sheet of TB67S112PG is downloadable from following web site.

<https://toshiba.semicon-storage.com/ap-en/semiconductor/product/motor-driver-ics/stepping-motor-driver-ics/detail.TB67S112PG.html>

Click Here

Moreover, about the circuit diagram, BOM (bill of materials), and PCB data of the evaluation board, they are downloadable from Reference Design Center of Toshiba web site.

<https://toshiba.semicon-storage.com/ap-en/semiconductor/design-development/referencedesign/articles/solenoid-driver.html>

Click Here

## Terms of Use

This terms of use is made between Toshiba Electronic Devices and Storage Corporation ("We") and customers who use documents and data that are consulted to design electronics applications on which our semiconductor devices are mounted ("this Reference Design"). Customers shall comply with this terms of use. Please note that it is assumed that customers agree to any and all this terms of use if customers download this Reference Design. We may, at its sole and exclusive discretion, change, alter, modify, add, and/or remove any part of this terms of use at any time without any prior notice. We may terminate this terms of use at any time and for any reason. Upon termination of this terms of use, customers shall destroy this Reference Design. In the event of any breach thereof by customers, customers shall destroy this Reference Design, and furnish us a written confirmation to prove such destruction.

### 1. Restrictions on usage

1. This Reference Design is provided solely as reference data for designing electronics applications. Customers shall not use this Reference Design for any other purpose, including without limitation, verification of reliability.
2. This Reference Design is for customer's own use and not for sale, lease or other transfer.
3. Customers shall not use this Reference Design for evaluation in high or low temperature, high humidity, or high electromagnetic environments.
4. This Reference Design shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.

### 2. Limitations

1. We reserve the right to make changes to this Reference Design without notice.
2. This Reference Design should be treated as a reference only. We are not responsible for any incorrect or incomplete data and information.
3. Semiconductor devices can malfunction or fail. When designing electronics applications by referring to this Reference Design, customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of semiconductor devices could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Customers must also refer to and comply with the latest versions of all relevant our information, including without limitation, specifications, data sheets and application notes for semiconductor devices, as well as the precautions and conditions set forth in the "Semiconductor Reliability Handbook".
4. When designing electronics applications by referring to this Reference Design, customers must evaluate the whole system adequately. Customers are solely responsible for all aspects of their own product design or applications. WE ASSUME NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.
5. No responsibility is assumed by us for any infringement of patents or any other intellectual property rights of third parties that may result from the use of this Reference Design. No license to any intellectual property right is granted by this terms of use, whether express or implied, by estoppel or otherwise.
6. THIS REFERENCE DESIGN IS PROVIDED "AS IS". WE (a) ASSUME NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (b) DISCLAIM ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO THIS REFERENCE DESIGN, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.

### 3. Export Control

Customers shall not use or otherwise make available this Reference Design for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). This Reference Design may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of this Reference Design are strictly prohibited except in compliance with all applicable export laws and regulations.

### 4. Governing Laws

This terms of use shall be governed and construed by laws of Japan.