W. Saito, "Breakthrough of drain current capability and on-resistance limits by gate-connected superjunction MOSFET," 2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Chicago, IL, 2018, pp. 36-39. doi: 10.1109/ISPSD.2018.8393596

Breakthrough of Drain Current Capability and On-Resistance Limits by Gate-Connected Superjunction MOSFET

Wataru Saito
Toshiba Electronic Devices & Storage Corporation
Kawasaki, Japan
wataru3.saito@toshiba.co.jp

***Abstract*—This paper reports a new structure of Gate-connected Superjunction (GS) MOSFET to cope with both high drain current density and low on-resistance. The conventional superjunction (SJ) structure is attractive to reduce the specific on-resistance dramatically due to the charge compensation concept. The drain saturation current density, however, is limited by JFET depletion at the bottom region of the SJ structure even if the on-resistance can be reduced by the lateral SJ pitch narrowing. The accumulation-mode operation is effective not only for low on-resistance but also for suppressing the depletion at the SJ bottom due to the accumulation carriers. This paper reports the potential of the GS-MOSFET for high drain current density and low on-resistance based on the simulation results. Dynamic characteristics are also compared with the conventional SJ-MOSFET.**

Keywords—superjunction; on-resistance; saturation current

I. INTRODUCTION

The power-MOSFET is a key component in switching mode power supply circuits and inverter systems. In these applications, low on-resistance of the MOSFETs is desired to reduce power losses in the system. A superjunction (SJ) MOSFET has been commercialized with ultra-low on-resistance below the Si-limit [1]. The SJ structure is consisted with multiple p- and n-columns to allow higher drift region (n-columns) doping concentration than conventional power-MOSFETs. The highly doped n-column directly reduces the on resistance. As a charge compensation concept, the excess charge in the n-column is counterbalanced by the adjacent charges in the p-column, and thus high breakdown voltage is maintained due to high vertical electric field distribution.

To reduce the specific on-resistance ($R_{on}A$) in the SJ MOSFETs, the lateral pitch of the SJ structure must be narrowed in principle due to maintaining high vertical electric field even with the increase of the n-column doping concentration [2]-[4]. According to this design, the $R_{on}A$ reduction with lateral pitch narrowing has been demonstrated, and also, at the 600-650 V-class power MOSFET products, the $R_{on}A$ has been reduced continuously [5]-[8].

The drain saturation current density (J_{dsat}) is also an important characteristic in the SJ MOSFET product design. Low drain current capability is an obstacle to shrink the chip area, even if the on-resistance can be reduced by the lateral SJ pitch narrowing. The products trend shows the J_{dsat} has been increased with inverse proportional to the $R_{on}A$, because the J_{dsat} is limited by JFET depletion at bottom region of the SJ structure [9], [10]. In addition, the high column doping concentration induces the breakdown voltage lowering due to the charge imbalance by the process variation [11], [12]. Therefore, the compatibility of high J_{dsat} and low $R_{on}A$ requires not only the SJ pitch narrowing but also the process margin cut and the thermal budget suppression, and it was estimated that the 600 V-class limits of the $R_{on}A$-J_{dsat} characteristics maintained the product trend were J_{dsat} = 900-1300 A/cm^2 and $R_{on}A$ = 5.5-7.3 mΩcm^2 in the previous work [9].

This paper reports a new structure of Gate-connected Superjunction (GS) MOSFET to cope with both high drain current density and low on-resistance in the SJ MOSFET. The simulation results show the potential of the GS-MOSFET for the breakthrough of high J_{dsat} and low $R_{on}A$ limits in the SJ MOSFET and the dynamic characteristics are also discussed.

II. DESIGN CONCEPT AND DEVICE STRUCTURE

To break through the limits of high J_{dsat} and low $R_{on}A$, the JFET depletion at the SJ bottom region must be suppressed. The accumulation-mode operation is attractive for suppressing the depletion and the on-resistance can be reduced due to the increase of the drift carrier density [13]-[15]. Although the gate electrode induces the accumulation layer at the MOS interface, it is difficult to realize 600 V-class devices, because an ultra-thick oxide film is necessary for sustaining the drain voltage and the thick oxide weakens the accumulation. A thick oxide film is also an obstacle for the lateral pitch narrowing and the process integration [4], [16].

Therefore the GS structure was chosen to realize the

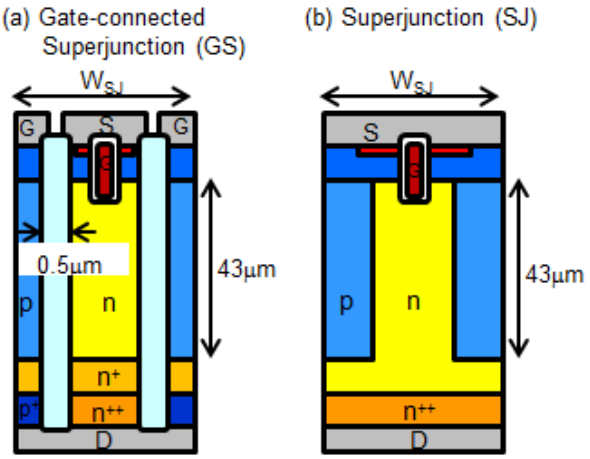

Fig. 1 Cross sectional structure of 600 V-class (a) GS-MOS and (b) SJ-MOS.

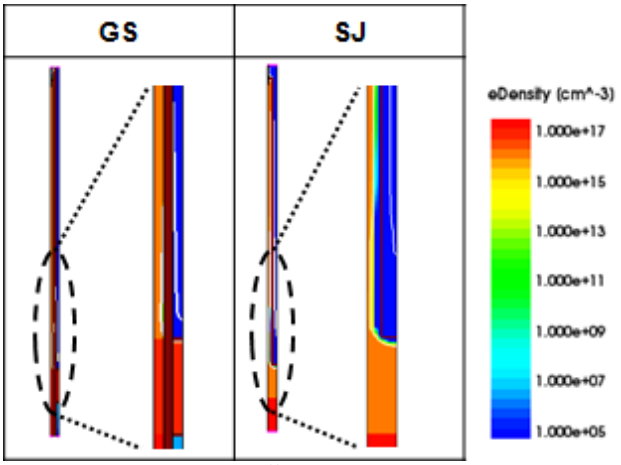

Fig. 2 Suppressing the pinch-off at n-column bottom region at saturation condition (V_{ds} = 20 V) in GS-MOS with W_{SJ} = 3μm.

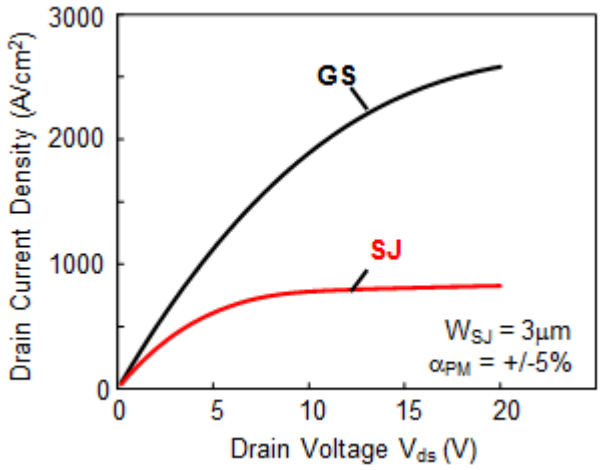

Fig. 3 On-state I_d-V_{ds} characteristics for GS-MOSFET and SJ-MOSFET.

accumulation-mode operation by the SJ structure without the thick oxide film. In the GS-MOSFET, p-columns are connected to the gate and the accumulation layer is generated at the interface between the n-column and the oxide film at the on-state as shown in Fig. 1. Since the p-columns are depleted at the off-state under low applied voltage and sustains the drain voltage, the oxide film thickness between the p- and n-columns can be designed independently from the breakdown voltage. The ON/OFF switching operation is obtained by the MOS gate structure as same as the conventional SJ-MOSFET. In addition, to avoid the G-D short at the on-state, the p-n-p structure, which is the anti-series connection of diodes, is formed between the drain and the p-column [15]. To avoid the turn-on of the parasitic p-ch MOSFET at the on-state, the doping concentration of the n-layer under the p-column must be optimized from the view point of the threshold voltage for the parasitic p-ch MOSFET.

The saturation current density J_{dsat} and the on-resistance $R_{on}A$ for a 600 V-class device were estimated by the device simulation Sentaurus Device of Synopsys. In this work, the oxide film thickness and the SJ thickness were constant of 0.5 μm and 43 μm, respectively as shown in Fig. 1. The J_{dsat} was

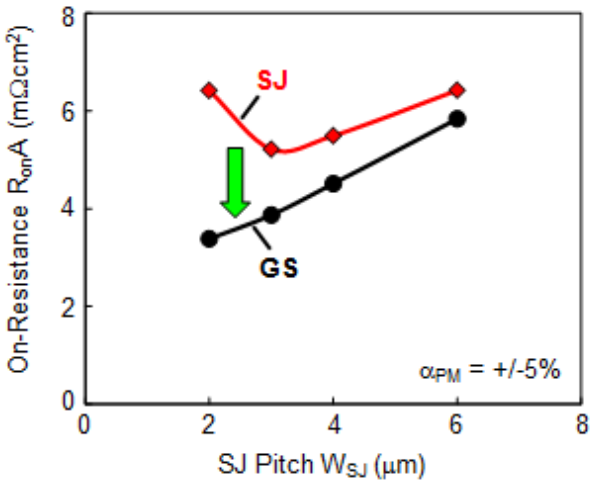

Fig. 4 On-resistance reduction by SJ pitch narrowing in GS-MOSFET.

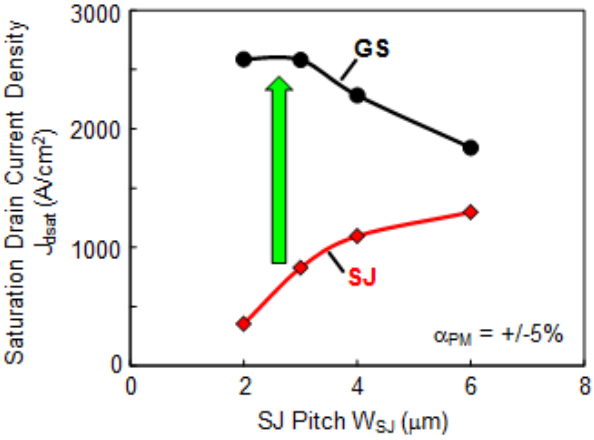

Fig. 5 Maintaining saturation current density increase with SJ pitch narrowing in GS-MOSFET.

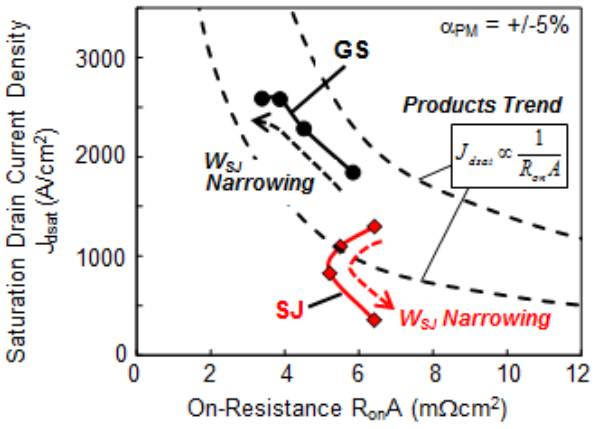

Fig. 6 Fig. 6 Maintaining products trend of drain current density and on-resistance by GS-MOSFET with lateral pitch narrowing.

defined as the drain current density at V_{ds} = 20 V and V_{gs} = 10V and the $R_{on}A$ was calculated from the on-state drain voltage at the drain current density of 100 A/cm^2 [9]. In the actual device, the doping concentration is varied and so the

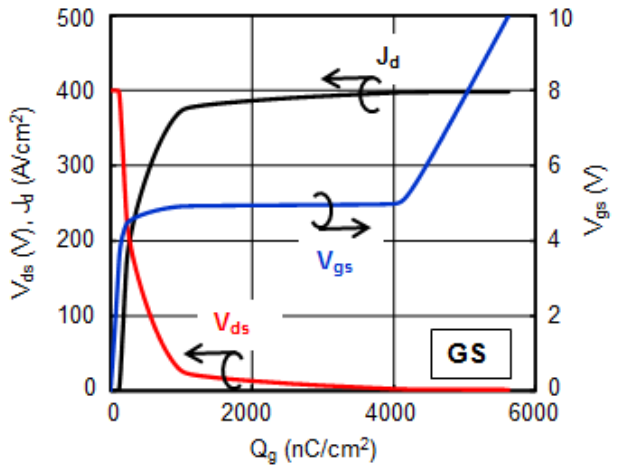

Fig. 7 Gate charge waveform of GS-MOSFET with W_{SJ} = 3μm.

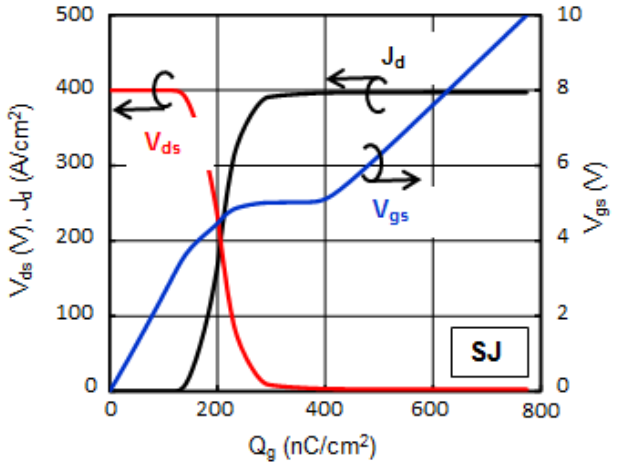

Fig. 8 Gate charge waveform of SJ-MOSFET with W_{SJ} = 3μm.

process margin α_{PM} was considered in this simulation. In this work, the α_{PM} was a constant of +/-5%. The gate charge was also simulated to discuss the switching characteristics.

III. Device Chatacterisitics

The GS-MOSFET achieved not only lower $R_{on}A$ but also higher J_{dsat} compared with the SJ-MOSFET, because the accumulation mode operation by the gate-connected p-column induces high carrier concentration in the drift layer and suppresses the SJ bottom depletion even under high drain voltage as shown in Fig. 2. At the same conditions of the lateral SJ-pitch W_{SJ} and the α_{PM}, the I_d-V_{ds} curve was improved clearly by the GS-MOSFET compared with the SJ-MOSFET as shown in Fig. 3. The W_{SJ} narrowing improves $R_{on}A$ and J_{dsat} characteristics for the GS-MOSFET, although the characteristics for the SJ-MOSFET are degraded by the W_{SJ} narrowing as show in Figs. 4 and 5. The characteristics for SJ-MOSFETs depart from the products trend at the W_{SJ} < 4μm [9]. In contrast, the GS-MOSFET achieves to maintain the products trend even with W_{SJ} = 2μm as shown in Fig. 6.

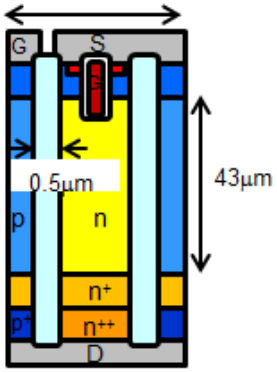

Fig. 9 Cross sectional structure of 600 V-class HGS (Half Gate-connected Superjunction) -MOSFET for gate charge reduction from GS-MOSFET.

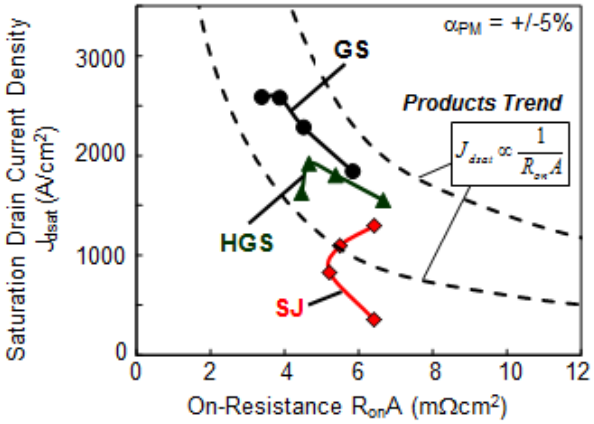

Fig. 10 Trade-off characteristics between saturation drain current density and on-resistance for HGS-MOSFET.

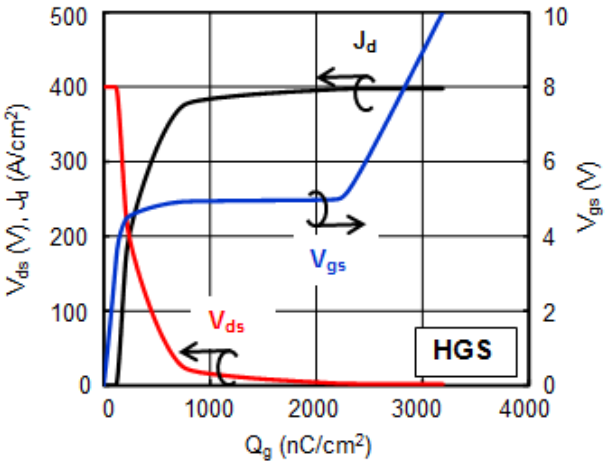

Fig. 11 Gate charge waveform of HGS-MOSFET with W_{SJ} = 3 μm.

The gate-connected p-column induces the accumulation layer and obtains good on-state characteristics as shown above. However, the gate charge is increased dramatically. This is the same manner at the field plate type device as reported in the previous work [14]. The switching gate charge Q_{SW} of the GS-MOSFET was 14 times larger than that of the SJ-MOSFET as shown in Figs. 7 and 8.

Table I Static and dynamic characteristics comparison between GS-MOSFET, HGS-MOSFET and SJ-MOSFET.

Device	GS	HGS	SJ
SJ Pitch	3μm	3μm	4μm
$R_{on}A$	**3.9mΩcm²**	4.7mΩcm²	**5.5mΩcm²**
J_{dsat}	**2600A/cm²**	1900A/cm²	**1100A/cm²**
$R_{on}Q_{sw}$	**15.5ΩnC**	9.8ΩnC	**1.4ΩnC**
$R_{on}Q_g$	**21.7ΩnC**	14.9ΩnC	**3.3ΩnC**

IV. Arrangement of Characteristics

The proposed GS-MOSFET has a potential for the breakthrough of the SJ-MOSFET limit. The switching characteristics, however, are degraded by the large gate capacitance. As a middle state structure, Half Gate-connected SJ (HGS)-MOSFET is also proposed to arrange the characteristics as shown in Fig. 9. In the HGS-MOSFET, one p-column is connected to the gate and another one is connected to the source. The HGS-MOSFET improves the $R_{on}A$ and J_{dsat} characteristics compared with the SJ-MOSFET and the characteristics correspond to the middle between those of the GS-MOSFET and the SJ-MOSFET as shown in Fig. 10. The Q_{SW} for the HGS-MOSFET becomes a half of that for the GS-MOSFET as shown Fig. 11. From these results, the static and switching characteristics can be adjusted by the number of p-columns connected to the gate.

The characteristics for the proposed devices in this work are summarized in Table I. It was estimated that the GS-MOSFET breaks through the SJ-MOSFET limits and obtains J_{dsat} = 2600 A/cm^2 and $R_{on}A$ = 3.9 mΩcm^2 for 600 V-class. Although 11 times larger $R_{on}Q_{sw}$ compared with the SJ-MOSFET is disadvantage for the power supply application, high J_{dsat} and low $R_{on}A$ are attractive for inverter applications, such as motor drive systems, power conditioning systems and so on. The HGS-MOSFET has a potential for the replacement of the old generation SJ-MOSFET, because $R_{on}Q_{SW}$ and $R_{on}Q_g$ values are almost the same. From these results, the GS-MOSFET and the HGS-MOSFET have a potential for breakthrough the SJ-MOSFET limits.

V. Conclusions

A new structure of Gate-connected Superjunction (GS) MOSFET was proposed to cope with both high drain current density and low on-resistance. The gate-connected p-column induces accumulation layer at the interface between the n-column and the oxide film. The accumulation-mode operation is effective not only for low on-resistance but also for suppressing the depletion at the SJ bottom due to the accumulation carriers. The GS-MOSFET breaks through the SJ-MOSFET limits and obtains J_{dsat} = 2600 A/cm^2 and $R_{on}A$ = 3.9 mΩcm^2 for 600 V-class. Since the gate-connected p-column increases the gate charge, the $R_{on}Q_{sw}$ is 11 times larger compared with the SJ-MOSFET. As a middle state structure, Half Gate-connected SJ (HGS)-MOSFET, in which a half of the p-columns are connected to the gate, was also proposed. The HGS-MOSFET also improves the $R_{on}A$ and J_{dsat} characteristics compared with the SJ-MOSFET and the characteristics can be adjusted by the number of p-columns connected to the gate. From these results, the GS-MOSFET and the HGS-MOSFET have a potential for breakthrough the SJ-MOSFET limits.

References

[1] G. Deboy, M. März, J. –P. Stengl, H. Strack, J. Tihanyi and H. Weber "A new generation of high voltage MOSFETs breaks the limit of silicon", in Technical Digests of IEDM'98, pp.683-685, 1998.

[2] T. Fujihira, "Theory of semiconductor superjunction devices," Jpn. J. of Appl. Phys., vol. 36, pp.6254-6262, 1997.

[3] A. G. M. Strollo and E. Napoli, "Optimul on-resistance versus breakdown voltage tradeoff in superjunction power devices: a novel analytical model," IEEE Trans. on Electron Devices, vol. 48, pp. 2161-2167, 2001.

[4] W. Saito, "Comparison of theoretical limits between superjunction and field plate structures," in Proceedings of ISPSD'13, pp. 241-244, 2013.

[5] W. Saito, I. Omura, S. Aida, S. Koduki, M. Izumisawa, H. Yoshioka, H. Okumura, M. Yamaguchi and T. Ogura, "A 15.5mΩcm^2-680V Superjunction MOSFET reduced on-resistance by lateral pitch narrowing," in Proceedings of ISPSD'06, pp.293-296, 2006.

[6] J. Sakakibara, Y. Noda, T. Shibata, S. Nogami, T. Yamaoka and H. Yamaguchi, "600V-class super junction MOSFET with high aspect ratio p/n columns structure," in Proceedings of ISPSD'08, pp.299-302, 2008.

[7] W. Saito, "Power Device Trends for High- Power Density Operation of Power Electronics System," Jpn. J. of Appl. Phys., vol. 53, 04EP02, 2014.

[8] F. Udrea, G. Deboy and T. Fujihira, "Superjunction power devices, history, development, and futre prospets," IEEE Trans. on Electron Devices, vol. 64, pp. 713-727, 2017.

[9] W. Saito, "Process design of superjunction MOSFETs for high drain current capability and low on-resistance," in Proceedings of ISPSD'17, pp. 475-478, 2017.

[10] D. Disney and G. Dolny, "JFET depletion in superjunction devices," in Proceedings of ISPSD'08, pp. 157-160, 2008.

[11] P. M. Shenoy, A. Bhalla and G. M. Dolny, "Analysis of the effect of charge imbalance on the static and dynamic characteristics of the super junction MOSFET," in Proceedings of ISPSD'99, pp. 99-102, 1999.

[12] W. Saito, "Theoretical limits of superjunction considering with charge imbalance margin," in Proceedings of ISPSD'15, pp. 125-128, 2015.

[13] B. Jayant Baliga, Tsengyou Syau, and Prasad Venkatraman, "The accumulation-mode field-effect transistor: a new ultralow on-resistance MOSFET," IEEE Electron Device Letters, vol. 13, pp. 427-429, 1992.

[14] M. A. Gajda, S. W. Hodgskiss, L. A. Mounfield, N. T. Irwin, G. E. J. Koops and R. van Dalen, "Industriation of resurf stepped oxide technology for power transistors," in Proceedings of ISPSD'06, pp. 109-112, 2006.

[15] J. Wei, X. Luo, Y. Zhang, P. Li, K. Zhou, Z. Li D. Lei, F. He and B. Zhang, "Accumulation-mode high voltage SOI LDMOS with ultralow specific on-resistance," in Proceedings of ISPSD'15, pp. 185-188, 2015.

[16] R. Siemieniec, C. Braz and O. Blank, "Design considerations for charge-compensated power MOSFET in the medium-voltage range, in Proceedings of ISPS'16, pp. 107-114, 2016.