1.2 kV-Class SiC MOSFET Equipped with Embedded SBD for Improvement of Reliability

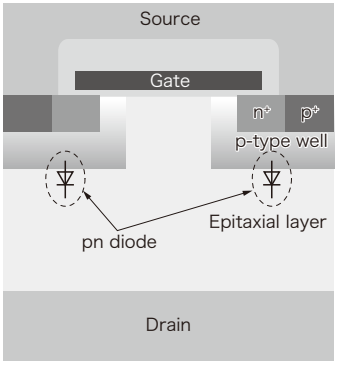
Silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) are a key type of power device for power supply units because of the superior performance of SiC materials. However, improvement of the reliability of SiC MOSFETs is hindered by issues associated with low carrier conductivity as a result of increased crystal defects caused by the energization of pn diodes formed between the source and drain when a current is passed through them.

In order to rectify this situation, Toshiba Electronic Devices & Storage Corporation has developed a new device structure for 1.2 kV-class SiC MOSFETs that can improve reliability by means of an embedded Schottky barrier diode (SBD) located in parallel to each pn diode so as to prevent current flowing through the diode. The results of tests that we conducted show that this device structure using embedded SBDs can suppress the generation of crystal defects, thereby improving the reliability of SiC MOSFETs, and thus we have confirmed the device structure's effectiveness.

1. Introduction

Power devices are indispensable in reducing the power consumption of automotive, industrial, and other electric applications. SiC is attracting much attention as a next-generation material that will enable the realization of power devices with higher breakdown voltage and lower power loss than conventional silicon (Si) power devices. In the future, SiC power devices are expected to be used for a wide range of applications requiring high breakdown voltage, including railway inverters, solar photovoltaic power generators, and various power supply units.

However, in order to achieve more widespread use of SiC power devices, it is necessary to improve their reliability. Power MOSFETs have pn diodes between the drain and the source as shown in **Figure 1**. These pn diodes act as freewheeling diodes (FWDs) in motor and some other applications. When the pn diodes are forward-biased, the SiC MOSFET enters bipolar mode. In this mode, the energy generated by the recombination of electrons and holes causes the basal plane dislocation (BPD)[1] in a wafer to expand, creating crystal defects called Shockley-type stacking faults (SSFs). SSFs hinder carrier conduction, increasing the turn-on voltage of the pn diodes and the resistance of the MOSFET. Toshiba Electronic Devices & Storage Corporation created a prototype of an SiC pn diode. **Figure 2** shows the images obtained before and after applying a forward current stress to a sample SiC pn diode using an electroluminescence measurement tool. In the dark triangular regions, carrier conduction is hindered because of BPD. When a voltage higher than the turn-on voltage of the pn diode is applied across its pn junction, current flows through the pn diode, generating energy that causes the BPD in the epitaxial layer of an SiC MOSFET to expand.



n⁺: heavily doped n-type semiconductor
p⁺: heavily doped p-type semiconductor

Figure 1. Cross-sectional structure of power MOSFET and pn diodes

A power MOSFET has pn diodes between the drain and the source.

We overcame this problem by embedding SBDs in MOSFET cells. We have already commercialized the SSM5H and SSM5G series of Si MOSFETs with SBDs embedded in MOSFET cells[2]. SiC MOSFETs with SBDs for applications requiring a breakdown voltage of 3.3 kV or higher have also been reported by other semiconductor manufacturers[3][4]. However, in the case of SiC MOSFETs with a breakdown voltage of 1.2 kV or less, the channel resistance accounts for a large proportion of the total

resistance of the MOSFET. Therefore, embedding SBDs in an SiC MOSFET would cause an increase in its on-resistance (R_{on}). In order to overcome the degradation in the reliability of the SBD-embedded SiC MOSFET caused by current conduction, we have optimized its structure while reducing an increase in R_{on}. This report discusses the structure, the principle of operation, and key parameters of the newly developed 1.2 kV SBD-embedded SiC MOSFET. It also describes the results of an electrical evaluation of this SBD-embedded MOSFET with a new structure.

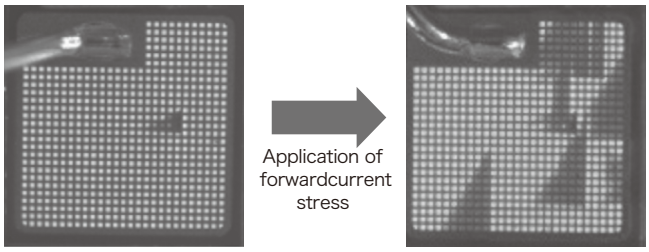


Figure 2. Electroluminescent images of pn diodes in SiC before and after current conduction

The right-hand electroluminescent image has dark triangular areas where carrier conduction is hindered as a result of expansion of basal plane dislocation (BPD).

2. Device structure and principle of operation

2.1. Design objective

A basic design policy was to reduce the electric current flowing through the pn diode. For this purpose, we added an SBD in parallel with the pn diode. Since the turn-on voltage of this SBD (roughly 0.7 V) is sufficiently lower than that of the pn diode (roughly 2.5 V), it helps reduce the current flowing to the pn diode. **Figure 3** shows the cross-sectional view of the SBD-embedded MOSFET and its equivalent circuit.

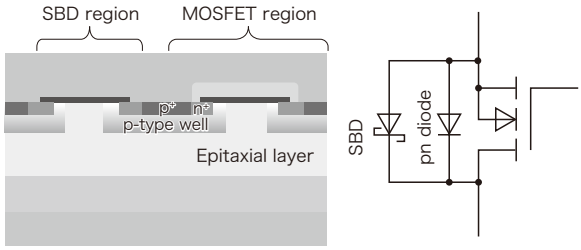


Figure 3. Crosssectional structure of SBDembedded MOSFET and its equivalent circuit

The current flowing through the pn diode can be reduced by adding an SBD with a turn-on voltage sufficiently lower than that of the pn diode in parallel.

2.2.Principle of operation and key parameters of the SBD-embedded MOSFET

When the source has a positive voltage with respect to the drain, current begins to flow through the SBD before the pn diode because the SBD has a lower turn-on voltage than the pn diode. **Figure 4** shows the current paths through the SBD region. The main resistance components along these current paths include the resistance of the junction-barrier-controlled Schottky (JBS) diode (R_{jbs}), current spreading resistance (R_{spread}), and drift layer resistance (R_{drift}). When current I flows through the pn junction, the voltage applied across it (V_{pn}) is expressed as follows:

$$V_{pn}=V_k + (R_{jbs}+R_{spread}) \cdot I \quad (1)$$

where V_k is the voltage applied across the Schottky barrier.

Let the turn-on voltage of the pn diode be V_{on}. Then, when the following equation is satisfied, the pn diode remains inactive and

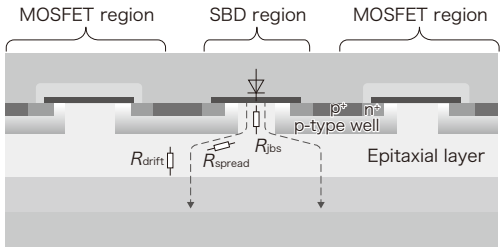


Figure 4. Current paths and main resistance components when current passed through SBD

In order to increase I_{umax}, it is necessary to reduce the resistance components in the current paths through the SBD region.

therefore does not cause any degradation in electrical characteristics:

$$V_{pn}<V_{on} \quad (2)$$

From Equations (1) and (2), current does not flow through the pn

diode when the following equation is satisfied:

$$I < \frac{V_{on} - V_k}{R_{jbs} + R_{spread}} \quad (3)$$

The maximum I value is equal to the maximum current in unipolar mode. Letting this value be I_{umax}, it is expressed as follows:

$$I_{umax} = \frac{V_{on} - V_k}{R_{jbs} + R_{spread}} \quad (4)$$

As this equation indicates, it is necessary to minimize V_k, R_{jbs}, and R_{spread} to increase the maximum current in unipolar operation mode (I_{umax}) of the SBD-embedded MOSFET. However, these parameters have a trade-off with other characteristics of the SBD-embedded MOSFET as described below. R_{jbs} is determined by the distance between the p-type regions on both sides of the SBD-embedded MOSFET and the dopant concentration of the n-type layer between them. R_{spread} depends on the dopant concentration of the n-type layer under the p-type regions. If the dopant concentration of the n-type region is increased to reduce R_{jbs} and R_{spread}, the electric field in the electrodes and the pn junction of the SBD tends to increase when the SBD-embedded MOSFET is off. This might cause the drain-source leakage current to increase. I_{umax} is also affected by the SBD-to-MOS cell ratio. In order to increase I_{umax}, it is necessary to increase the SBD-to-MOS cell ratio so that current can reach the area below the p-type region farthest from the SBD. However, increasing the SBD-to-MOS cell ratio causes the R_{on} of the SiC MOSFET to increase. In order to overcome these trade-offs, it is necessary to optimize the device structure.

3. Prototyping results

3.1. Measuring the maximum current density in unipolar mode

The density of the source-to-drain current (J_{sd}) depends on the source-to-drain voltage (V_{sd}). **Figure 5** shows the J_{sd}–to-V_{sd} curves at a junction temperature (T_j) of 175°C for conventional and SBD-embedded MOSFETs. The maximum current density in unipolar mode (J_{umax}) can be derived by taking into consideration the difference in the slope of the J_{sd}–V_{sd} curve between the unipolar and bipolar regions as shown in Figure 5. Specifically, J_{umax} is calculated as the current density at which the first-order (second-order) derivative of the source-to-drain current (I_{sd}) with respect to the source-to-drain voltage (V_{sd}) becomes constant. In **Figure 6**, the horizontal axis represents current, and the left-hand and right-hand scales of the vertical axis represent the first-order and second-order derivatives of I_{sd} with respect to V_{sd}, respectively. We obtain J_{umax} as the current density when the second-order derivative of I_{sd} with respect to V_{sd} is equal to 2.5. The effectiveness of this method has been verified through long-term conduction reliability evaluations. As a result of repeated evaluations, we have confirmed that reliability faults occur when the J_{umax} value derived by this method is exceeded.

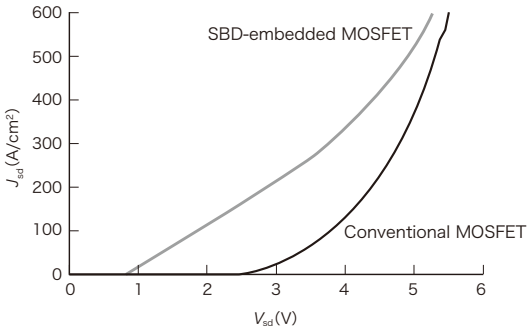


Figure 5. Current-voltage (*I*-*V*) characteristics of conventional and SBD-embedded MOSFETs at junction temperature (T_j) of 175°C

The slopes of the J_{sd}–V_{sd} curve of the newly developed SBDembedded MOSFET differ between the unipolar and bipolar regions because the turn-on-state voltage of its SBD is lower than that of the pn diode in the conventional MOSFET.

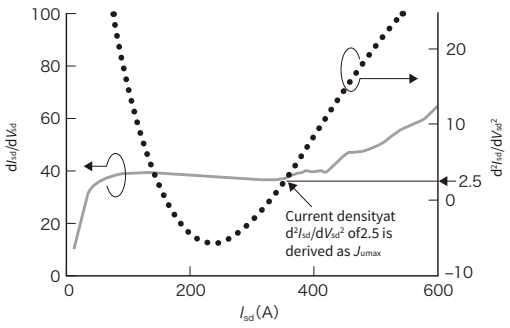


Figure 6. First-order and second-order derivatives of diode characteristics

J_{umax} is defined as the current density when the second-order derivative of I_{sd} with respect to V_{sd} becomes constant.

3.2. Characteristics of the SBD-embedded MOSFET

As Equation (4) shown in Section 2 indicates, J_{umax} is determined by V_{on}, V_k, R_{jbs}, R_{spread}, and the SBD-to-MOS cell ratio. **Figure 7** plots the J_{umax} values calculated from the I_{sd}–V_{sd} characteristics at several junction temperature (T_j) points in the range of 80 to 175°C using the method described in Section 3.1. We applied direct current (DC) to the reverse-biased diode for up to 1,000 consecutive hours at multiple arbitrary T_j points at which the current density is smaller than J_{umax}. As a result, we confirmed that R_{on} remains constant throughout the test. **Figure 8** shows the dependence of J_{umax} at a T_j of 175°C and the dependence of R_{on} at a T_j of 25°C on the SBD-to-MOS cell ratio. Here, N is an integer that represents the number of MOS cells per unit SBD cell. The larger the N, the smaller the SBD-to-MOS cell ratio. There is a trade-off between the SBD-to-MOS cell ratio and the R_{on} of the MOSFET. Since increasing the SBD-to-MOS cell ratio causes an increase in R_{on}, the optimum SBD-to-MOS cell ratio value is chosen, taking the MOSFET's rated current into consideration.

Figure 9 shows the temperature dependence of the R_{on} of the conventional and SBD-embedded MOSFETs. The channel density of the SBD-embedded MOSFET is lower than that of the conventional MOSFET. Therefore, the SBD-embedded MOSFET has higher R_{on} and a higher ratio of the channel resistance to the total MOSFET resistance. The channel resistance decreases as temperature increases. Since the channel resistance accounts for a large proportion of the total resistance of the SBD-embedded MOSFET, its channel resistance component decreases in the high-temperature region. The SBD-embedded MOSFET exhibits less increase in total resistance over temperature than the conventional MOSFET. Therefore, in the high-temperature region, the R_{on} of the SBD-embedded MOSFET gradually approaches that of the conventional MOSFET. The on-resistance per unit area ($R_{on}A$) of the SBD-embedded MOSFET is less than 1.2 times that of the conventional MOSFET over the temperature range in which actual applications are typically used (T_j = 80 to 175°C).

Figure 10 shows the trade-off between the $R_{on}A$ and the threshold voltage (V_{th}) of the newly developed SBD-embedded MOSFET at a T_j of 80°C in comparison with conventional 1.2 kV discrete SiC MOSFETs. The lower the $R_{on}A$ and the higher the V_{th}, the better. We performed a 1,000-hour DC conduction test at a current density of 250 A/cm^2 and a T_j

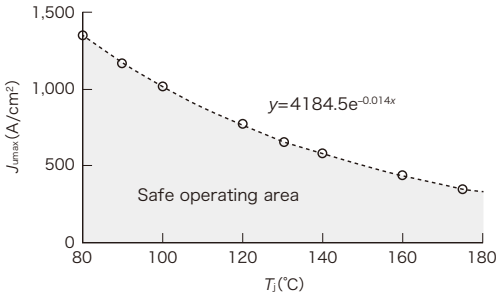


Figure 7. Temperature dependence of maximum current in unipolar operation

J_{umax} was calculated from the I_{sd}–V_{sd} characteristics at several junction temperature (T_j) points in the range of 80 to 175°C in order to grasp the safe operating area.

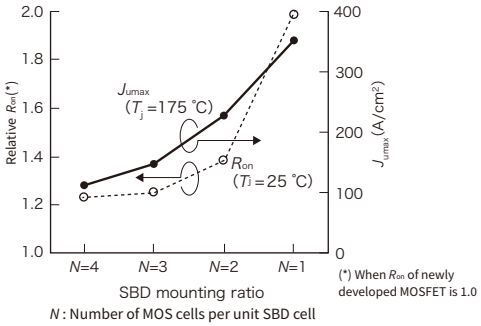


Figure 8. Dependence of maximum current in unipolar operation and on-resistance on SBD-to-MOS cell ratio

There is a trade-off between N and R_{on}. As N is increased, J_{umax} increases, yet at the expense of increased R_{on}.

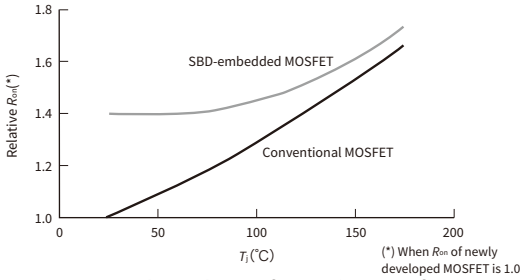


Figure 9. Temperature dependence of on-resistance of conventional and SBD-embedded MOSFETs

In the high-temperature region, the R_{on} of the SBD-embedded MOSFET gradually approaches that of the conventional MOSFET. Therefore, the $R_{on}A$ of the SBD-embedded MOSFET is less than 1.2 times that of the conventional MOSFET in the temperature range in which actual applications are typically used (T_j = 80 to 175°C).

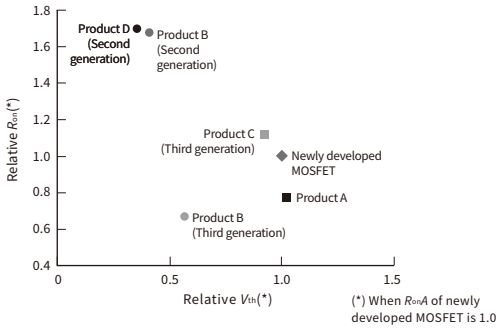


Figure 10. Trade-off between on-resistance per univt area and threshold voltage of 1.2 kV SiC MOSFETs

We benchmarked the trade-off between the R_{on} and the V_{th} of the newly developed SBD-embedded MOSFET at a T_j of 80°C in comparison with commercially available 1.2 kV discrete SiC MOSFETs.

of 175°C. **Figure 11** shows the resulting changes in the R_{on} of the conventional and SBD-embedded MOSFETs during the test. The R_{on} of the conventional MOSFET changed shortly after current is applied to it whereas the R_{on} of the SBD-embedded MOSFET remained unchanged for 1,000 hours. As demonstrated by the results of this test, we succeeded in developing a 1.2 kV-class SiC MOSFET, overcoming the problem of reliability degradation caused by the conduction of pn diodes.

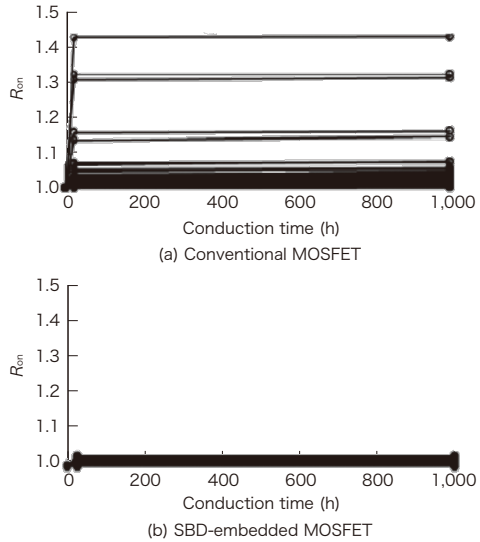


Figure 11. Changes in on-resistance when DC current is applied to conventional and SBD-embedded MOSFETs for 1,000 hours

We applied DC current to the reverse-biased diode for up to 1,000 consecutive hours at multiple arbitrarily selected temperature points at which the current density is smaller than J_{umax}. As a result,we confirmed that R_{on} remains constant throughout the test.

We also verified the reliability of the gate oxide of the SBD-embedded SiC MOSFET. SiC has higher defect density and generally a shorter time-dependent dielectric breakdown (TDDB) life than Si. Therefore, in addition to the embedding of SBDs, we optimized the gate oxide formation process to realize high-quality SiC MOSFETs. We obtained voltage and temperature acceleration factors by experiment and then evaluated the life of the gate oxide film under typical MOSFET drive conditions (gate-source voltage V_{gs} = 20 V and T_j = 120°C). This evaluation confirmed that the gate oxide film of the SBD-embedded SiC MOSFET has an extremely long life with a failure rate of 1 part per million (ppm) per roughly 10 million years (**Figure 12**).

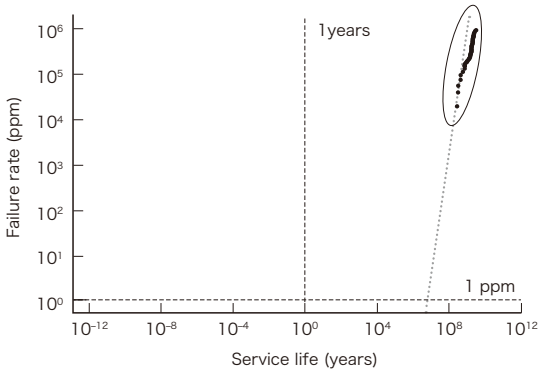


Figure 12. Result of time-dependent dielectric breakdown (TDDB) evaluation of SBD-embedded MOSFET

We realized high-quality SiC MOSFETs by means of the optimized gate oxide formation process. Our evaluation confirmed that the gate oxide film of the SBD-embedded SiC MOSFET has an extremely long life with a failure rate of 1 ppm per roughly 10 million years.

4. Conclusion

We added an SBD in parallel with the pn diode of the MOSFET in order to reduce the amount of current flowing through the pn diode, overcoming degradation in device reliability. Because of the optimized embedding of SBDs, the newly developed 1.2 kV-class SiC MOSFET is also competitive in terms of $R_{on}A$.

References

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