Improving the specific on-resistance and short-circuit ruggedness tradeoff of 1.2-kV-class SBD-embedded SiC MOSFETs through cell pitch reduction and internal resistance optimization

Hiroshi Kono, Shunsuke Asaba, Teruyuki Ohashi+, Takahiro Ogata, Masaru Furukawa, Kenya Sano, Masakazu Yamaguchi, Hisashi Suzuki

Toshiba Electronic Devices & Storage Corporation

300, Ikaruga, Taishi-Cho, Ibo-Gun, Hyogo, Japan,

E-Mail: hiroshi.kono@toshiba.co.jp

+Corporate Research & Development Center, Toshiba Corporation, Kawasaki, Japan

Abstract— **The impact of cell size and JFET width reduction on static and dynamic device characteristics is investigated in 1.2-kV-class Schottky barrier diode (SBD)-embedded SiC metal–oxide–semiconductor field effect transistors (MOSFETs). We compare a conventional SBD-embedded MOSFET with improved SBD-embedded MOSFETs with smaller cell pitch and JFET width than the conventional SBD-embedded SiC MOSFET. The optimized SBD-embedded SiC MOSFETs achieve 39% lower on-resistance and 16% lower switching energy loss compared with the conventional design. We also investigate the tradeoff between $R_{on}A$ and short-circuit withstand time (t_{SC}). Although $R_{on}A$ reduction generally causes a decrease in short circuit withstand capability and reverse conduction capability, we demonstrate that the optimized SBD-embedded SiC MOSFETs have a lower forward voltage drop and short circuit withstand capability. These results show that it is possible to simultaneously reduce $R_{on}A$ and improve t_{SC} with adequate optimization.**

Keywords—SiC MOSFET, SBD-embedded MOSFET, Short-circuit withstand time.

I. INTRODUCTION

Silicon carbide (SiC) metal-oxide-semiconductor field effect transistors (MOSFETs) are next-generation power switching devices for high power and high blocking voltage applications. However, degradation of the on-resistance of SiC MOSFETs caused by bipolar operation has been an issue for SiC MOSFETs [1,2]. Although several studies have reported that the degradation rate is reduced by using screening [3] and buffer layers [4], a more fundamental solution for this issue is needed for high-power modules in order to achieve high reliability. Schottky barrier diode (SBD)-embedded MOSFETs can suppress the bipolar operation of the body diode of MOSFETs [5,6]. In 1.2-kV-class MOSFETs, the ratio of the channel resistance accounts for a large percentage of the device specific on resistance ($R_{on}A$). Hence the impact of increasing the resistance due to the SBD-embedding is larger than that of high-blocking voltage devices such as 3.3 kV or higher. Therefore, it is important to reduce the $R_{on}A$ of SBD-embedded MOSFETs, particularly in the 1.2 kV class. In a previous study, we reported on a structure that minimizes the increase in $R_{on}A$ and suppresses the body diode operation by optimizing the ratio of SBD cells to MOSFET cells.

In high-voltage high-power modules, there is demand for even lower power dissipation without reducing tolerance and reliability. However, reducing $R_{on}A$ generally requires decreasing in the short-circuit withstand capability and reducing the SBD ratio, which causes a decrease in the maximum reverse conductivity that can prevent bipolar operation of the body diode. Therefore, the objective of this study is to develop a 1.2-kV-class SBD-integrated SiC MOSFET with lower conduction and switching losses without degrading the bipolar current suppression capability and short-circuit tolerance. In particular, we focus on the impact of cell pitch reduction and current spreading layer (CSL) structure optimization on device $R_{on}A$, switching loss, reverse current capacity, and short-circuit tolerance.

II. SBD-EMBEDDED SIC MOSFET DEVICE

We investigate a planar type double-implanted SiC MOSFET of which a schematic cross-sectional view of the unit cell is shown in Fig. 1.
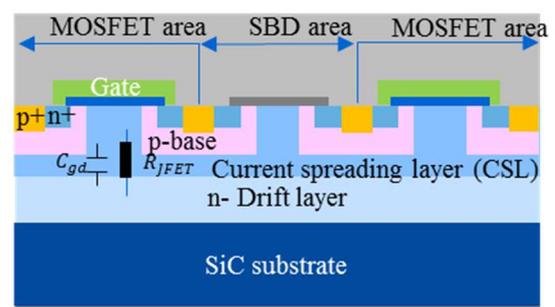
Fig.1: Schematic cross-sectional diagram of the fabricated SBD-embedded SiC MOSFET.

In this paper, we study the impact of reducing $R_{on}A$ by reducing the cell pitch and JFET width. The reduction in JFET width not only reduces the gate-drain capacitance (C_{gd}) but also improves the switching speed. In general, although the reduction in $R_{on}A$ leads to a decrease in short-circuit tolerance owing to the increase in saturation current, the reduced JFET width can also suppress the saturation current. Because the reduction in JFET width causes an increase in

JFET resistance (R_{JFET}), internal resistance optimization is needed. We investigate two types of devices (devices A and B) that have different cell pitches and optimize the SBD/MOS ratio as described in [6]. We suppress the increase in R_{JFET} by optimizing the current spreading layer in device B, as described in [7], using Synopsys technology computer aid design (TCAD). The cell pitch of device B is reduced by 18% compared with that of device A by shrinking the JFET width and reducing the dimensions of other components.

Figure 2 shows the resistance components of $R_{on}A$ of each device when the gate voltage (V_g) is 20 V as calculated by TCAD. Each of the values of $R_{on}A$ are normalized with respect to the $R_{on}A$ of device A. These results show that the $R_{on}A$ of device B was reduced by 29% compared to device A by reducing both channel and JFET resistance.
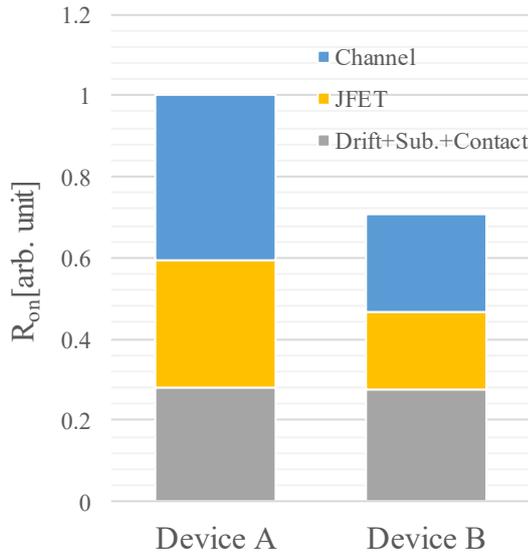
Fig.2 Specific on resistance components of each device as calculated by TCAD simulation @ 300 A/cm². (simulated values)

III. EXPERIMENTAL RESUSLTS

We fabricated devices A and B on n-type 4H-SiC wafers. The measured static I_d-V_d characteristics of the fabricated SiC MOSFETs when V_g = 20 V at room temperature (RT) and 150°C are shown in Fig. 3. The temperature dependence of $R_{on}A$ evaluated at a drain current density of 300 A/cm² is shown in Fig. 4. Fig. 5 shows the off-state characteristics of devices A and B. The blocking voltages (V_{bd}) of devices A and B were 1580 and 1620 V, respectively, at RT. The $R_{on}A$ of device B was reduced by 39% compared with device A at RT while maintaining the same breakdown voltages. Although the temperature dependence of device B was increased compared with device A, $R_{on}A$ of device B at 150°C was lower than that of device A at RT. The threshold voltages of devices A and B were sufficiently high at 4.1 and 3.8 V, respectively, even at 150°C. The tradeoff between $R_{on}A$ and V_{bd} follows the same tradeoff line that was previously reported for SBD-integrated trench MOSFETs [7].
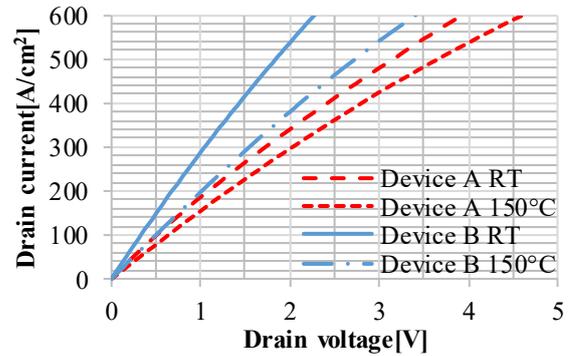
Fig. 3 I_d-V_d characteristics of fabricated SiC MOSFETs (experimental values) showing on-state characteristics at room temperature and 150°C when V_g = 20 V.
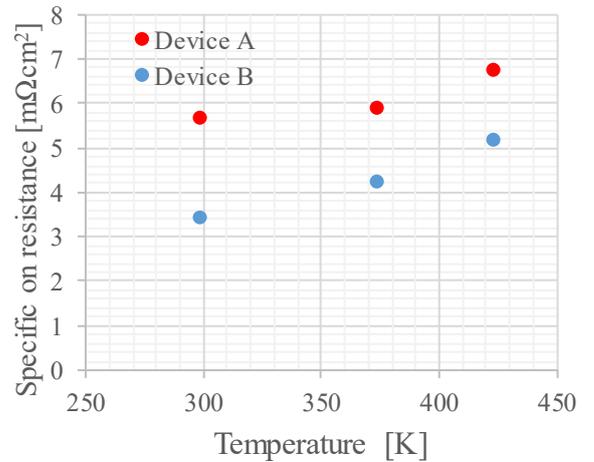
Fig. 4. Temperature dependence of the specific on resistance of the fabricated SiC MOSFETs (experimental values).
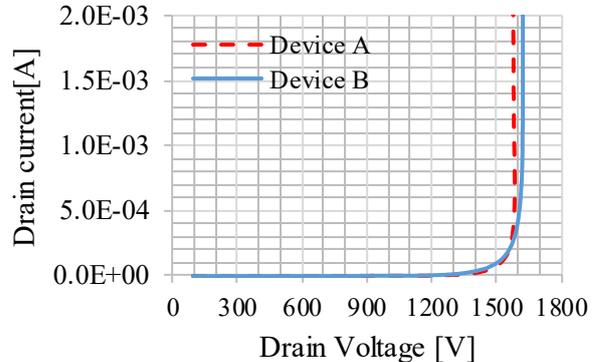
Fig. 5 I_d-V_d characteristics of fabricated SiC MOSFETs (experimental values) showing off-state characteristics at room temperature when V_g=0 V.
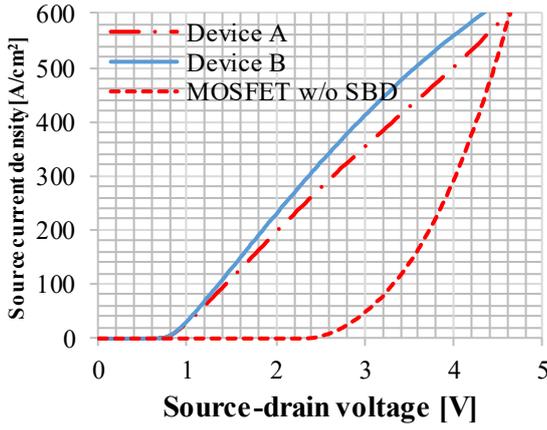
Fig. 6 I_{sd}-V_{sd} characteristics of the fabricated MOSFET without SBD when $V_g = -5$ V at 150 °C.

Fig. 6 shows the reverse conducting characteristics of devices A and B when $V_g = -5$ V at 150°C. A MOSFET without SBD is also shown for reference. Although the MOSFET without SBD started bipolar operation at about 2.3 V, neither of devices A or B started bipolar operation until the current was 600 A/cm^2 at 150°C. Comparing the voltage (V_f) of each device at 300 A/cm^2, the V_f of the MOSFET without SBD was 4.0 V, while that of device A was 2.6 V and that of device B was 2.4 V. Therefore, the reverse conduction loss of device B was lower than that of device A.

The capacitance–voltage (C-V) characteristics are shown in Fig. 7. These values are normalized with respect to the output capacitance (C_{oss}) of device A at $V_d = 0.1$ V. The reverse transfer capacitance (C_{rss}) was reduced by about 50% at low drain voltage, due to the reduction in JFET width and cell optimization.
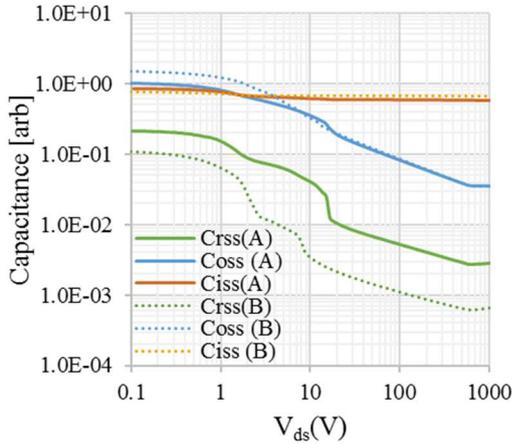
Fig. 7 C-V characteristics of fabricated SiC MOSFETs.

Fig. 8 shows the double-pulse test waveforms obtained in an inductive load circuit. In the measurements, the supply voltage was 600 V, the gate drive voltage was −5/20 V and the load inductance was 300 μH. Fig. 9 shows the measured switching energy losses for devices A and B. The turn-off loss was calculated by integrating the energy loss between the time when the drain voltage exceeds 60 V and the time when the current drops below 10 A. The turn-on loss was calculated

by integrating the energy loss between the time when the drain current exceeded 10 A and the time when the voltage fell below 60 V.
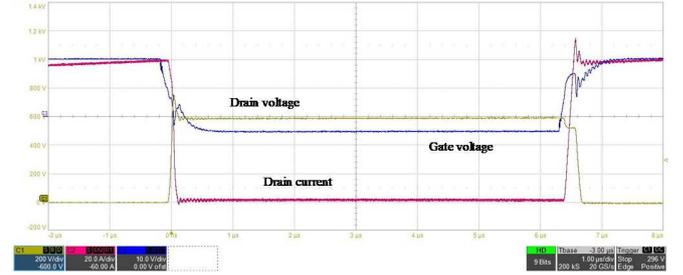
Fig. 8 Turn-off and turn-on waveforms of the fabricated SiC MOSFETs. The supply voltage was 600 V and the load current was 100 A.
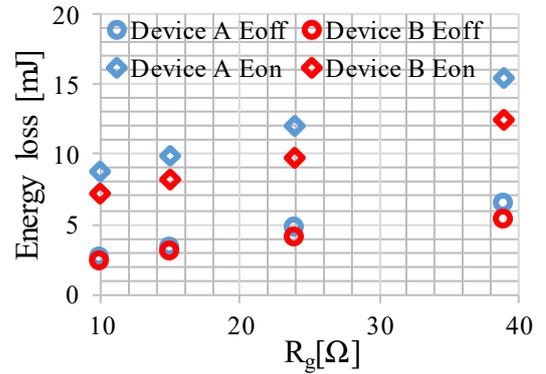
Fig. 9 Comparison of switching energies for different gate resistances between different device structures. The supply voltage was 600 V and the load current was 100 A.
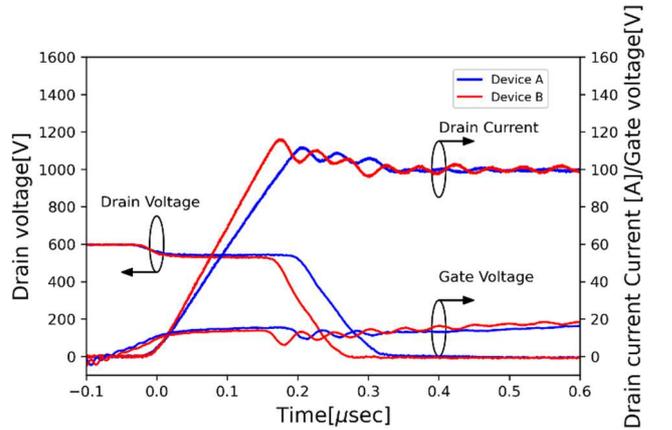
Fig.10 Turn-on waveforms of the fabricated SiC MOSFETs, when $V_d = 600$ V, $I_d = 100$ A and $R_g = 15$ Ω.

The total switching loss of device B was reduced by about 16% compared with that of device A. Fig. 10 shows magnified turn-on waveforms. From these results, it can be seen that the time at which the current rise ended and the voltage fall time differed between devices A and B. The current rise time t_1 is calculated as follows:

$$t_1 = R_g(C_{iss} + C_{rss})ln\left[\frac{V_g}{(V_g - V_{th}) - I_d/g_m}\right],$$

where R_g is gate resistance, C_{iss} is input capacitance, C_{rss} is reverse transfer capacitance, V_g is gate voltage, V_{th} is threshold voltage, and g_m is transconductance. The drain fall time t_2 is calculated as follows:

$$t_2 = \frac{R_g C_{rss}(V_{ds}-V_{on})}{V_g-(V_{th}+I_d/g_m)},$$

where V_{on} is the drain voltage at 100 A. It is thought that the increase in g_m and decrease in C_{rss} affect the switching time reduction.

The short-circuit withstand time t_{SC} of these devices at RT was investigated by setting the stress duration from 0.7 to 1.3 in steps of 0.016. The time axis was normalized to the short-circuit withstand time of device A. The waveforms of the last test before destruction are shown in Fig. 10. The t_{SC} of device B was improved by 25% compared with that of device A (Fig. 11). A reduction in $R_{on}A$ generally causes an increase in the saturation current and decrease in the short-circuit withstand time. However, device B did not decrease the short-circuit withstand time but actually improved it. It can be seen that this improvement was due to the reduction of JFET width. These results show that it is possible to simultaneously reduce $R_{on}A$ and improve t_{SC} by adequate optimization.
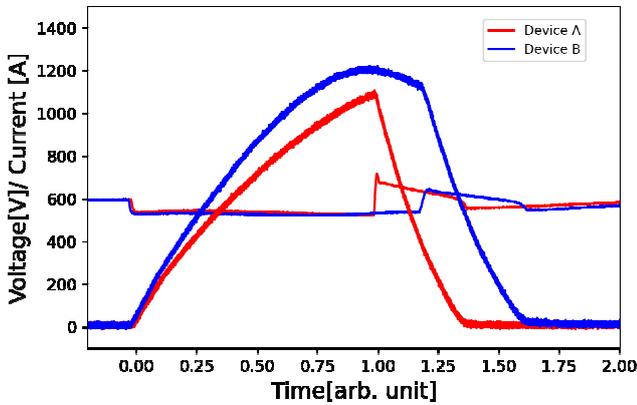
Fig.11 Measured short-circuit current waveforms of devices A and B. The supply voltage was 600 V at room temperature. The time axis is normalized with respect to the short-circuit withstand time of device A.
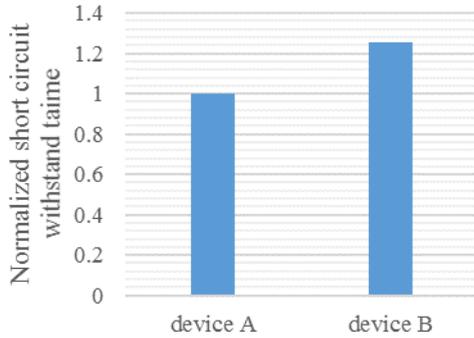
Fig. 12 Comparison of short-circuit withstand time.

IV. CONCLUSION

The aim of this study was to develop a 1.2-kV-class SBD-integrated SiC MOSFET with lower conduction and switching losses without degrading the bipolar current suppression capability and short-circuit tolerance. We focused on improving the specific on-resistance and short-circuit ruggedness tradeoff of 1.2-kV-class SBD-embedded SiC MOSFETs through cell pitch reduction and internal resistance optimization. The $R_{on}A$ of optimized SBD-embedded SiC MOSFET was reduced by 39% compared with that of a conventional SBD-embedded SiC MOSFET at RT while maintaining the same breakdown voltages. These results imply that the tradeoff between $R_{on}A$ and V_{bd} follows the same tradeoff line that was previously reported for SBD-integrated trench MOSFETs [8].

The present study also showed that the optimized SBD-embedded SiC MOSFET did not start bipolar operation until a current of 600 A/cm^2, even at 150°C. The t_{SC} of device B was improved by 25% compared with that of device A. These results show that it is possible to simultaneously reduce $R_{on}A$ and improve t_{SC} with adequate optimization. Consequently, the newly developed device is expected to achieve low loss and high reliability in applications that require high reliability.

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