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Impact of reverse current spreading on diode conduction reliability of SBD-embedded SiC MOSFET with deep p-shield structure

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***Abstract*—The device structure of SBD-embedded MOSFET was investigated and the complicated trade-off relationship of on-state resistance, short-circuit ruggedness, and diode conduction capability was improved. TCAD analysis indicated that bipolar conduction in body diode of MOSFET with deep p-shield can be suppressed by developing current spreading layer structure. The fabricated devices demonstrated adequate ruggedness in short-circuit operation and unipolar conduction capability in diode operation while obtaining low on-state resistance. The reduction in leakage by the developed structure enabled drift layer tuning and finally low on-resistance of 2.0 mΩ·cm² was demonstrated.**

***Keywords*— SiC, MOSFET, Embedded SBD, Short circuit**

I. Introduction

Bipolar conduction in diode operation of SiC MOSFET causes a reliability problem due to expanding crystal defects of SiC substrates. Embedding Schottky barrier diode (SBD) into the cell structure of SiC MOSFET is a credible design to avoid such bipolar degradation and has been commercially available [1-8]. Fig.1.(a) illustrates the device structure and equivalent circuit diagram of the cell design with striped pattern embedded-SBD. When reverse current smaller than the critical current density called J_{umax} (maximum current density of unipolar conduction) flows, current is dominated by unipolar conduction through embedded SBD. We reported a drastic decrease in specific on-resistance ($R_{on}A$) while improving J_{umax} by employing the cell structure with two-dimensional SBD layout shown in Fig. 2(b) [3]. A design strategy for realizing both low $R_{on}A$ and high J_{umax} was shown; however, securing short-circuit (SC) ruggedness is another important demand considering application of low $R_{on}A$ SiC MOSFET. In particular, the destruction mechanism attributed to embedded SBD [4] has to be considered carefully. There is a complicated trilemma in determining device design to satisfy the requirements of low $R_{on}A$, high J_{umax}, and good SC ruggedness. Improvement in SC ruggedness by introducing deep p-well structure that suppresses SC current and Schottky leakage has recently been reported (Fig. 1(c)) [5-6]. Considering commercial application, demonstrating the advantage of introducing deep p-well structure while realizing high J_{umax} and low $R_{on}A$ is essential. In this paper, we propose the developed cell structure with extended CSL (Current Spreading Layer) as shown in Fig. 1(d). The mechanism to improve J_{umax} and SC ruggedness while obtaining low $R_{on}A$ was investigated and performance improvement was evaluated.

II. Devepopment of the Cell Structure

A. Importance of narrow W_{JBS} for SC-ruggedness

Firstly, TCAD simulation was conducted in order to clarify the SC failure mechanism and determine appropriate geometry of embedded SBD. The simplified two-dimensional structures containing the MOSFET region and embedded SBD with different W_{JBS} (width of Junction Barrier for Schottky junction) as shown in Fig. 2 were computed. Long gate turn-on of 5.0 microseconds was applied and the simulations were continued regardless of the device temperature so that behavior of SBD leakage could be clarified. Figure 3 shows the simulated waveforms of current and temperature when wide or narrow W_{JBS} was used. Immediately after gate is turned on, drain current through channel rapidly increases. Generated Joule heat elevates the temperature of the JFET region and that causes SC current saturation in approximately 2 microseconds. After gate turn-off, drain current rapidly decreases. Despite the negligible difference in current attributed to channel, a different behavior was observed in the SBD current. Initially after gate turn-on, SBD current did not appear for both W_{JBS} geometry. This is

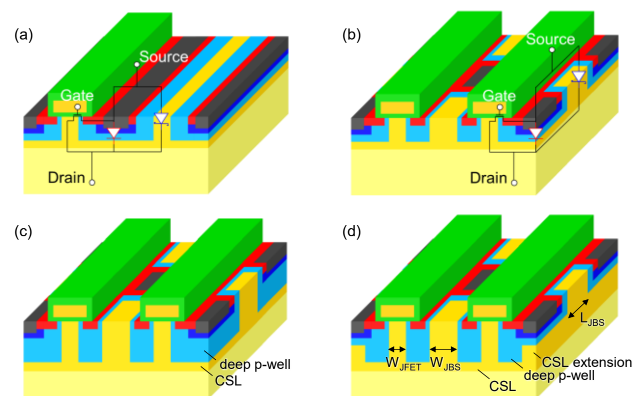

Fig. 1 Device structure of the SBD-embedded SiC MOSFETs.
(a) Conventional stripe-SBD (b) 2D-SBD
(c) 2D-SBD + deep p-well
(d) 2D-SBD + deep p-well with CSL extension (This work)

because p-Base structure is designed to control the reverse bias of Schottky junction in the blocking mode. Although reverse leakage is well suppressed by the junction barrier effect, leakage may increase when temperature is elevated extremely. As for the model with wide W_{JBS}, leakage continues to increase even after gate was turned off, which leads to thermal runaway. Choosing metals with high Schottky barrier height and narrower W_{JBS} are the solution to reduce leakage of SBD in SC operation. However, both of them simultaneously degrade J_{umax} because of higher voltage drop and loss of effective area. We determined the maximum W_{JBS} essential for securing SC ruggedness through the TCAD investigation and used it in designing the cell structure, which is described below.

B. J_{umax} improvement by the extended CSL

J_{umax} improvement by modifying the device structure without changing metal or W_{JBS} is discussed. We have reported that the clamping effect of embedded SBDs against the bipolar conduction is strongly influenced by the spreading of SBD current[7-8]. Now we examine the contribution of CSL structure in deep p-well structure in order to improve fundamental J_{umax} by comparing the developed structure with CSL extension to the conventional structure without CSL extension. Extended CSL is placed under the ohmic contact region alternating with some portion of deep p-well. Injected SBD current can easily conduct below the p-n junction underneath the ohmic contacts. What is important is that introducing the CSL extension does not influence the shield effect on the Schottky interface. This is because the SBD junction is always placed between the deep p-well stripes in the common spacing of W_{JBS}. Therefore, low leakage of SBD in the reverse bias can be maintained while enhancing spreading of SBD current in the forward bias. To evaluate the enhancement effect in SBD current spreading, device structure models combine cross-sectional planes perpendicular and parallel to the MOS gate stripes of the cell structure (Fig. 4). Considering this model is equivalent to examining the longest route of SBD current. Figure 5 shows the simulated diode

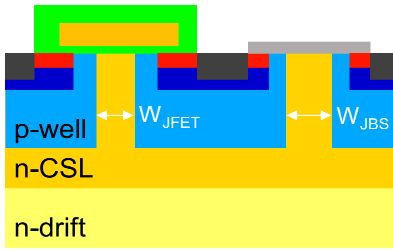

Fig. 2 Schematical diagram of the simulated device structure.

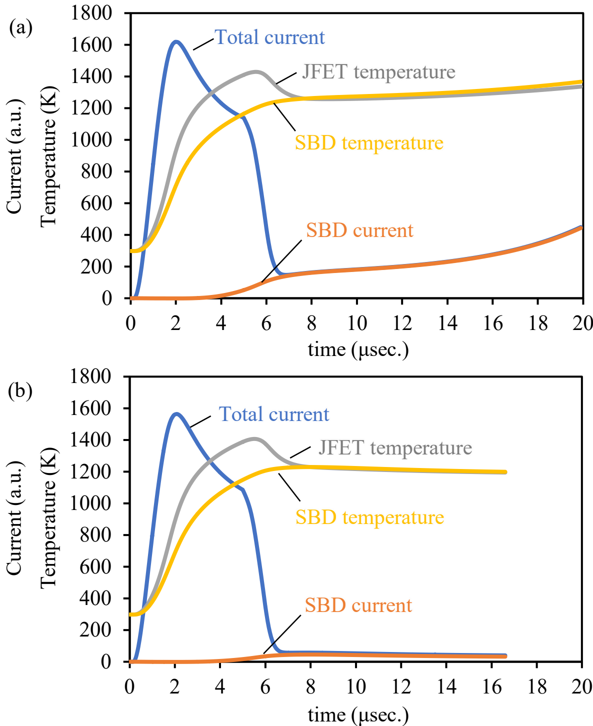

Fig. 3 Simulated short-circuit characteristics of different W_{JBS}.
(a) Wide W_{JBS} (b) Appropriately narrow W_{JBS}.
Vds=600V. Gate turn-on at 0- 5.0 microseconds.

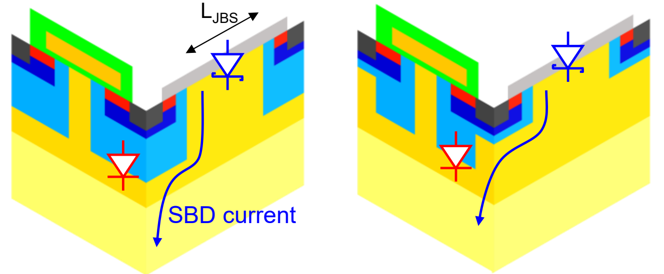

Fig. 4 Simplified device structure used in the TCAD simulation.
(a) conventional structure without CSL extension.
(b) proposed structure with CSL extension.
Arrow lines schematically illustrate SBD current flow.

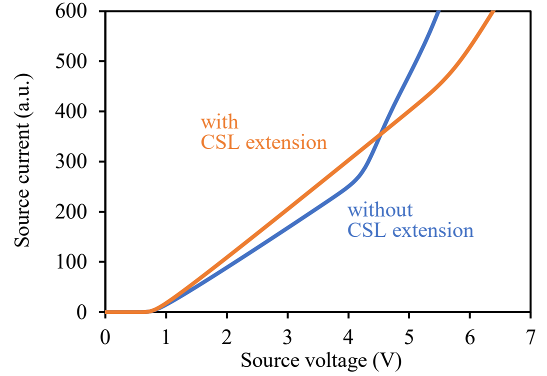

Fig. 5 Simulated diode characteristics. 175°C

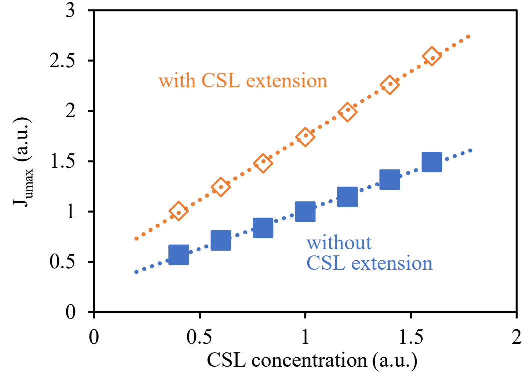

Fig. 6 Simulated J_{umax} dependency on the CSL doping concentration.

characteristics at the high temperature of 175°C. When source voltage larger than Schottky barrier height is applied, unipolar current through SBD linearly increases. When even larger voltage is applied, bipolar current through parasitic p-n junction is observed. J_{umax} which is the boundary point between unipolar and bipolar conduction is determined by the curvature transition. Obvious increase in J_{umax} by introducing CSL extension was confirmed. Spreading SBD current below parasitic p-n junction modulates potential distribution, which prevents bipolar conduction. Figure 6 shows the J_{umax} dependency on doping concentration of CSL. J_{umax} is almost doubled by introducing CSL extension over all simulated CSL doping concentrations. Since higher doping concentration of CSL increases total leakage of the device and not only of the embedded SBD region, CSL extension is fascinating when considering overall design of SBD-embedded MOSFET chip. It is shown that CSL extension enhances the current spreading effect, leading to fundamental improvement in J_{umax} without modulating W_{JBS}. Doping concentrations of CSL were also determined through the TCAD analysis.

III. Demonstration of Superior Performance Trade-Off

We fabricated 1.2-kV-class SiC MOSFETs utilizing the developed structure with deep p-well employing CSL extension. Devices with different W_{JFET} (JFET width) were prepared and tested in order to confirm the trade-off relationship between $R_{on}A$ and SC ruggedness. SC stress is repeatedly applied while increasing duration until device is destroyed, and the final duration was determined to be SCWT (Short-circuit withstand time). Figure 7 shows the SC waveforms when destruction happened. Immediately after gate turned on, drain current increased and saturated in 2-3 microseconds. After drain current once decreased to zero by gate turn-off, the devices were destroyed in about ten microseconds after turn-off (not shown in the figure). Narrower W_{JFET} diminished the peak current and resulted in longer SCWT. This dependency is evidence supporting the existence of a mechanism whereby JFET resistance suppresses short-circuit current and narrower W_{JFET} emphasized this self-stop effect. Figure 8 shows the trade-off relationship between $R_{on}A$ and SCWT. Compared to conventional design with shallow p-well structure, the developed structure with deep p-well exhibited better SC ruggedness with smaller $R_{on}A$ compromise. It is demonstrated that deep p-well structure evidently improves SC ruggedness.

We also fabricated MOSFETs with different SBD area ratios and common W_{JBS} in order to evaluate the clamping effect of integrated SBDs. Figure 9 shows the diode characteristics measured at the high temperature of 175°C. Unipolar current by embedded SBD linearly increased and conductivity modulation due to bipolar conduction through parasitic p-n diode was observed as well as the simulation result shown in Figure 3. As the contribution of enlarged Schottky junction area, the amount of unipolar current was reasonably increased. Although CSL structure and W_{JBS} were not changed, increase in source voltage of J_{umax} was measured. It is suggested that plenty of SBD current also contributed to modification of the potential near the p-n junctions, which

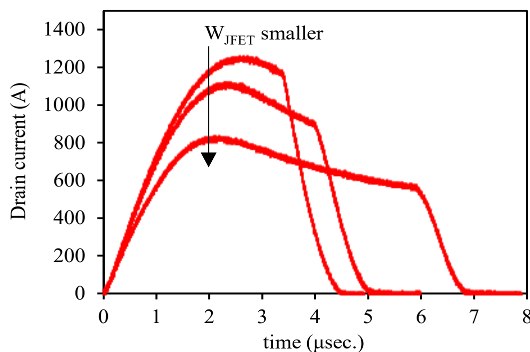

Fig. 7 Measured short-circuit characteristic of fabricated MOSFETs with various W_{JFET}.

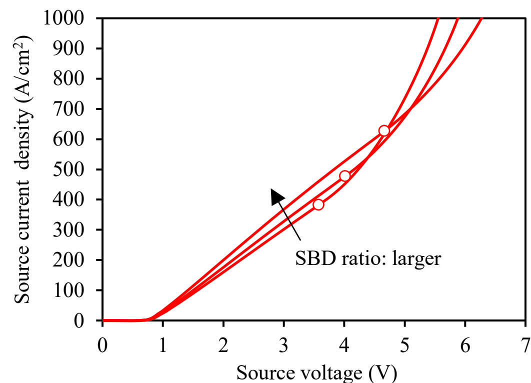

Fig. 9 Diode characteristics of 1.2-kV-class MOSFETs measured at the high temperature of 175°C. Circles on the line indicate J_{umax}.

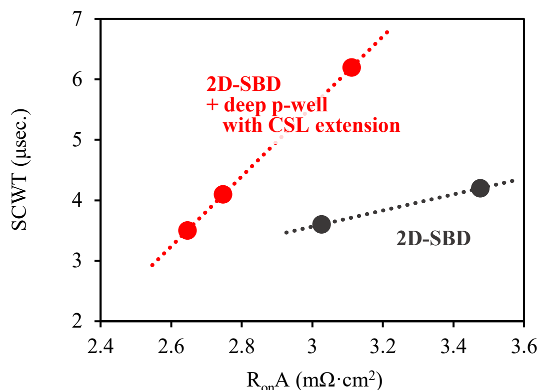

Fig. 8 Relationship between measured SCWT and $R_{on}A$.

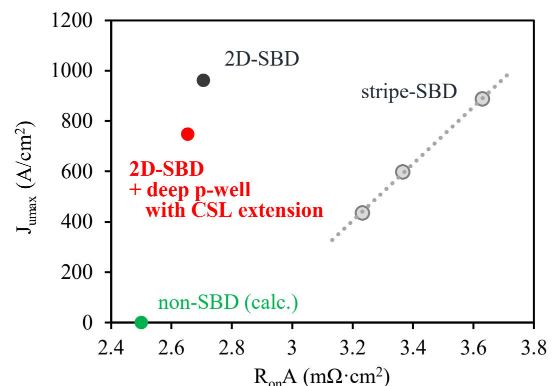

Fig. 10 Relationship between measured J_{umax} (175°C) and $R_{on}A$ (R.T.).

suppressed bipolar conduction more effectively. We also confirmed that $R_{on}A$ was not affected by enlarging SBD area ratio. This proves that ohmic contact and source drift have minor effects on the total resistance of the fabricated devices. Figure 10 shows the relation between J_{umax} and $R_{on}A$ of the MOSFETs with a typical design. Obtained J_{umax} was certainly smaller than that of the conventional device structure with shallow p-well depth. It is supposed that optimization, such as enlarging the SBD area ratio, would realize a better trade-off between J_{umnax} and $R_{on}A$. What is important is that feasibility of improving the trade-off of low $R_{on}A$, high J_{umax} and good SC ruggedness by the developed cell design is demonstrated.

IV. Resistance Reduction Utilizing Leakage Suppression

We examined further $R_{on}A$ reduction by aggressive tuning of the drift layer design. Figure 11 shows the simulated SBD leakage in SC condition when the various drift layer designs are adopted. Although leakage increased, thermal runaway was not observed owing to the excellent electric field reduction effect of the developed deep p-well structure. Fabricated MOSFET with the optimized design demonstrated ultra-low $R_{on}A$ of 2.0 mΩ·cm^2 (Fig. 12). Reduction in SBD leakage is an important effect that offers flexibility in designing the entire device structure of SBD-embedded MOSFET.

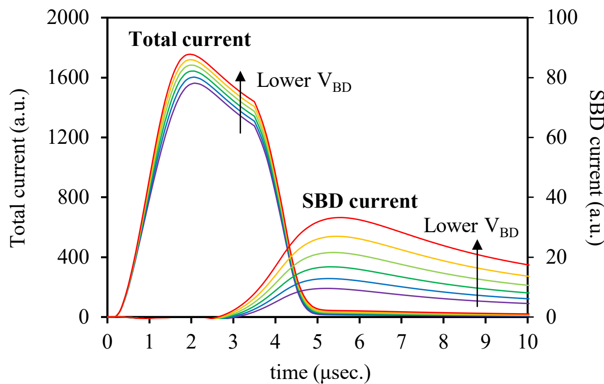

Fig. 11 Simulated SC characteristics of the structures with various drift layer designs. Vds=600V. Gate turn-on at 0- 3.5 microseconds. Breakdown voltage were culculated to be 1601, 1550, 1500, 1445 and 1383 V, respectively.

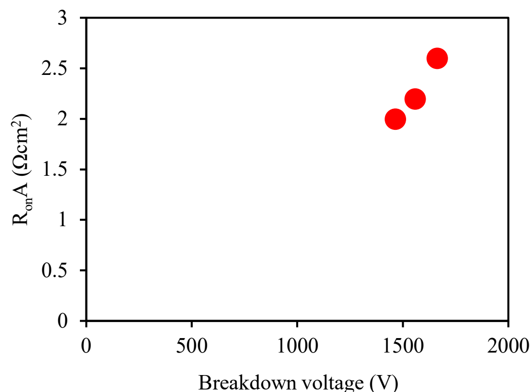

Fig. 12 Measured $R_{on}A$ and breakdown voltage of MOSFETs with various drift layer designs.

V. Summary

The device structure of SiC MOSFET with embedded SBD was investigated in order to improve the complicated trade-off relationship of on-state resistance, diode conduction capability, and SC ruggedness. Introducing deep p-well and modifying the shape of CSL structure were considered. TCAD simulation revealed optimal geometry to shield integrated Schottky junction and J_{umax} improvement effect by enhanced SBD current spreading. Fabricated 1.2-kV-class MOSFETs demonstrated improvement in the trade-off relationship between SC-ruggedness and $R_{on}A$ as the effect of introducing deep p-well structure. Measured diode characteristics showed good unipolar conduction capability although further tuning is desired. The developed design technology allowed the aggressive drift layer design and the fabricated device finally exhibited $R_{on}A$ of 2.0 mΩ·cm^2, which is outstandingly low for SBD-embedded 1.2-kV-class SiC MOSFET.

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