T. Nishiwaki et al., "Demonstration of Pseudo Independent Driving of Buried Gate in Trench Field Plate MOSFETs", 2024 36th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Bremen, Germany, 2024, pp. 355-358. Doi: 10.1109/ISPSD59661.2024.10579695

Demonstration of Pseudo Independent Driving of Buried Gate in Trench Field Plate MOSFETs

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***Abstract*—We have proposed pseudo independent driving technique of Gate and buried Field Plate (FP) gate in a Trench Field Plate Power MOSFET (Trench FP MOSFET). Proposed method is expected to low conduction loss due to biased buried FP gate as well as a Gate-connected buried FP gate (Gate FP) and high-speed switching as well as a Source-connected buried FP gate (Source FP) by using only three additional components and this module behaves like a conventional three-terminal power MOSFET. In this paper, we experimentally demonstrated static characteristics and dynamic switching performances of this pseudo independent driving. We fabricated proposed pseudo driving module with discrete components on DBC (Direct Bonded Copper) substrate. Breakdown voltage and diode characteristics of this module were comparable to the Source FP and the Gate FP. On-resistance of this module was lower than the Source FP and the same as the Gate FP. Turn-on and turn-off period of this module became shorter than the Gate FP and were almost comparable to the Source FP.**

Keywords— Trench Field Plate MOSFET, Gate-connected FP, Buried FP gate, Gate driving technique, Pseudo independent buried FP gate driving

I. INTRODUCTION

Trench Field Plate Power MOSFETs (Trench FP MOSFETs) [1] have responded strong demands such as high current capability for automotive applications and low loss switching for industrial applications. Low specific on-resistance ($R_{ON}A$), which contributes high current capability, of the Trench FP MOSFET have been achieved by charge coupling in ultra fine pitch trench structure. In addition, a Source-connected buried FP gate (Source FP) decreases Gate-Drain capacitance C_{GD} which corresponds to feedback capacitance C_{rss} [2]. This low C_{rss} characteristics enables us low loss switching. However, cell pitch shrinking of the Trench FP MOSFET is getting difficult and challenging because increase of transconductance (Gm) decreases Safe Operating Area (SOA) [3]. One of the other methods for reducing $R_{ON}A$ is a Gate-connected buried FP gate (Gate FP) [2, 4]. The accumulation effect of the Gate FP in the drift layer contributes reduction of drift resistance. However, it is known that the Gate FP is hardly used for high-speed switching due to its large C_{rss}. To overcome this issue, independent driving of the Gate and the buried FP gate was proposed and discussed [5]. Such multi-gate driving technique have been studied intensively on IGBT field to improve tradeoff between turn-on/off loss and conduction loss [6-8]. However, these proposed techniques need a dedicated gate driver or more than one gate driver per one device. This must be one of the significant issues of these gate control techniques.

We have proposed pseudo independent driving (pseudo driving) technique of buried FP gate in a Trench FP MOSFET and validate its operation by TCAD simulation [9]. This proposed method is expected to low conduction loss by the accumulation effect of biased FP gate (Fig. 1) as well as the Gate FP and high-speed switching as well as the Source FP by only

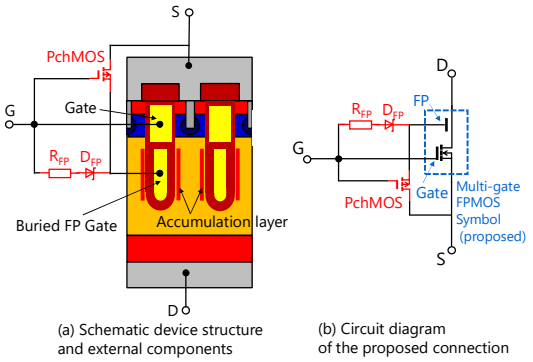

Fig. 1. Schematic device structure and proposed connection of the pseudo independent buried FP gate driving circuit. This module works like a conventional three-terminal power MOSFET device (Proposed in [9]).

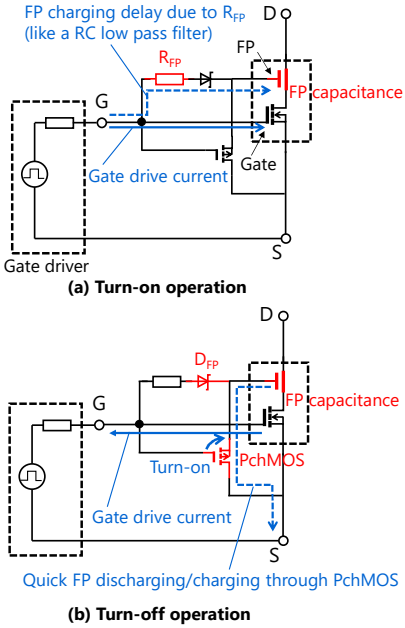

Fig. 2. Turn-on and turn-off operation mode of the pseudo independent buried FP gate driving module. R_{FP} and FP capacitance decrease turn-on period and PchMOS and D_{FP} decrease turn-off period (Proposed in [9]).

three additional components of a resistance R_{FP}, a diode D_{FP}, and a PchMOS (Fig. 2). In the case of turn-on operation depicted in Fig. 2(a), charging of the FP delays compared with the Gate because FP capacitance, which mainly consists of capacitance between the FP and the drain, and the R_{FP} work like an RC filter. This decoupling of the Gate and the FP realize lower effective C_{rss} then enables fast turn-on. In the case of turn-off operation shown in Fig. 2(b), quick charging/discharging of the FP through the PchMOS enables fast turn-off. The most significant feature is that this technique can be modularized, and this module looks like a pseudo three terminal device. Thus, we can use conventional gate drivers. In this paper, we fabricated this pseudo driving modules and experimentally demonstrated static characteristics and dynamic switching performances.

II. Fabricated Pseudo Gate Driving Modules

We fabricated Trench FP MOSFET dice which have a Gate and a buried FP gate pad as shown in Fig. 3(a). We assembled the proposed pseudo independent driving module on DBC (Direct Bonded Copper) substrate with discrete components as shown in Fig. 3(b). We prepared five types of DBC modules of a conventional Source FP, a conventional Gate FP, and proposed pseudo independent FP gate driving modules (Pseudo driving modules) as listed in Table I. These modules have three terminals of Gate, Drain and Source. Optional sense terminals of Source and Drain were prepared for on-resistance measurement. We measured their characteristics in the same way as conventional three terminal MOSFET.

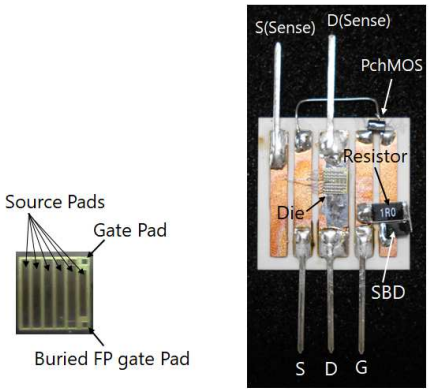

Fig. 3. (a) A photo of a dedicated multi-gate die which has the Gate and Buried FP gate pad, (b) a pseudo independent buried FP gate driving module assembled with discrete components on DBC substrate.

TABLE I. Fabricated Modules

No.	Connection	R_{FP}	D_{FP}[a]	PchMOS[b]
1	Source-connected FP	none	none	none
2	Gate-connected FP	none	none	none
3	Pseudo independent FP gate driving module	10 Ω	CMS01	SSM3J332R
4		3.3 Ω	CMS01	SSM3J332R
5		1.0 Ω	CMS01	SSM3J332R

[a] D_{FP}: CMS01 30V Si SBD (Toshiba)

[b] PchMOS: SSM3J332R -30V Si PchMOS (Toshiba)

III. Static Characteristics

Fig. 4 shows measured V_{DS}-I_D characteristics of the modules listed in Table I. When the buried FP gate is floating, breakdown voltage is low (about 22 V) due to premature breakdown. In contrast, proposed pseudo driving modules obtained comparable breakdown voltage to the Source FP and the Gate FP. We also confirmed the same body diode forward conduction characteristics of these modules as shown in Fig. 5.

Next, we estimated MOS conduction characteristics of the modules. These modules showed almost comparable V_{GS}-I_D characteristic as shown in Fig. 6. Fig. 7 shows typical Gate bias dependence of chip on-resistance (R_{ON}). The proposed pseudo driving modules achieved lower R_{ON} than the Source FP and almost the same R_{ON} as the Gate FP. As we proposed in [9], R_{ON} of the proposed pseudo driving modules decreased as Gate bias increase. If application allows applying Gate bias voltage higher, advantage of the proposed technique will increase.

We also measured small signal capacitance characteristics of the modules and compared with simulation results as shown in Fig. 8. C_{iss} and C_{rss} curves of the pseudo driving modules are located between the Gate FP and the Source FP because the buried FP gate is weakly coupled to the Gate via the R_{FP} and the D_{FP}. On the other hand, C_{oss} of the pseudo driving device looks lower than that of the Gate FP and the Source FP because the FP capacitance is decoupled from the Source and the Gate by the D_{FP} and the PchMOS. These tendency of capacitance curves agreed well with simulation results.

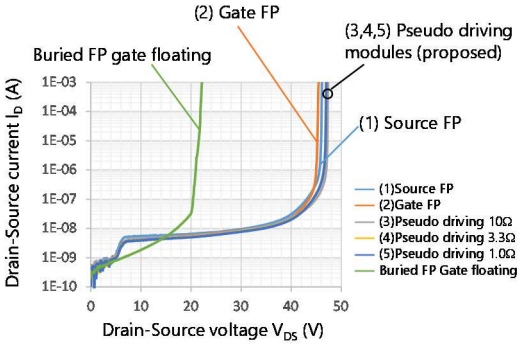

Fig. 4. Experimental V_{DS} - I_D characteristics of the modules listed in Table I. A characteristic of floating buried FP case was also plotted for the reference.

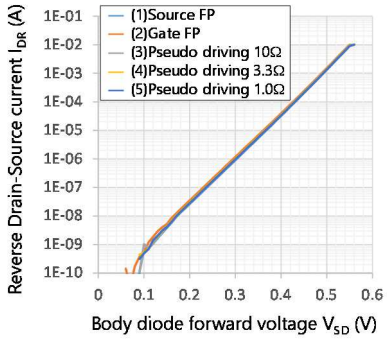

Fig. 5. Experimental body diode forward (3rd quadrant) characteristics of the modules listed in Table I. There are no diode characteristics difference among these modules.

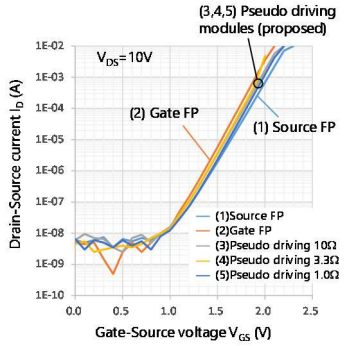

Fig. 6. Experimental V_{GS}-I_D characteristics of the modules.

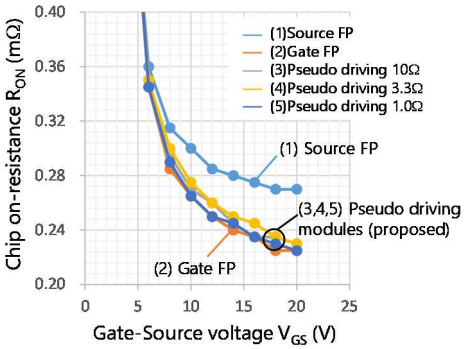

Fig. 7. Measured V_{GS} dependence of chip R_{ON}. R_{ON} of the proposed pseudo driving module decreased as V_{GS} increased, which was comparable to the Gate FP.

IV. Dynamic Characteristics

We evaluated both resistive load switching and Unclamped Inductive Switching (UIS) of the pseudo driving modules and compared with the Source FP and the Gate FP. Because proposed modules can be treated as three terminal Power MOSFET, we evaluated all modules with a conventional switching tester and an UIS tester as well as the Source FP and the Gate FP.

A. Resistive load switching performance

We evaluated resistive load switching performance of the modules as shown in Fig. 9 and 10. As we expected, turn-on period of the pseudo driving module (R_{FP} = 10 Ω) became shorter than that of the Gate FP as shown in Fig. 9. We confirmed the FP gate voltage (V_{FP}) rise delayed compared with the Gate voltage (V_{GS}) rise as the R_{FP} increased as shown in Fig. 10. These FP gate voltage behaviors are almost consistent with

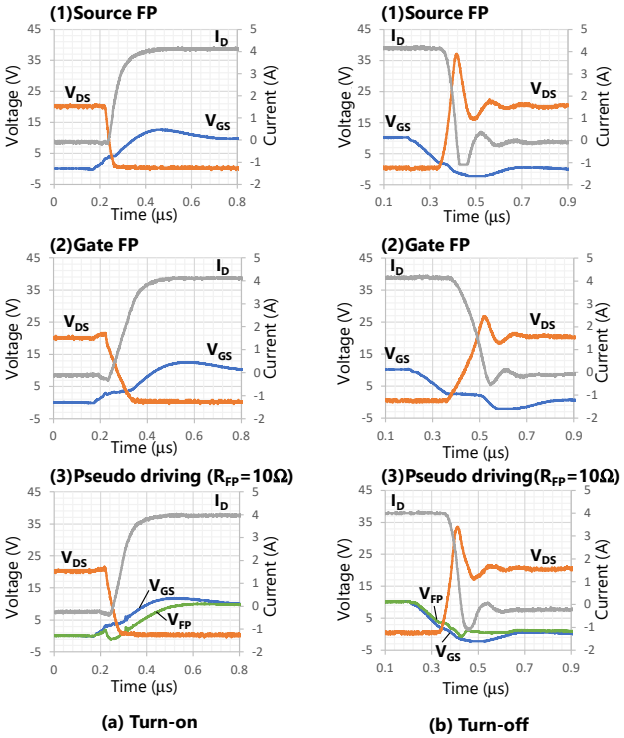

Fig. 9. Measured (a) Turn-on and (b) turn-off waveforms of resistive load switching among (1) the Source FP, (2) the Gate FP, and (3) the Pseudo driving module (R_{FP} = 10 Ω). External gate resistance R_G = 3.0 Ω, power supply voltage V_{DD} = 20 V, and load of resistance R_{load} = 4.6 Ω.

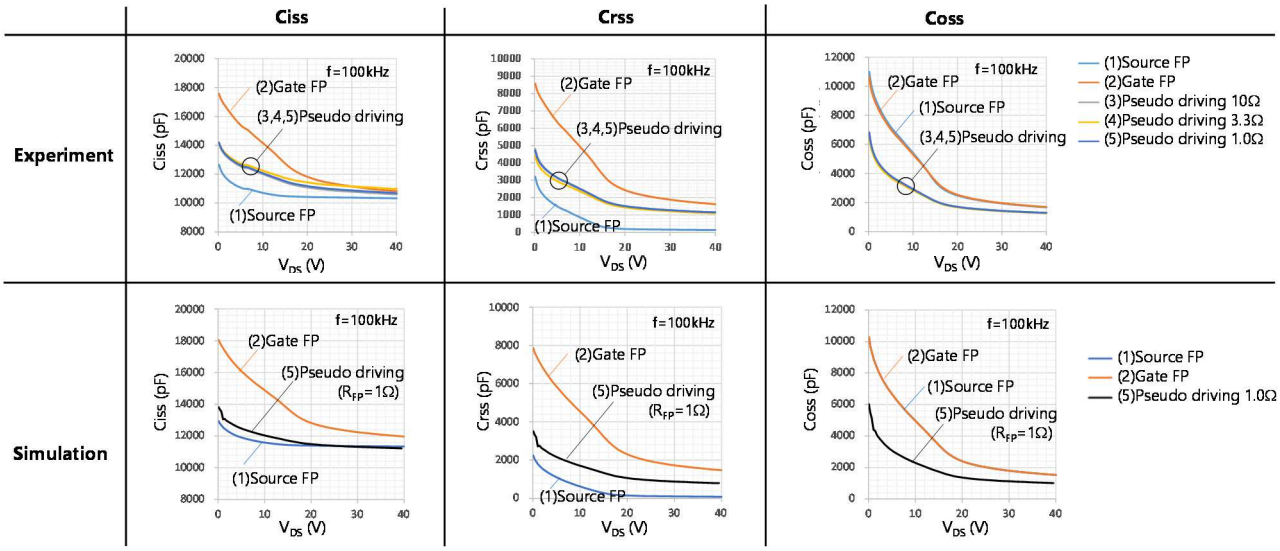

Fig. 8. Measured (upper row) and simulated (lower row) small signal capacitance characteristics (C_{iss}, C_{rss}, C_{oss}) of each module.

simulated waveforms [9]. Optimum R_{FP} value is determined by effective RC time constant, therefore it depends on the FP capacitance and the external gate resistance R_G value. In addition, faster turn-off which is comparable to the Source FP was achieved by pseudo driving modules. This is an effect of quick FP discharging/charging by bypass circuit which consists of the D_{FP} and the PchMOS.

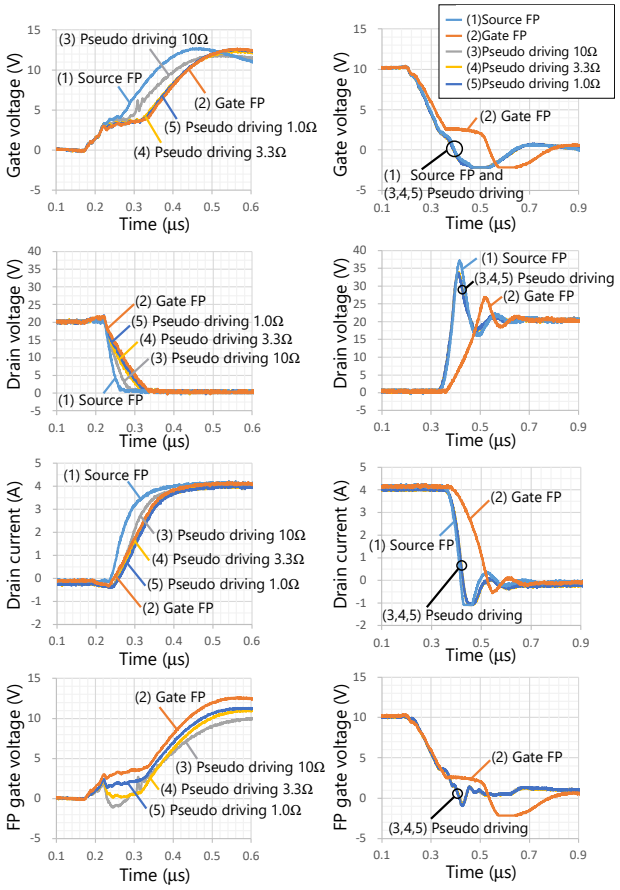

Fig. 10. Overlaid comparison of measured Gate voltage, Drain voltage/current and FP gate voltage waveforms of (a) turn-on and (b) turn-off in resistive load switching among (1) the Source FP, (2) the Gate FP, and (3,4,5) the Pseudo driving modules (R_{FP} = 10, 3.3, 1.0 Ω). Turn-on of the pseudo driving became faster and closer to the Source FP as the R_{FP} increased. Turn-off period of the pseudo driving was comparable to the Source FP.

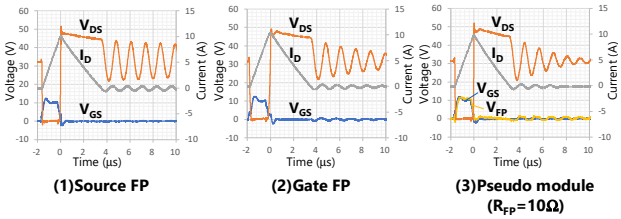

Fig. 11. Measured Unclamped Inductive Switching waveforms of (1) the Source FP, (2) the Gate FP and (3) the Pseudo driving module (R_{FP} = 10 Ω). Load inductance was 20 μH, power supply voltage was 32 V, and external Gate resistance was 3 Ω.

B. Unclamped Inductive Switching (UIS) performance

We also evaluated UIS performance of the modules. Fig. 11 shows UIS waveforms of the Source FP, the Gate FP, and the Pseudo driving modules. We demonstrated successful UIS switching operation of this pseudo driving module. Interestingly, the oscillation of the V_{DS} of the pseudo module after finishing avalanche period was suppressed compared with the Source FP. This might be due to damping effect of equivalent RC snubber circuit which consists of the FP capacitance and the R_{FP}.

V. CONCLUSIONS

We fabricated the pseudo driving modules using discrete components on DBC and demonstrated their static and dynamic performances. We confirmed that proposed pseudo independent driving technique realized lower on-resistance than the Source FP and achieved very close switching speed of the Source FP. We also demonstrated the UIS performance of the pseudo driving modules. We believe that the proposed concept of pseudo driving push forward implementation of multi-gate driving not only FPMOS but also other power devices.

ACKNOWLEDGEMENT

The authors would like to thank Mr. Keita Saito, Mr. Kota Tomita for fabricating the sample chips, and Mr. Yusuke Kawaguchi for significant discussions.

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