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Novel Approach to Mitigate Parasitic Oscillation of Power Modules with Parallel Connected SiC-MOSFETs

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***Abstract*—In a power module with multiple MOSFETs connected in parallel, a type of current oscillation known as "parasitic oscillation" can occur during switching. Parasitic oscillation can lead to module failure, so a means of mitigating parasitic oscillation is required. In this paper, we derived oscillation conditions using the Monte Carlo method as well as theoretical analysis of an equivalent circuit, using a simplified circuit model of two chips connected in parallel. Furthermore, we showed that it is possible to apply the oscillation condition to any number of parallel chips by considering them to be equivalent to a two-chip model by performing an appropriate equivalent-circuit transformation. According to these conditions, increasing the value of L_g/L_s is effective for mitigating parasitic oscillation. To verify the above considerations, we fabricated power modules with different L_g/L_s values and performed switching measurements. The results revealed that the module with higher L_g/L_s values mitigated oscillation without increasing switching loss. This novel approach might be useful in designing the wiring structure of power modules.**

Keywords—SiC, MOSFET, power module, switching, parasitic oscillation, parallel connection

I. Introduction

When multiple MOSFETs are connected in parallel in a power module, an unexpected type of current oscillation known as "parasitic oscillation" can occur during switching, potentially leading to module failure. In general, parasitic oscillation is suppressed by increasing internal gate resistance (R_{g_int}) [1], increasing gate-to-gate inductance (L_g) [2], or reducing source-to-source inductance (L_s) [3]. Increasing gate impedance results in higher switching losses, so reducing L_s is desirable. However, simply lowering L_s by shortening the wiring between chips increases the thermal interference between chips, which has a negative effect on heat dissipation. In addition, there is a constraint on the extent to which L_s can be reduced because parallel chips must be separated to avoid thermal interference. Therefore, it is necessary to design a wiring structure that suppresses oscillation without increasing losses within the given constraints. The purpose of this work is to reveal the quantitative oscillation conditions by performing a Monte Carlo simulation as well as theoretical analysis of an equivalent circuit, using a simplified circuit model of two MOSFET chips connected in parallel and to propose a novel approach to designing an optimal wiring structure that does not oscillate and does not increase losses. This approach is verified by performing switching measurements of the fabricated modules.

II. Oscillation Simulations of a Circuit Model of Two MOSFET Chips Connected in Parallel

A. Approach

In the case of considering oscillations inside a module, external circuits can be eliminated [4]. Fig. 1 shows an equivalent circuit of two identical MOSFET chips connected in parallel, where wiring resistances and R_{g_int} are ignored. The circuit constants are parasitic capacitances (C_{gd}, C_{ds}, C_{gs}) and stray wiring inductances (L_d, L_s, L_g), which includes the bonding wires and circuit patterns. The inductances are virtually divided at the midpoint between the two chips. We created a half-bridge simulation model by adding a power supply, gate driver, load, and reverse-side freewheeling diode, as shown in Fig. 2. We performed switching simulations using the Monte Carlo method, with (L_d, L_s, L_g) as variables. Based on the results, we analyzed the conditions for cases with and without oscillation. Then, we considered this using the equivalent circuit.

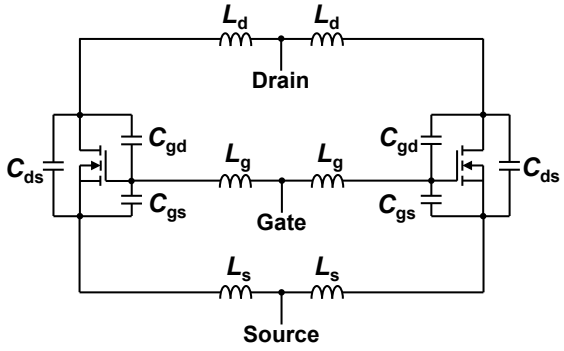

Fig. 1. Equivalent circuit of two MOSFET chips connected in parallel. L_d, L_s, L_g are the half inductances of drain-to-drain, source-to-source, and gate-to-gate, respectively. C_{dg}, C_{ds}, C_{gs} are the capacitances of drain-to-gate, drain-to-source, and gate-to-source, respectively.

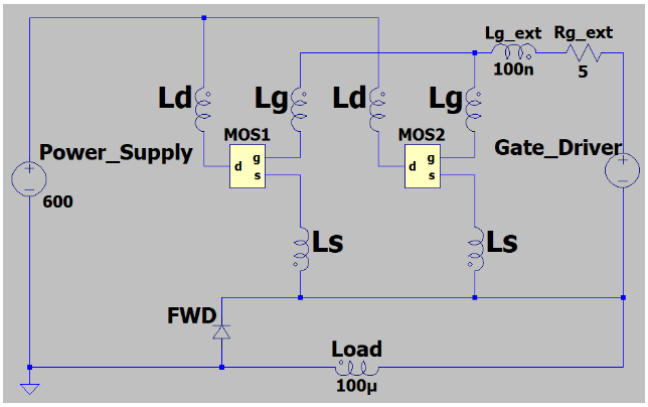

Fig. 2. Half-bridge circuit simulation model. L_{g_ext} [H] is a common inductance of wiring to the gate driver, R_{g_ext} [Ω] is a common external gate resistor. In the simulations, the supply voltage was 600 V and the load current was 100 A.

B. *Visualization of the Oscillation Condition by Monte Carlo Method*

We performed 2,000 simulations in which the model shown in Fig. 2, with (L_d, L_s, L_g) as random parameters. Based on the results, the waveforms for one chip were classified according to their parameters into oscillating cases (Fig. 3) and non-oscillating cases (Fig. 4). The waveforms were automatically classified according to the peak amplitude of the Fourier spectrum of drain currents, based on predetermined criteria. Fig. 5 shows the classified oscillation distribution of 2,000 simulations plotted as (L_d, L_s, L_g). From Fig. 5, it can be seen that the oscillation distribution does not depend on L_d. When drawn on a two-parameter plane (L_s, L_g) without L_d, the boundary becomes a straight line as $L_g = 4.3L_s$ (Fig. 6).

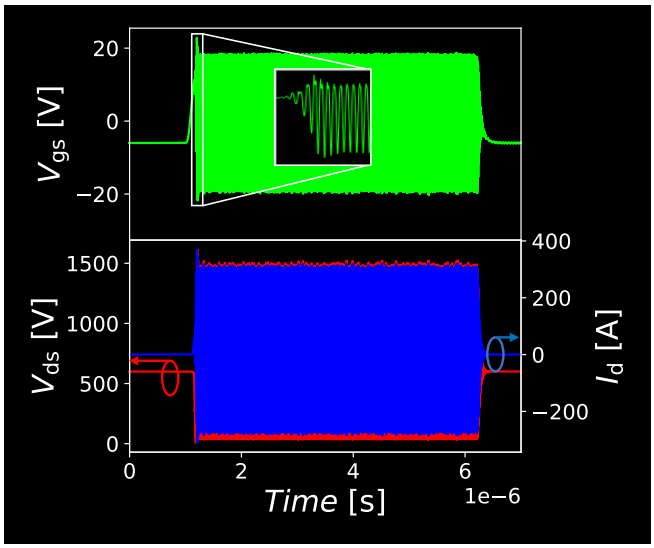

Fig. 3. Simulated waveform switching in one chip in oscillating cases. V_{gs} is the gate-to-source voltage, V_{ds} is the drain-to-source, and I_d is the drain current.

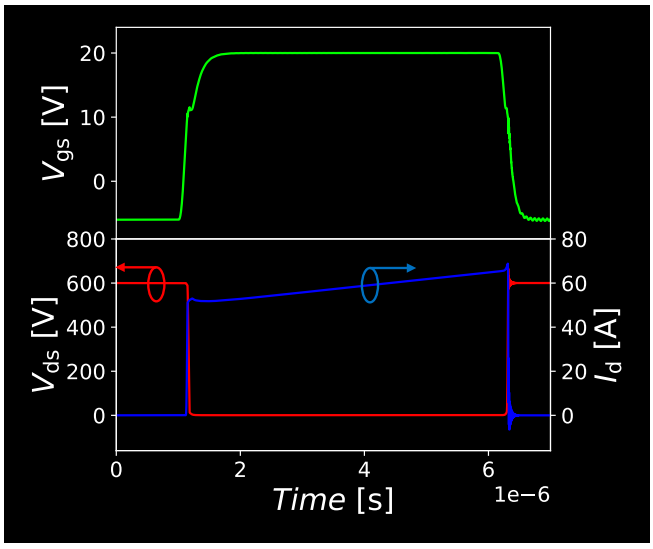

Fig. 4. Simulated waveform switching in one chip in non-oscillating cases.

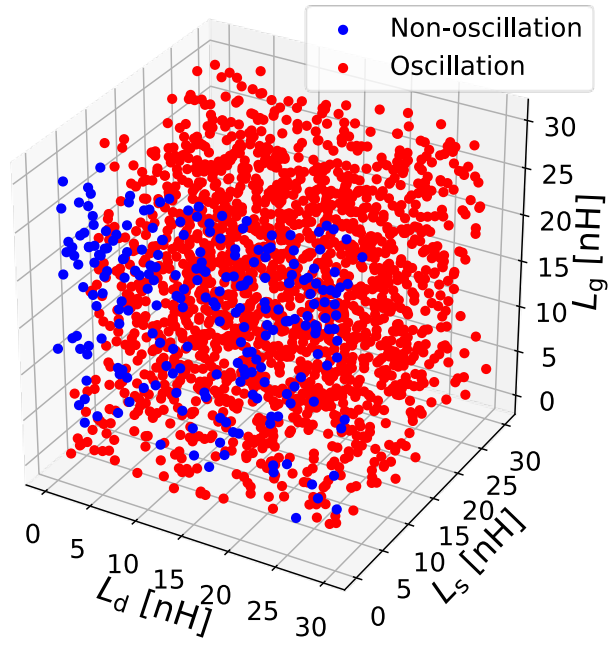

Fig. 5. Results of 2,000 simulations, with classifications plotted as (L_d, L_s, L_g).

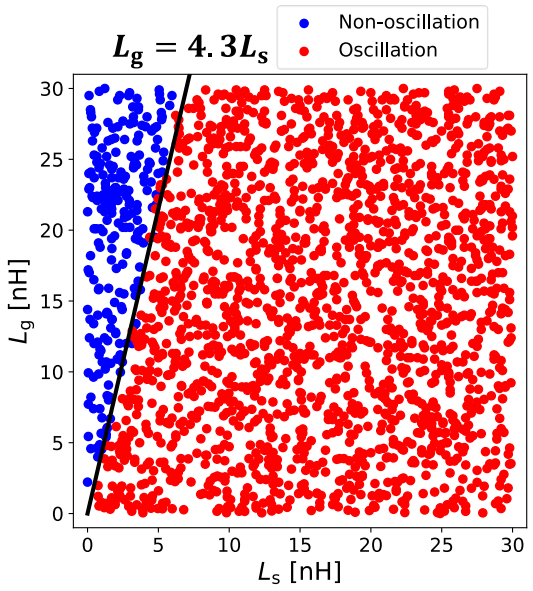

Fig. 6. Results of 2,000 simulations, with classifications plotted as (L_s, L_g).

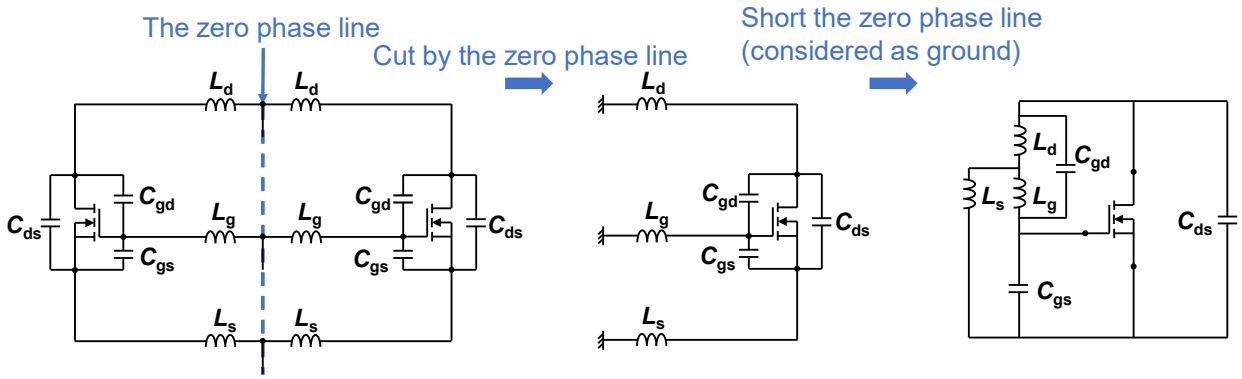

Fig. 7. Transformation of the equivalent circuit shown in Fig. 1.

C. *Theoretical Considerations Using an Equivalent Circuit*

We considered the above results using an equivalent circuit. The circuit in Fig. 1 can be transformed as shown in Fig. 7 [5]. When two MOSFETs oscillate simultaneously, current flows through each chip in opposite phases. In this case, the midpoint between the two chips (the dashed line in Fig. 7) is always zero phase at the oscillating frequency and can be shorted as a virtual ground. Additionally, we can ignore L_{d} and C_{gd}, as shown in Fig. 8 (a), because they are typically very small. This is similar to the Colpitts oscillator shown in Fig. 8 (b) [1][6], except that L_{s} is connected in parallel with C_{ds}. Generally, oscillation conditions can be calculated by (1) and (2) [1].

$$\mathrm{Re}(AH) \geq 1 \tag{1}$$

$$\mathrm{Im}(AH) = 0 \tag{2}$$

Here, AH is the loop gain. In the case of the Colpitts oscillator shown in Fig. 8 (b), (1) and (2) become (3) and (4), respectively [1], where $\mu = G_{\mathrm{m}}R_{\mathrm{ds}}$, G_{m} is transconductance, R_{ds} is drain-source resistance, and ω is frequency.

$$\frac{\mu}{\omega^2 L_2 C_3 - 1} \geq 1 \tag{3}$$

$$C_1 + C_3 - \omega^2 L_2 C_1 C_3 = 0 \tag{4}$$

From (3) and (4), the oscillation conditions of the Colpitts oscillator can be calculated by (5) [1].

$$\mu \geq \frac{C_3}{C_1} \tag{5}$$

In Fig. 8 (a), by using $C_{\mathrm{ds}} - \frac{1}{\omega^2 L_{\mathrm{s}}}$ instead of C_1 in (3) and (4), we calculated the oscillation conditions of the circuit shown in Fig. 8 (a) by (6).

$$\frac{L_{\mathrm{g}}}{L_{\mathrm{s}}} \leq \left(1 + \frac{1}{\mu}\right)\left(\frac{C_{\mathrm{ds}}}{C_{\mathrm{gs}}}\mu - 1\right) \tag{6}$$

The condition (6) is similar to $L_{\mathrm{g}}/L_{\mathrm{s}} \leq (\mathrm{Const.})$, in that it is consistent with the condition revealed by the Monte Carlo simulations. Considering this condition, we can design a wiring structure that does not oscillate if we modify $L_{\mathrm{g}}/L_{\mathrm{s}}$.

In the above considerations, only two chips are connected in parallel, but in actual modules, there may be three or more chips connected in parallel. Therefore, it is necessary to extend the above considerations to any number of parallel chips. Fig. 9 (a) and (b) shows the connection of source and gate inductances, respectively, in the case of two chips connected in parallel and in the generalized case of N chips in parallel. Inductances between chips are virtually divided in half at the midpoints. As in the above considerations, the circuit of two chips connected in parallel shown in Fig. 9 (a) could be shorted at the midpoint of the inductances as the ground. In the case of N chips connected in parallel shown in Fig. 9 (b), if we focused on one chip with index i, we could consider all combinations of two chips, including the chip with index i individually. Then, the midpoints of each combination could be shorted in the same way as the case of two chips connected in parallel. The equivalent circuit between the source and gate of the chip with index i consists of parallel synthesis from the inductances of each two-chip combination. Thus, we can consider the oscillation condition of N chips in parallel to be the same as that for two chips connected in parallel. In the oscillation condition for the chip with index i, we can use $L_{\mathrm{g}i}/L_{\mathrm{s}i}$ as defined by the parallel synthesis of L_{g}, L_{s} from one chip with index i to all other chips, instead of $L_{\mathrm{g}}/L_{\mathrm{s}}$ in two chips connected in parallel as (6). This can be applied to every chip in parallel individually.

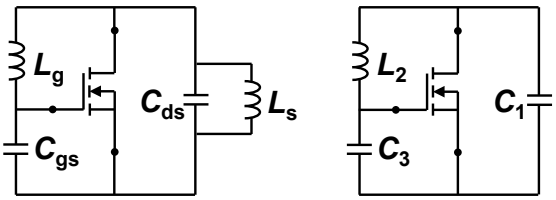

Fig. 8. Comparison of the equivalent circuit ignoring L_{d} and C_{gd} as shown in Fig. 7 (a) with the Colpitts oscillator (b).

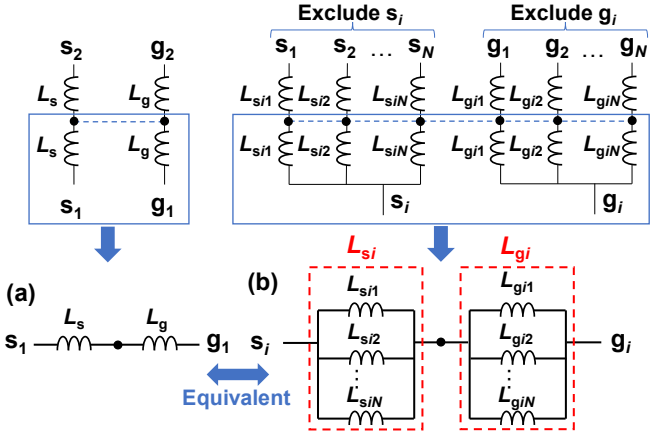

Fig. 9. Transformation of the equivalent circuit in the generalized case of N chips in parallel (b) and comparison with two chips in parallel (a). Here, s_i, g_i are the source or gate electrode of a chip with index i ($i = 1 \sim N$). L_{sij}, L_{gij} are half-inductances of source-to-source and gate-to-gate between a chip with index i ($i = 1 \sim N$) and a chip with index j ($j = 1 \sim N, j \neq i$).

III. Verification by Performing Switching Measurements of Fabricated Modules

To verify the above considerations experimentally, we fabricated three SiC modules with different L_{gi}/L_{si} and internal gate resistance R_{g_int} values, using the same chip layout. A picture of the module is shown in Fig. 10. The modules have more than three chips in parallel, but we compared the modules with the minimum value of L_{gi}/L_{si} for each chip in parallel because that chip is most likely to oscillate. The L_{gi}/L_{si} value was determined by electromagnetic field analysis. By focusing on one chip electrode and considering all other parallel chips as a common electrode, L_{gi} and L_{si} can be obtained by calculating the inductances between those electrodes for source and gate, respectively. This minimum value of L_{gi}/L_{si} can be modified by adjusting the source wiring between chips. The configuration is shown in Table I. We measured the switching waveforms (Fig. 11) and calculated the switching losses (Table II). From the measurement results, increasing R_{g_int} or the minimum value of L_{gi}/L_{si} mitigates oscillation; the former increases losses while the latter does not. From the simulations and experiments, we verified the novel approach that increasing the minimum value of L_{gi}/L_{si} by adjusting the source wiring can mitigate oscillation without increasing loss, even when more than three chips are connected in parallel.

Fig. 10. Photograph of the fabricated SiC module.

TABLE I. Configuration of the Fabricated Modules.

Configurations	Module (a)	Module (b)	Module (c)
R_{g_int} (chip) [Ω]	12	30	12
L_{gi}/L_{si} (minimum)	2.10	2.10	3.86

IV. Conclusion

In this paper, with the aim of designing an optimal wiring structure for a power module that mitigates oscillation without increasing losses, we derived the theoretical oscillation conditions from Monte Carlo simulations and an equivalent circuit using a simplified circuit model of two chips in parallel. The theoretical oscillation condition is expressed by (6), where the L_g/L_s values are the wiring inductances that affect oscillation. Any number of chips connected in parallel can be considered equivalent to two chips connected in parallel by performing the appropriate equivalent-circuit transformation, and the parallel synthesis of L_g, L_s from one chip with index i to all other chips can be defined as L_{gi}, L_{si}. Once defined, the oscillation conditions are obtained using L_{gi}/L_{si} for each chip instead of L_g/L_s in (6). To verify the above considerations, we fabricated modules having different L_{gi}/L_{si} and R_{g_int} values and performed switching measurements. The results revealed that the module with a higher minimum value of L_{gi}/L_{si} can mitigate oscillation without increasing loss. This novel approach to mitigating oscillation might be useful in designing the wiring structure of power modules.

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TABLE II. Measured Turn-On and Turn-Off Losses (E_{ON}, E_{OFF}) of Each Module.

Measurement conditions		Module (a)	Module (b)	Module (c)
I_d = 100 A	E_{on} [mJ]	1.78	2.94	1.80
	E_{off} [mJ]	1.68	2.14	1.61
I_d = 600 A	E_{on} [mJ]	N/A	6.69	4.89
	E_{off} [mJ]	N/A	29.26	24.66

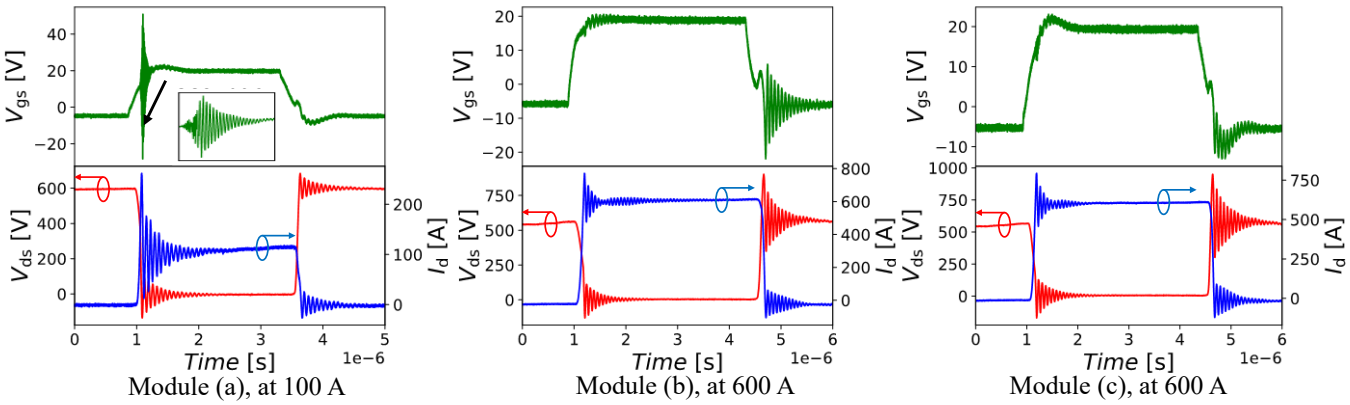

Fig. 11. Measured switching waveforms of the fabricated modules at 600 V and 25 °C. The external gate resistor was 1 Ω.