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3D integration technology with photosensitive mold for fan-out package

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An innovative 3D packaging and integration technology with a newly developed photosensitive mold material was successfully demonstrated. This technology needs neither a tall Cu pillar electroplating nor a laser drilling. A test die was mounted face up on a substrate, then a more than 100 μm thick photosensitive mold film was laminated on the whole substrate. The lithography process on the mold film was executed to make openings with depth of 10 μm on the embedded die, and with depth of 110 μm on the substrate. The Cu redistribution layer formed the electrical contacts between the die and the substrate through the photosensitive vias with different diameters and depths. The developed 3D package passed 1000 thermal cycles at −55/125 °C. This work disclosed future capability of a fan-out process using a photosensitive mold, thereby realizing a rapid growth of 3D integrated modules. © 2021 The Japan Society of Applied Physics

1. Introduction

Fan-out wafer-level packaging (FOWLP) technology eliminates wire bonding or solder bumping and package substrate,[1–6] potentially leading to lower cost, lower profile and better electrical performance, thereby is now extending to 3D integration.[7–10] Using package-on-package (PoP), the present 3D fan-out package technology has already achieved high-density interconnections between logic devices and memory devices in mobile applications.[11–13] The PoP-based packages using epoxy molding compound (EMC) usually build tall Cu pillars by long time-consuming electroplating following thick photoresist patterning process.[14–18] In order to interconnect the two packages, it is necessary to expose the top surface of the Cu pillar by chemical mechanical planarization (CMP) of the mold surface. The thick photoresist patterning and CMP process needed to fabricate the tall Cu pillars is costly. Therefore, various approaches have been developed to reduce the cost and increase the density of through-molded interconnects.[19–21] Vertical wire bonding is one of the technologies to achieve lower production costs and improve high-density interconnections.[22–24] These process schemes are called "Pillar First." In traditional printed circuit board manufacturing field, "Via First" process using laser drilling is executed to open vias in a non-photosensitive and filler-containing EMC,[25–28] but does not have the same process capability as the latest PoP-based packages require for the tall electroplated Cu pillars.[9,10] We have developed advanced "Via First" process utilizing a newly developed photosensitive mold material for 3D FOWLP integration to offer an affordable process scheme instead of conventional EMC.[29,30]

This paper deals with the process description of the key packaging processes such as die mounting, photosensitive film lamination, photolithography for photo via opening, and metallization layer formation for Cu redistribution layer (RDL). In particular, the two lithography process options were discussed to form vias with different depths and sizes. The process margin evaluation of the photo via opening was also discussed in this paper. Furthermore, the reliability assessment was demonstrated with the developed 3D package. The novel developed photosensitive mold material has characteristics of a higher coefficient of thermal expansion (CTE) and a lower elastic modulus,[29] compared to the traditional EMC for a usual FOWLP. Therefore, it is considered that the thermal stress in Cu RDL caused by its high CTE usually influences the reliability of thermal cycling. To analyze the effect of the microstructure of the electroplated Cu film after thermal cycling, growth behavior of the Cu grains and the strain have been investigated by electron backscatter diffraction (EBSD) analysis.

2. Photosensitive mold material

2.1. Value proposition

The newly developed 3D fan-out package is featured by the utilization of a photosensitive mold material instead of the traditional non-photosensitive EMC containing fillers. The photosensitive mold is mainly composed of silicone and does not contain any fillers.[29] The material has merits for the application to the fan-out package. Firstly, in contrast to traditional EMC, the photosensitive mold material provides fine-pitch photosensitive vias and high flexibility for applications in hetero-integration technologies. Secondly, the lateral wall quality on a photo via opening is smooth because it has filler-less, which allows for smaller via formation and finer via pitch. Thirdly, the film material will be suitable for panel-level packaging processes.[31–34] Applying a material with the above properties to package structure will realize higher design flexibility and improved productivity for 3D integration.

Figure 1 shows the proposed process using photosensitive mold material to realize 3D integration. A thick photosensitive mold film is applied to a substrate on which multi dies are mounted, and then the surface is planarized [Figs. 1(a) and 1(b)]. The photolithography process is applied to fabricate vias with different depths and sizes [Fig. 1(c)]. A metallization layer is fabricated to connect to multi dies and substrate [Fig. 1(d)]. This process is unique in that via openings with different depths and sizes can be fabricated using the lithography process, and RDL can be formed for various opened vias using electroplating at the same time.

2.2. Comparison with reference Cu pillar process

3D fan-out packages using the Cu pillar process have already been in high volume production for some mobile applications.[9,10] However, the thick photoresist and CMP processes needed to fabricate the tall Cu pillars are very expensive. Figure 2 shows a comparison of the process flow of interconnection between the die and the substrate for the

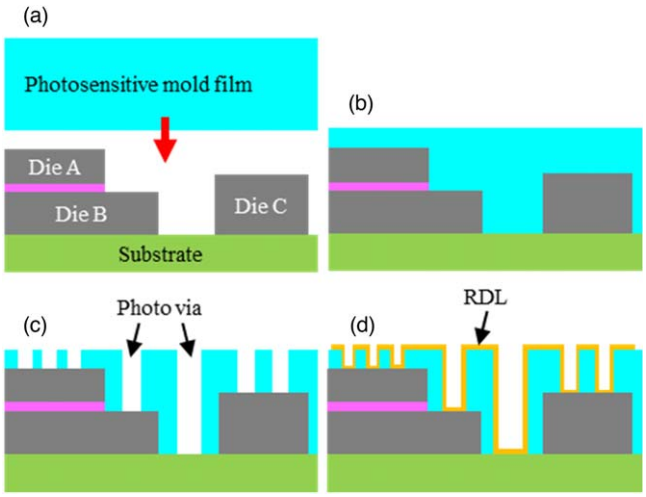

Fig. 1. (Color online) The proposed process using photosensitive mold material for 3D integration. (a) Mounting of multi dies on base substrate. (b) Thick photosensitive mold film lamination and surface flattening. (c) Via opening. (d) Metallization layer formation.

Cu pillar and the proposed photo via. It shows that the photo via process offers a simplified process flow. The photo via process does not need the Cu pillar and CMP process. In addition, using the lithography process, via openings on the die and on the substrate are formed at the same time. Furthermore, in contrast to Cu pillar processes, the Cu electroplating in this process has no need for Cu bottom-up filling in the vias. It means that low-cost Cu conformal electroplating can be used. This new approach promises to reduce costs and improve productivity.

3. 3D fan-out package process

3D packaging process integration with photosensitive mold was evaluated using Si test dies. The objectives were to confirm feasibility and evaluate the reliability test of the 3D integration package. Table I shows the die specification. It is 10 mm × 10 mm with 100 μm thickness and over 2000 vias

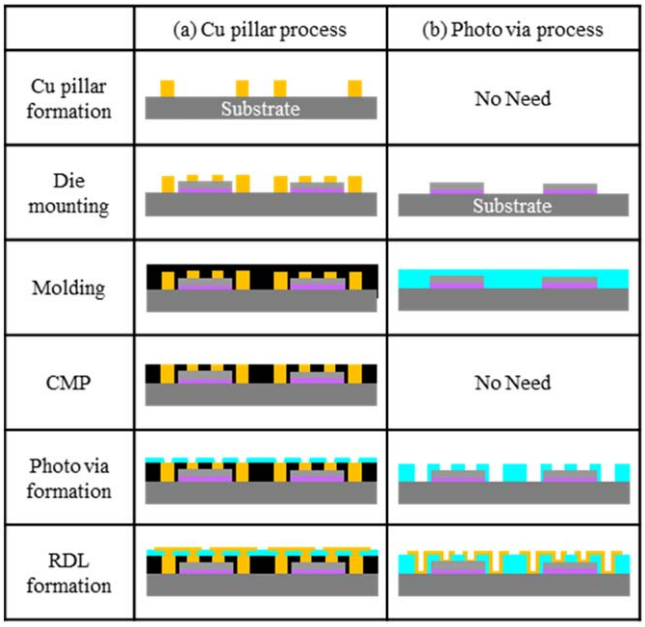

Fig. 2. (Color online) Comparison of the process flow for 3D FOWLP. (a) Cu pillar process. (b) Photo via process.

Table I. Die specification.

Size (mm)	10 × 10
Thickness (μm)	100 (including DAF)
Pad pitch (μm)	200
Pad count	2116

with 200 μm pitch on the die. The fabrication process for the package with photosensitive mold was done as indicated in Fig. 2(b).

3.1. Die mounting

Firstly, the die was mounted face up on 8 inch Si substrate as shown in Figs. 3(a)–3(b). Cu pad with 300 μm pad pitch was formed by electroplating on the Si substrate before a die with Al bond pad with 200 μm pad pitch was mounted as shown in Figs. 3(c)–3(d). Die and Si substrate were connected through die attach film (DAF) using die bonder achieving high bonding accuracy of less than ±5 μm. The bonding conditions were 120 °C, 0.1 MPa, and 5 s. In total, 72 dies were mounted on the substrate with a 15.08 mm pitch.

3.2. Photosensitive film lamination

After die mounting, dies with 100 μm thickness were embedded in a more than 100 μm thick photosensitive mold film using a vacuum lamination process. Since the material has very low viscosity, it can be used to embed components with height and flatten their surfaces. To confirm the flatness after the film formation, the film thickness from the substrate to the surface of the film was measured at the die area (y) and die side area (x) using cross-sectional analysis as shown in Fig. 4. Figure 5 shows the results of the film thickness at three points from the center to the edge of the Si substrate. It can be seen that the gap between the film thickness on the substrate (x) and the film thickness on the embedded die (y) was about 4.1 μm at the wafer center. Because the film has low viscosity, the film thickness of the

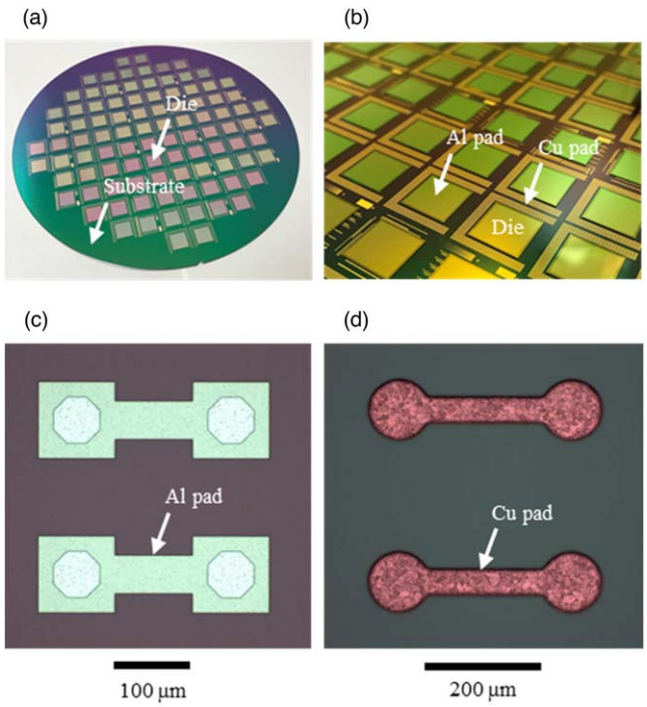

Fig. 3. (Color online) Photograph of die mounting. (a) 8 inch Si wafer with 72 dies mounted. (b) Top view after mounting. (c) Al bond pad on the die. (d) Cu pad on the substrate.

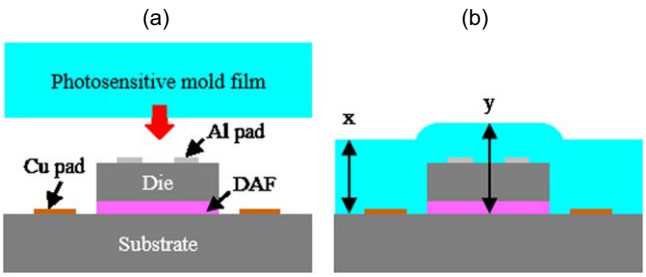

Fig. 4. (Color online) Film lamination process. (a) Before film lamination. (b) After film lamination.

wafer edge tends to be thinner. However, the trend of the gap remains the same at the wafer edge as well as at the wafer center. It is assumed that a gap of less than 5.0 μm is acceptable for the RDL formation.

3.3. Photo via formation

After the photosensitive film was cured to achieve a thickness of 110 μm on the substrate, the lithography process was implemented to make vias with depth of 10 μm on the Al pad of the embedded chip (shallow via) and vias with depth of 110 μm on the Cu pad of the substrate (deep via) [Fig. 6(a)]. The relationship between exposure amount and top diameter of different depth vias is shown in Fig. 7. From this figure, it can be seen that the diameter of the vias tends to decrease as the amount of exposure increases. This tendency is a reasonable result because this material is of negative type, in which light-irradiated areas do not dissolve during the development process using a solvent. There are two lithography processes that can be selected to fabricate vias with different depths and sizes. One is a multiple exposure process using photomasks designed for each via depth as described in Fig. 7(a). It means that two different photomasks are required to open vias of two different depths in the exposure process. In the other process, using exposure conditions that target the deepest via openings described in Fig. 7(b), all via openings with different depths are fabricated in a single exposure using one mask.

In this work, the mask diameters for shallow vias and deep vias were respectively designed at 60 and 100 μm. The exposure condition for the fabrication of shallow vias was adopted as 400 mJ cm^{-2}. The shrinkage from the mask diameter was confirmed as 6 μm. Similarly, the exposure condition for the formation of deep vias was adopted as 1600 mJ cm^{-2}. The shrinkage from the mask diameter was

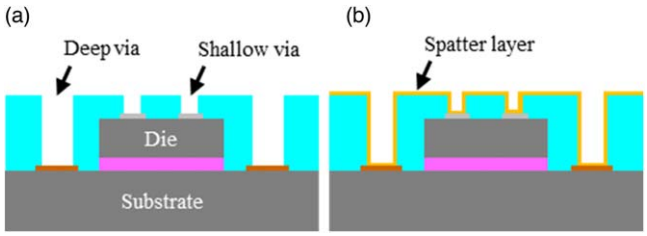

Fig. 6. (Color online) (a) Via opening. (b) Ti/Cu sputtering deposition.

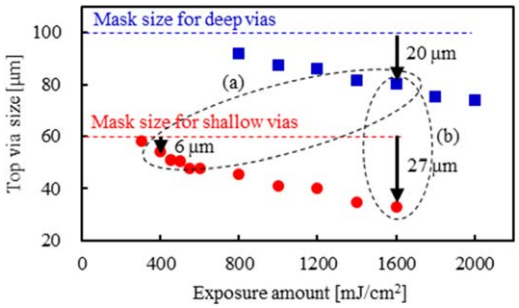

Fig. 7. (Color online) Relation between the exposure dose and via top diameter. (a) Multiple exposure process, (b) one-time process.

also confirmed as 20 μm [Fig. 7(a)]. On the other hand, if the exposure amount of shallow vias is the same as that of deep vias (1600 mJ cm^{-2}), it is possible to fabricate shallow vias by considering the large shrinkage (27 μm) of shallow vias [Fig. 7(b)]. This one-time process is a cost-effective solution for greater productivity improvement.

Using the optimized exposure condition (1600 mJ cm^{-2}) for forming deep vias, the via opening of various sizes was evaluated with three film thicknesses (70, 85 and 110 μm) and five mask diameters (60, 70, 80, 90 and 100 μm) as shown in Fig. 8. It can be seen that the deep via with an aspect ratio (AP) larger than 2.9 could not be formed. The AP of a via is the ratio between the depth of the hole and the diameter of the hole. From this evaluation, the target deep via with the film thickness of 110 μm and the mask of 90–100 μm was selected.

3.4. RDL formation

Cu RDL was fabricated to connect Al bond pads on the die with Cu pads on the substrate using Ti/Cu sputtering deposition, photoresist patterning, Cu electroplating, photoresist removal, and etching of sputter-deposited Ti and Cu. Sputtering depositions were performed with physical vapor

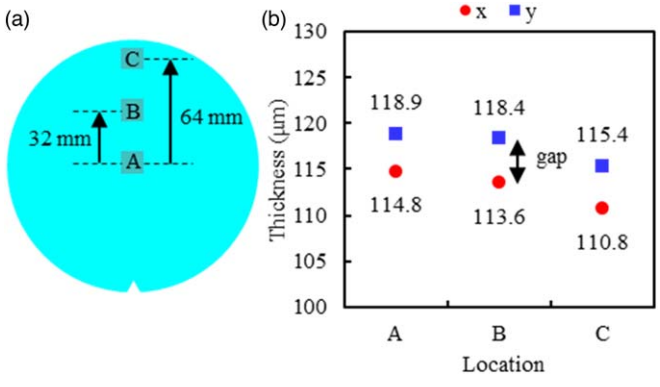

Fig. 5. (Color online) Thickness measurement of the photosensitive film after film lamination. (a) Location of die. (b) Results of thickness measurement.

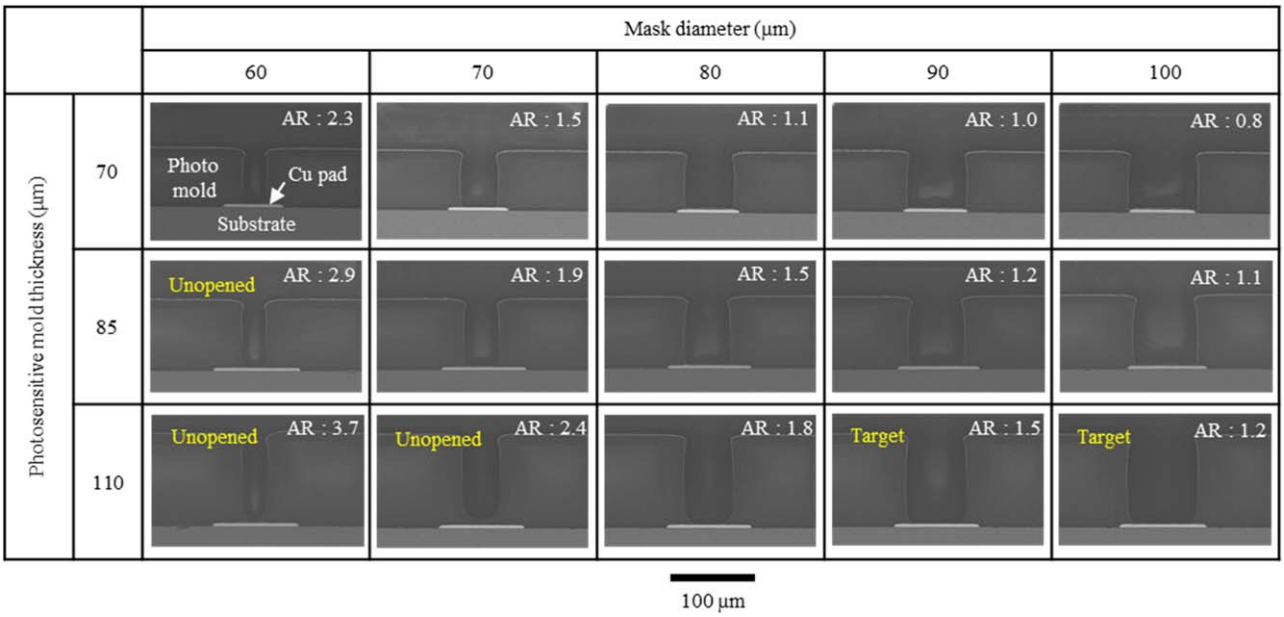

Fig. 8. (Color online) Evaluation of the dependence of the deep via opening on the photosensitive mold thickness and mask diameter.

deposition (PVD) over the entire surface of the wafer with opened vias as shown in Fig. 6(b). The target thicknesses of the Ti and Cu were 50 nm and 350 nm, respectively. To evaluate the actual thickness of sputtering deposition, the thickness of sputtered Ti layer on the surface and bottom of shallow via and deep via were measured using cross-sectional analysis as shown in Fig. 9. The thicknesses of the surface at the shallow via and deep via were the same, 45 nm, whereas the thickness of the bottom of the deep via was thinner than that of the bottom of the shallow via. The thickness of the bottom of the shallow via was 35 nm, and that of the bottom of the deep via was 20 nm as shown in Fig. 10. It was found that the deeper the via, the thinner the thickness of sputtering deposition at the bottom of the via. It indicates that controlling the sputtering deposition thickness at the bottom of deep via is important for achieving the robust Cu interconnection, in the case of sputtering deposition using PVD on a wafer with different via depths.

The proposed RDL process achieves low cost and high productivity by combining the photosensitive mold and Cu conformal electroplating. However, it is difficult to achieve high density interconnect because stacked vias cannot be applied in the case of using Cu conformal electroplating. To achieve further high density interconnect, it may be necessary to introduce Cu filling electroplating or CMP process in RDL formation.

4. Results and discussion

4.1. Prototype package

The specifications of the prototype package are shown in Table II and a top view of the package is shown in Fig. 11. The size of the package is 15 mm × 15 mm and the size of the embedded test die is 10 mm × 10 mm. The developed prototype package is based on the fabrication process described in Sect. 3. Figure 12 shows a photograph of the embedded die edge. A die is embedded face-up in the photosensitive mold. RDL interconnects the deep via on the substrate with the shallow via on the embedded die. There is no significant step gap at the edge of the die. The gap in

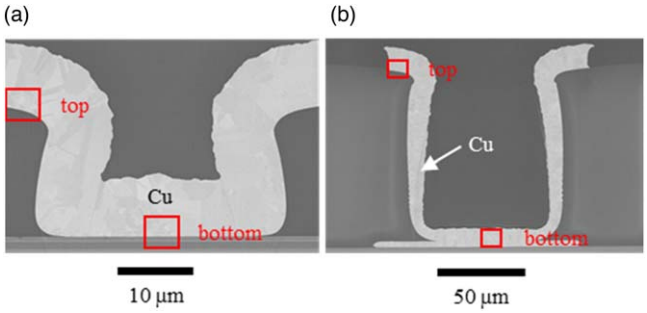

Fig. 9. (Color online) Measurement point of the thickness of sputtered Ti layer. (a) Cross section of shallow via. (b) Cross section of deep via.

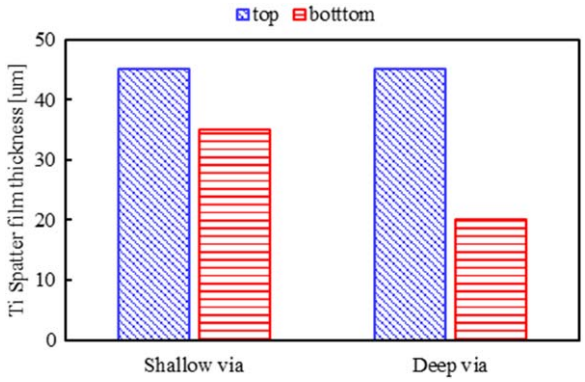

Fig. 10. (Color online) Thickness Measurement of the Ti sputter layer of shallow via and deep via.

Table II. Package specification.

Die	Size (mm)		10 × 10
	Thickness (μm)		100 (including DAF)
Package	Size (mm)		15 × 15
	Thickness (μm)		835
Via	Shallow	Pad count	2116
		Pad pitch (μm)	200
	Deep	Pad count	768
		Pad pitch (μm)	300

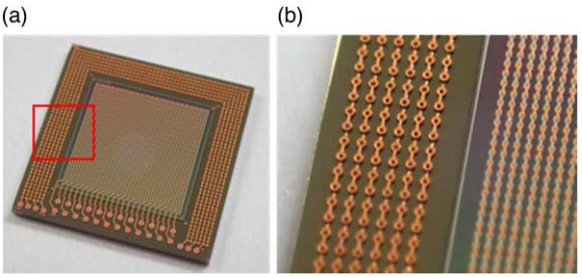

Fig. 11. (Color online) Photograph of the developed prototype package.

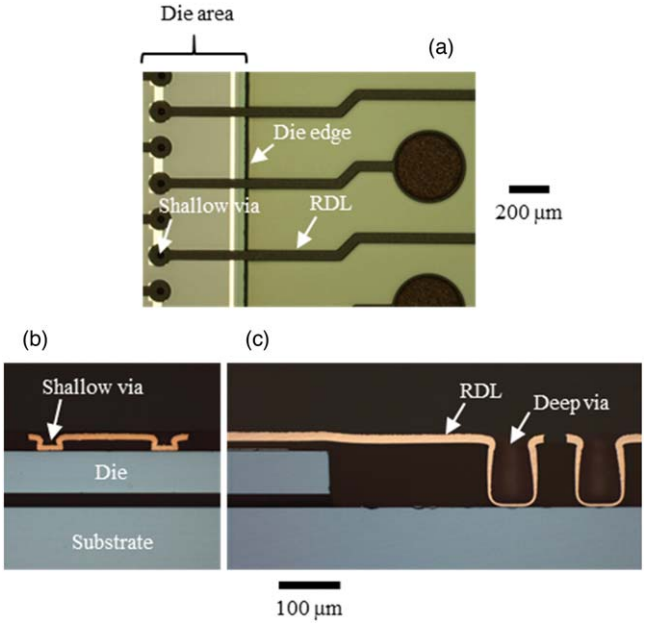

Fig. 12. (Color online) Photograph of a developed prototype package. (a) Top view of deep vias. (b) Cross-section of the embedded die edge. (c) Cross-section of deep vias.

this process is less than 5 μm. The void-free gap filling and flat surface are confirmed after film formation. Formation of the shallow via openings with height of 10 μm and top diameter of 35 μm is confirmed. And formation of the deep via openings with height of 110 μm, top diameter of 80 μm, and AP of 1.4 is confirmed. The deep vias can be placed with a 150 μm pitch. Compared with the conventional Cu pillar process, the 3D integration can provide higher pin counts. Deep vias can be placed at 100 μm from the die edge, significantly minimizing the keep-out zone for through-mold via layout to accommodate smaller package sizes and more pins in 3D stacked devices. The X-ray image of the prototype package is shown in Fig. 13. It can be seen that the shallow via and the deep via are properly fabricated with RDL.

4.2. Package reliability

Reliability assessment of the developed packages was performed. Daisy chains connecting over 2000 vias with 200 μm pitch on the die and over 700 vias with 300 μm pitch on the substrate were checked to measure their electrical resistance. Before the test, all package samples are rated at moisture sensitivity level-3 conditions (MSL 3) as shown in Table III. A 1000-cycle package-level thermal cycle test (TCT), a 1000 h high-temperature storage test (HTS), and a 96 h pressure cooker test (PCT) were performed as shown in Table IV.

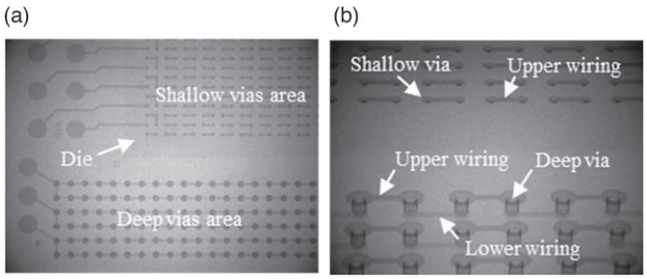

Fig. 13. (Color online) X-ray images of a developed prototype package. (a) Top view. (b) Bird's-eye view.

Table III. Pre-treatment conditions.

#	Pre-treatment	Test condition
1	Pre-bake	125 °C for 10 h
2	Moisture absorption	30 °C, 70%RH for 7 d
3	Reflow	Max. 260 °C, 3 times

Physical properties of electroplated Cu vary drastically depending on its micro-texture. EBSD was employed to characterize the orientation of grains, grain size distribution, and strain mapping of the Cu films before and after 1000 thermal cycles. EBSD measurements were performed at incident beam energy of 15 kV and specimen tilt of 60°. Orientation mapping was done over a 75 μm × 35 μm area. Grain boundaries were defined by a minimum of 5° orientation change from one grain to contiguous ones. 1000-cycle package-level TCT confirmed that tiny cracks occurred at the top edge of the shallow via openings in Fig. 14(d). Residual stress around the crack was confirmed from grain reference orientation deviation in Fig. 4(e). It was also revealed, as shown in Fig. 15, that the grain size after the 1000 thermal cycles was enlarged compared with that before the thermal cycling, which causes tiny cracks along the grain boundaries. On the other hand, as shown in Fig. 14(f), the crystal orientation distribution after the 1000 thermal cycles remained unchanged from those before the thermal cycling. This means that the microstructures of the interconnection after 1000 thermal cycles had no texture during recrystallization generated by thermal stress. The failure criterion for the reliability test was defined as the electrical resistance of the daisy chain within ±10% from the initial value. The prototype package with photosensitive through mold interconnects passed a 1000-cycle package-level TCT, a 1000 h high-temperature storage test, and a 96 h PCT. In harsh testing environments, RDL cracking may become an issue. The material developed in this study has a higher CTE and a lower modulus of elasticity compared to traditional mold materials. In future material development, further reduction of CTE will be an important issue in order to reduce concerns about reliability.

Table IV. Package-level reliability test.

Test item (test condition)	End point
Temperature cycling/TC (−55 °C/125°C)	1000 cycles
High temperature storage/HTS (150 °C)	1000 h
Pressure cooker test/PCT (121 °C/100% RH)	96 h

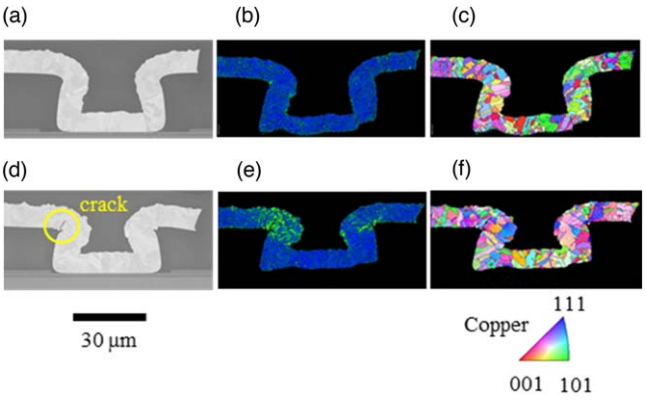

Fig. 14. (Color online) SEM image, orientation image (normal direction) and GROD maps of shallow via. (a)–(c) Initial, (d)–(f) after 1000 thermal cycles.

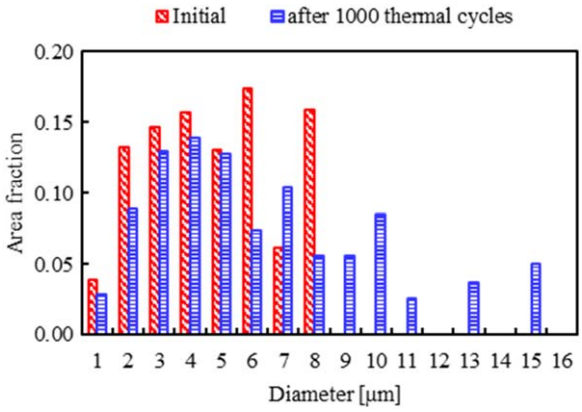

Fig. 15. (Color online) Comparison of grain size change of shallow via before and after 1000-cycle package-level thermal cycle test.

5. Conclusions

3D packaging and integration using photosensitive mold is promising technology to reduce costs and improve productivity for future heterogeneous integration. By applying a mold material with characteristics such as photo via opening, low viscosity, filler-less, thick, and film shape to fan-out package, an innovative 3D integration with high design flexibility can be expected. We have confirmed the feasibility of the 3D integration packaging process and evaluated the package reliability assessment for photo vias with different diameters and depths. Reliability assessment results for the 3D package samples have confirmed that no failures are observed after a 1000-cycle package-level TCT, a 1000 h HTS test, and a 96 h PCT. After a 1000-cycle TCT, EBSD analysis was adopted to analyze the thermal stress and crystal orientation distribution on the Cu RDL. The developed package using photosensitive mold showed high reliability and the possibility of applying it as a future 3D package for integration was confirmed.

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1) M. Brunnbauer, E. Fgut, G. Beer, and T. Meyer, Proc. 8th Electronic Packaging Technology Conf., 2006, p. 1.
2) X. Fan and Q. Han, Proc. 10th Electronic Packaging Technology Conf., 2008, p. 834.
3) Y. Jin, X. Baraton, S. W. Yoon, Y. Lin, P. C. Marimuthu, V. P. Ganesh, T. Meyer, and A. Bahr, Proc. 12th Electronic Packaging Technology Conf., 2010, p. 520.
4) J. H. Lau et al., IEEE Trans. Compon., Packag. Manuf. Technol. **8**, 991 (2018).
5) J. H. Lau et al., IEEE Trans. Compon., Packag. Manuf. Technol. **8**, 1544 (2018).
6) T. Fukushima, A. Alam, A. Hanna, S. C. Jangam, A. A. Bajwa, and S. S. Iyer, IEEE Trans. Compon., Packag. Manuf. Technol. **8**, 1738 (2018).
7) M. Wojnowski, G. Sommer, K. Pressel, and G. Beer, Proc. 63th Electronic Components and Technology Conf., 2013, p. 2121.
8) A. Cardoso, L. Dias, E. Fernandes, A. Martins, A. Janeiro, P. Cardoso, and H. Barros, Proc. 67th Electronic Components and Technology Conf., 2017, p. 14.
9) F.-C. Hsu, J. Lin, S.-M. Chen, P.-Y. Lin, J. Fang, J.-H. Wang, and S.-P. Jeng, Proc. 68th Electronic Components and Technology Conf., 2018, p. 337.
10) S. Ma, J. Wang, F. Zhen, Z. Xiao, T. Wang, and D. Yu, Proc. 68th Electronic Components and Technology Conf., 2018, p. 1493.
11) S. C. Chong, D. H. S. Wee, V. S. Rao, and N. S. Vasarla, IEEE Trans. Compon., Packag. Manuf. Technol. **3**, 1654 (2013).
12) W. M. Ki, W. G. Lee, I. B. Lee, I. S. Mok, W. C. Do, M. Kolbehdari, A. Copia, S. Jayaraman, C. Zwenger, and K. W. Lee, Proc. 68th Electronic Components and Technology Conf., 2018, p. 580.
13) C.-F. Tseng, C.-S. Liu, C.-H. Wu, and D. Yu, Proc. 66th Electronic Components and Technology Conf., 2016, p. 1.
14) C. H. Khong, A. Kumar, X. Zhang, G. Sharma, S. R. Vempati, K. Vaidyanathan, J. H.-S. Lau, and D.-L. Kwong, Proc. 59th Electronic Components and Technology Conf., 2009, p. 1289.
15) V. Carias, J. Thompson, P. D. Myers Jr., P. Kumar, L. M. Racz, R. Toomey, and J. Wang, IEEE Trans. Compon., Packag. Manuf. Technol. **5**, 921 (2015).
16) A. Kumar, X. Dingwei, V. N. Sekhar, S. Lim, C. Keng, G. Sharma, V. S. Rao, V. Kripesh, J. H. Lau, and D.-L. Kwong, Proc. 59th Electronic Components and Technology Conf., 2009, p. 535.
17) R. Zoberbier, J. Welsh, C. Ohde Dr., and H. Huebner, Proc. 67th Electronic Components and Technology Conf., 2017, p. 1767.
18) J. A. M. Plomantes, R. A. D. Mamangun, A. T. Clarina Jr., and R. J. L. Guevara, 20th Electronic Packaging Technology Conf., 2018, p. 514.
19) T. Braun et al., Proc. 61th Electronic Components and Technology Conf., 2011, p. 48.
20) V. S. Rao, C. T. Chong, D. Ho, D. M. Zhi, C. S. Choong, P. S. Sharon Lim, D. Ismael, and Y. Y. Liang, Proc. 66th Electronic Components and Technology Conf., 2016, p. 1522.
21) S. W. Ho, L. C. Wai, S. A. Sek, D. I. Cereno, B. L. Lau, H.-Y. Hsiao, T. C. Chai, and V. S. Rao, Proc. 18th Electronic Packaging Technology Conf., 2016, p. 51.
22) S. P.-S. LIM, S. C. Chong, M. Z. Ding, and V. S. Rao, Proc. 18th Electronic Packaging Technology Conf., 2016, p. 435.
23) I. Qin, O. Yauw, G. Schulze, A. Shah, B. Chylak, and N. Wong, Proc. 67th Electronic Components and Technology Conf., 2017, p. 1309.
24) H. Hsiang-Yao, S. W. Ho, S. S. B. Lim, W. L. Ching, C. S. Choong, S. L. P. Siang, H. Yong, and C. T. Chong, Proc. 69th Electronic Components and Technology Conf., 2019, p. 21.
25) K. Jinseong et al., Proc. 58th Electronic Components and Technology Conf., 2008, p. 1089.
26) J. Hunt, Y. C. Ding, A. Hsieh, J. Chen, and D. Huang, Proc. 4th Electronic System-Integration Technology Conf., 2012.
27) V. S. Rao, C. T. Chong, D. Ho, D. M. Zhi, C. S. Choong, P. S. Sharon Lim, D. Ismael, and Y. Y. Liang, Proc. 67th Electronic Components and Technology Conf., 2017, p. 615.
28) V. N. Sekhar, D. I. Cereno, D. Ho, and V. S. Rao, Proc. 20th Electronic Packaging Technology Conf., 2018.

29) K. Mori, S. Yamashita, T. Fukuda, M. Sekiguchi, H. Ezawa, and S. Akejima, Proc. 69th Electronic Components and Technology Conf., 2019, p. 1140.
30) K. Mori, S. Yamashita, and M. Sekiguchi, Extended Abstracts of the 2020 Int. Conf. on Solid State Device and Materials, C-2-03, 2020, p. 131.
31) T. Braun, K.-F. Becker, S. Voges, T. Thomas, R. Kahle, J. Bauer, R. Aschenbrenner, and K.-D. Lang, Proc. 63th Electronic Components and Technology Conf., 2013, p. 1235.
32) T. Braun, K.-F. Becker, M. Wöhrmann, M. Töpper, L. Böttcher, R. Aschenbrenner, and K.-D. Lang, Proc. Int. Conf. on Electronics Packaging, 2017, p. 325.
33) F. Hou, T. Lin, L. Cao, F. Liu, J. Li, X. Fan, and G. Q. Zhang, IEEE Trans. Compon., Packag. Manuf. Technol. **7**, 1721 (2017).
34) F.-L. Schein, R. Kahle, M. Kunz, T. Kunz, J. Kossev, T. Müller, M. Pentz, M. Dietterle, and A. Ostmann, IEEE Trans. Compon., Packag. Manuf. Technol. **10**, 5 (2020).