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Analysis of dependence of dV_{CE}/dt on turn-off characteristics with a 1200 V double-gate insulated gate bipolar transistor

Yoko Iwakaji[1*], Tomoko Matsudai[1], Tatsunori Sakano[2], and Kazuto Takao[2]

[1]*Toshiba Electric Devices & Storage Corporation, Kawasaki, Kanagawa 212-8520, Japan*
[2]*Corporate Research & Development Center, Toshiba Corporation, Kawasaki, Kanagawa 212-8582, Japan*

[*]E-mail: yoko.iwakaji@toshiba.co.jp

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The double-gate drive is a remarkable gate control technique for dramatically reducing turn-off loss in Si-insulated gate bipolar transistors (IGBT) by increasing dV_{CE}/dt. However, no detailed analysis of the difference of turn-off mechanism according to the difference in dV_{CE}/dt between double-gate drive and conventional gate drive has been reported. The double-gate (DG) drive allows the dV_{CE}/dt of IGBTs to increase beyond the maximum dV_{CE}/dt of 7000 V μs^{-1} in conventional gate drives. Furthermore, the influence of relations between gate-drive timings and dV_{CE}/dt on turn-off operations were confirmed in the case of three different DG IGBT structures.

1. Introduction

The main stream of development of Si-insulated gate bipolar transistor (IGBT) chip technology is improvement of the trade-off between conduction losses and switching losses.[1,2] The non-latch-up IGBT was proposed in 1984,[3] and since then the trade-off has been improved by such innovations, as trench-gate structures,[4] non punch through-structure,[5] field-stop technology,[6,7] injection enhanced gate transistor[8] and carrier stored trench-gate bipolar transistor.[9] These innovations enabled the current density increase, which is the key to chip miniaturization.

However, the limits of silicon have recently made it increasingly difficult to improve the performance of Si-IGBTs through modification of device structures alone. Gate-control techniques have therefore attracted attention as a means of reducing energy loss throughout the system, including IGBTs and fast-recovery diodes[10–19] or gate-drive circuits.[20–25] Double-gate (DG) IGBT technology is one such gate-control technique.[26–29] Energy loss can be reduced by using a device with two gates controlled at different timings. According to these reports, increasing dV_{CE}/dt during turn-off reduces turn-off loss. We have reported the dependence of dV_{CE}/dt on turn-off operations in the case of a fabricated DG IGBT.[30] In this paper, we additionally discuss the influence of relations between gate-drive timings and dV_{CE}/dt on turn-off operations in the case of different DG IGBT structures.

2. Experimental methods

We fabricated 1200 V, 100 A DG IGBTs (Fig. 1) having two gates—a main gate (MG) and a control gate (CG)—connected to separate gate pads. All dummy trenches and all n^+ emitter layers are connected to the emitter electrodes. Type A is the structure having a dummy trench between MG and CG [Fig. 1(a)]. Type B is the structure having three dummy trenches between MG and CG [Fig. 1(b)]. Type C is the structure having a dummy trench between MG and CG, and n^+ emitter layer is not formed at the side of CG trench [Fig. 1(c)]. Therefore, electron injection cannot be carried out even if a plus voltage is applied to the CG pad.

Figure 2 shows the timing chart of the gate drive during turn-off, and Fig. 3 shows a conceptual diagram of carrier movement during turn-off switching.

[Period 1] Period 1 is the conducting state. V_{MGE} and V_{CGE} (voltage from the emitter to MG and CG) are 15 V. N channel is formed at the surface of p base layer along MG and CG, and electron is injected into n^- base layer through n channel.

[Period 2] When –15 V is applied to CG, the n channel formed along the CG disappears and a p channel is formed. Holes can then be easily drained through the p channel, regardless of the MG state (n channel is formed or not). Further, the amount of stored carrier near the emitter side of the n-base layer becomes smaller. Therefore, V_{CE} becomes a little higher than that of Period 1. The duration of Period 2 is called the "gate delay time" (DT). In the case of DT 0 μs, the MG and CG are simultaneously turned off. In this mode, the operation of the DG IGBT is the same as that of a conventional IGBT having one gate.

[Period 3] Turn-off behavior of IGBT starts when −15 V is applied to MG. The n channel along MG also disappears and electron injection from n^+ emitter layer stops. Because the amount of carriers in the n^- base layer decreased in Period 2 and p channel along CG enhances hole drain, the depletion region formed in the n^- base layer extends rapidly in Period 3. This causes dV_{CE}/dt to increase and the turn-off time to shorten.

We performed switching measurements using the fabricated DG IGBTs. All measurements described below were performed at room temperature with a 600 V supply voltage (V_{CC}). Turn-off dV_{CE}/dt is defined as the rate of increase in V_{CE} from 50% to 90% of V_{CC}.

3. Results and discussion

3.1. Dependence of dV_{CE}/dt with type A

We confirmed gate resistance (R_G) dependence of turn-off characteristics by varying R_G from 3.9 to 82 Ω. Figure 4 shows the relations between DT and turn-off losses at R_G 3.9 Ω, 33 Ω and 82 Ω with type A structure. When R_G is 3.9 Ω, turn-off losses decrease as DT increases, and turn-off losses are almost constant when DT is over 5 μs. This is because it takes time for stored carriers in the n^- base layer to drain because of the slow carrier mobility and electron injection and hole drain balance over 5 μs. The reduction ratio of turn-off loss using the DG drive to that when DT is 0 μs (equivalent to conventional IGBT) is 27%, as in previous reports.[27,28] However, turn-off losses do not decrease at higher R_G. Though dV_{CE}/dt increasing is observed at R_G 3.9 Ω, it is not observed at R_G 33 Ω and 82 Ω.

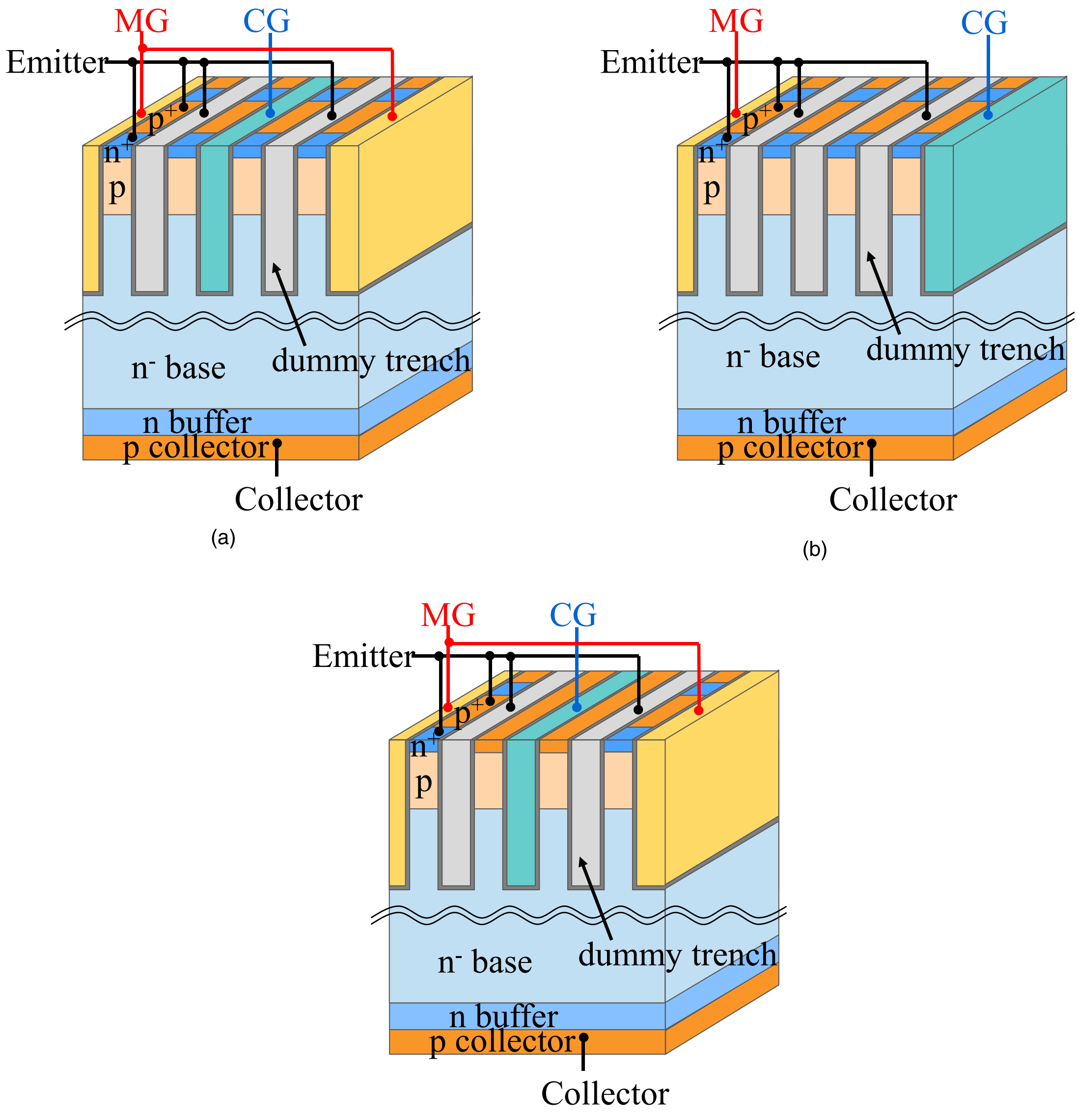


Fig. 1. (Color online) Double-gate IGBT structures (a) Type A, (b) Type B, (c) Type C.

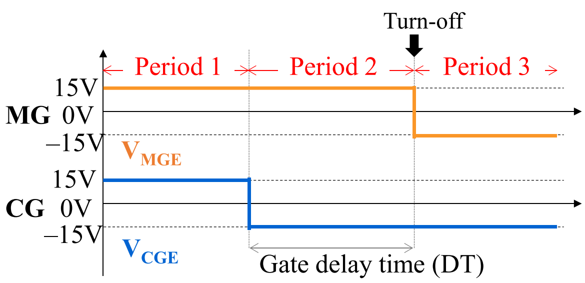


Fig. 2. (Color online) Gate-drive method during turn-off switching.

Figure 5 shows the measured relations between R_G and dV_{CE}/dt, and Fig. 6 shows the measured relations between dV_{CE}/dt and turn-off loss at DT 0 μs and 5 μs. Figure 7 shows the measured waveforms at DT 0 and 5 μs. In that figure, V_{MGE} is 13.5 V (the V_{MGE} drops below 90% of 15 V) at 100 ns on the time axis. As R_G decreases, the value of dV_{CE}/dt slightly increases, peaking at about 7000 V μs^{-1} in the case of DT 0 μs as shown in Fig. 5. In the case of DT 0 μs, shorter turn-off delay time (the time from when the V_{MGE} drops below 90% of 15 V until the V_{CE} reaches 10% of V_{CC}) is observed at R_G 3.9 Ω, as shown in Fig. 7(a). dV_{CE}/dt increasing in comparison with that when R_G is 33 Ω is not observed. In Fig. 5, in contrast, dV_{CE}/dt can increase to about 12 000 V μs^{-1} at DT 5 μs, as RG decreases. This increase in dV_{CE}/dt causes turn-off loss to decrease. However, compared with the case where dV_{CE}/dt is less than 7000 V μs^{-1}, higher turn-off loss is observed at DT 5 μs as shown in Fig. 6.

Then, we compared turn-off waveforms at R_G 3.9 Ω, 33 Ω and 82 Ω to explore the difference between turn-off behaviors of DG drive and conventional drive (DT is 0 μs). Figure 8 shows turn-off waveforms when R_G is 3.9 Ω. Shorter turn-off delay time and higher dV_{CE}/dt are observed at DT 5 μs than at DT 0 μs. The expected effect of turn-off loss reduction by using a DG drive is observed. At both DT 0 μs and 5 μs, V_{CE} increases occur after the Miller period. This is because it takes time after electron injection stops before the extension of the depletion region starts because of the slow carrier mobility. Because the amount of carriers in the n^- base layer decreased in Period 2, the depletion region extends rapidly using DG drive regardless of the slow carrier mobility.

Figure 9 shows turn-off waveforms when R_G is 33 Ω. In this figure, V_{CE} is 500 V at 0 ns on the time axis for

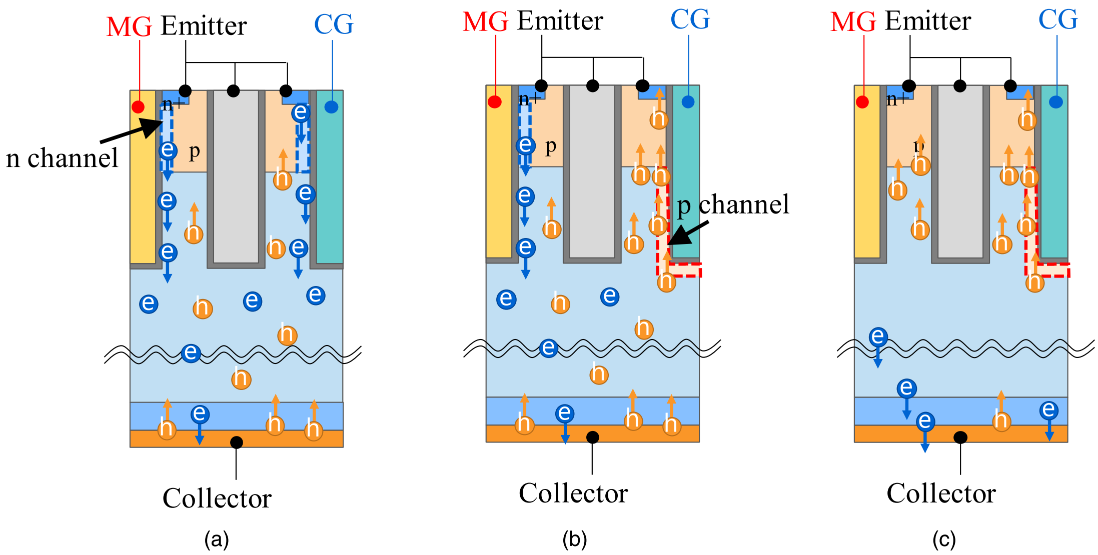


Fig. 3. (Color online) Conceptual diagram during turn-off switching with type A (a) Period 1, (b) Period 2, (c) Period 3.

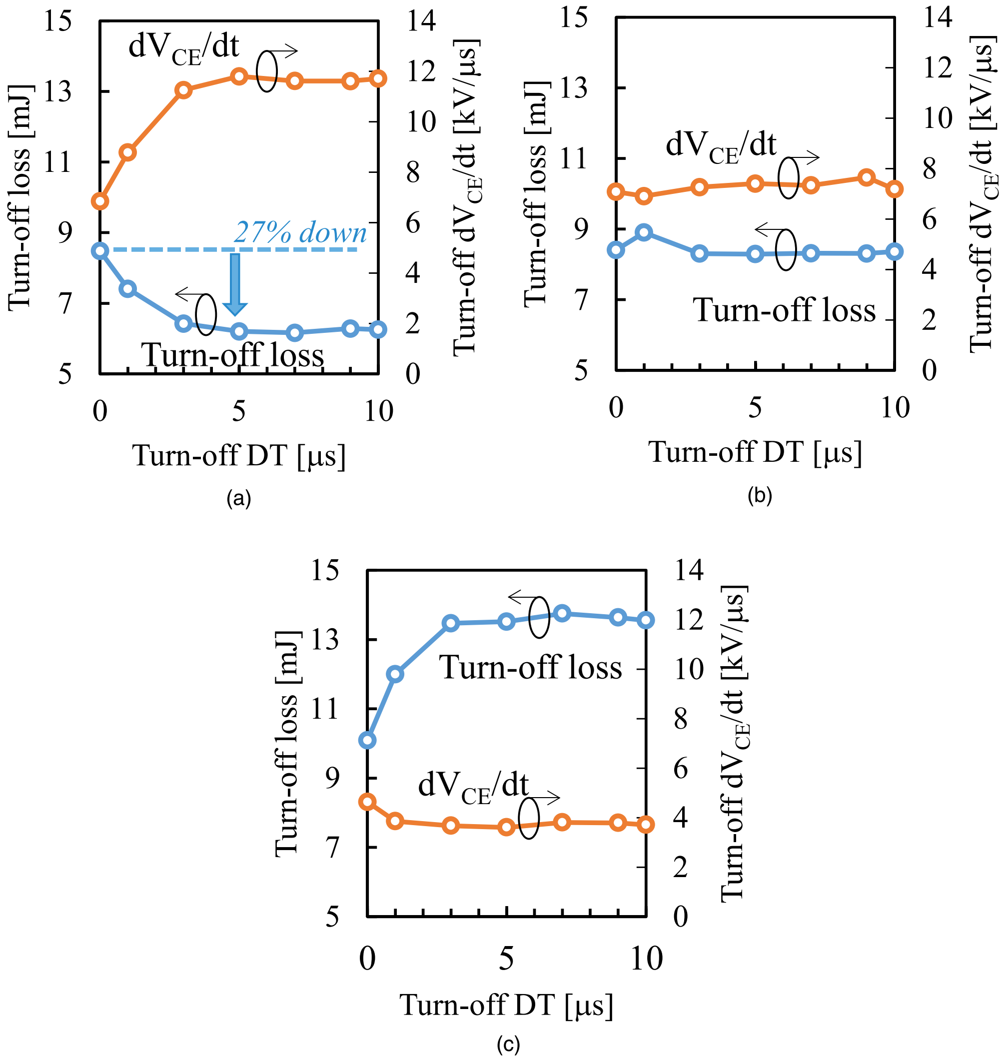


Fig. 4. (Color online) Measured DT dependence of turn-off losses with type A (a) $R_G = 3.9\ \Omega$, (b) $R_G = 33\ \Omega$, (c) $R_G = 82\ \Omega$.

comparison of dV_{CE}/dt. In the case of DT 5 μs, step-up of V_{CE} is observed in a range of <300 V. However, the collector current I_C decreases more rapidly than at DT 0 μs, because of the rapid hole drain through the p channel along the CG. As a result, turn-off losses at DT 0 μs and 5 μs are nearly equal (8.4 and 8.3 mJ, respectively).

We performed a TCAD simulation to analyze the phenomenon of V_{CE} step-up at low voltage. Figure 10 shows the

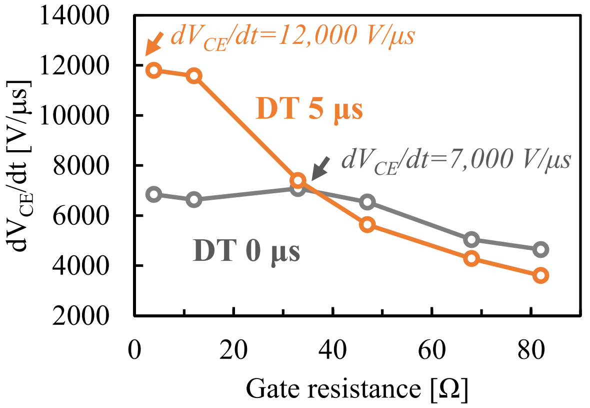


Fig. 5. (Color online) Measured relations between gate resistance and dV_{CE}/dt with type A.

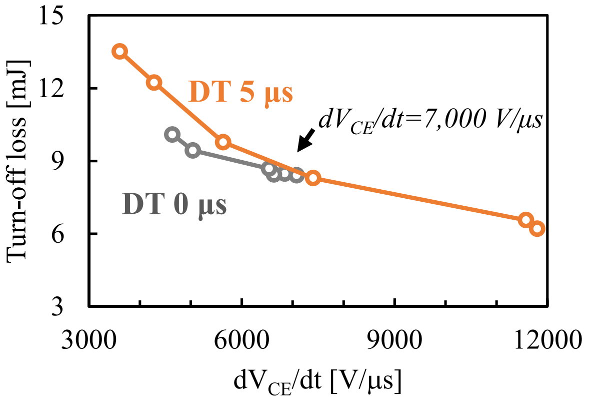


Fig. 6. (Color online) Measured relations between dV_{CE}/dt and turn-off loss with type A.

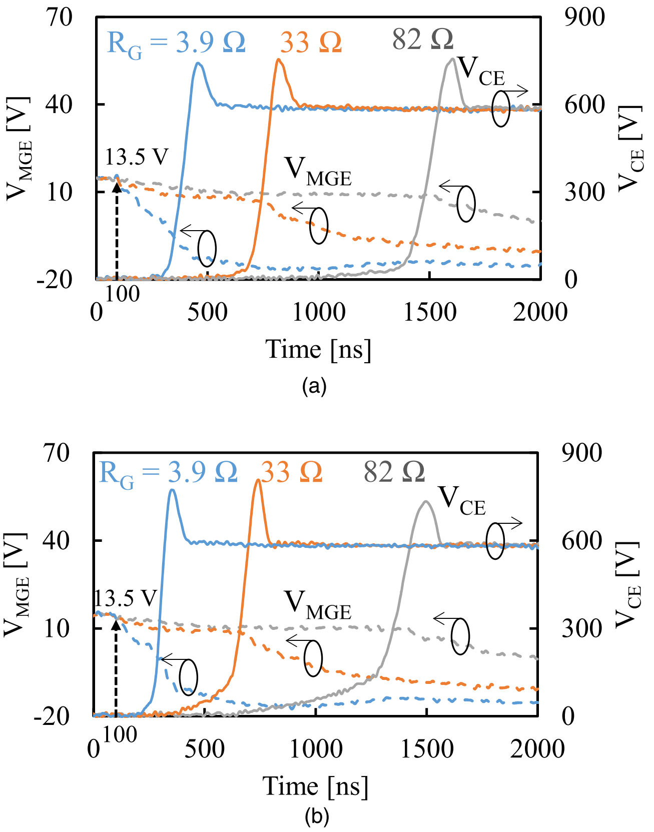


Fig. 7. (Color online) Measured turn-off waveforms at DT 0 μs and 5 μs (a) DT 0 μs, (b) DT 5 μs.

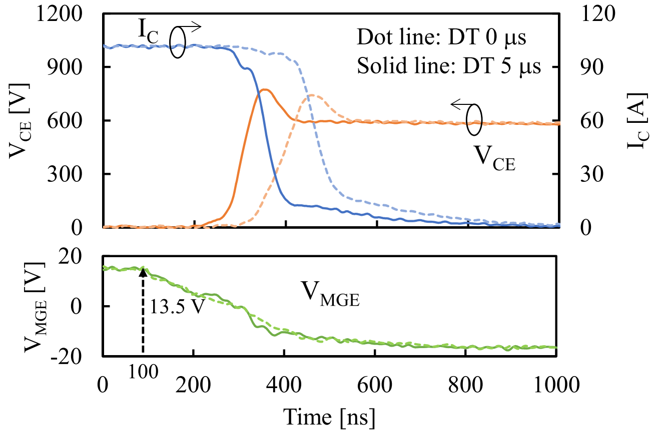


Fig. 8. (Color online) Measured turn-off waveforms at $R_G = 3.9\ \Omega$ with type A.

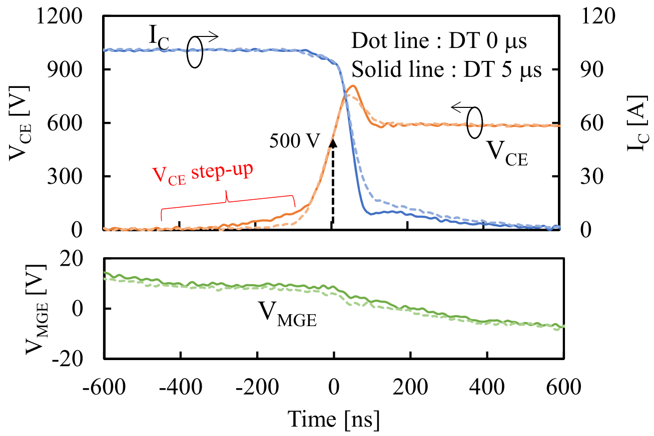


Fig. 9. (Color online) Measured turn-off waveforms at $R_G = 33\ \Omega$ with type A.

simulated turn-off waveforms when R_G is 33 Ω at DT 0 and 5 μs. Figure 11 shows hole densities at 0, −50, −100, −150, and −200 ns. In the case of DG drive at DT 5 μs, the stored carriers rapidly drain near the emitter side surface, mainly near CG with V_{MGE} decreasing. This carrier decreasing causes step-up of V_{CE}. However, during the period V_{MGE} remains constant due to the Miller effect, the n channel along MG does not disappear and electron injection continually occurs. Extension of the depletion region does not occur during this period, and V_{CE} change remains slow. The depletion region extends at almost the same speed at both DT 0 and 5 μs after the Miller period.

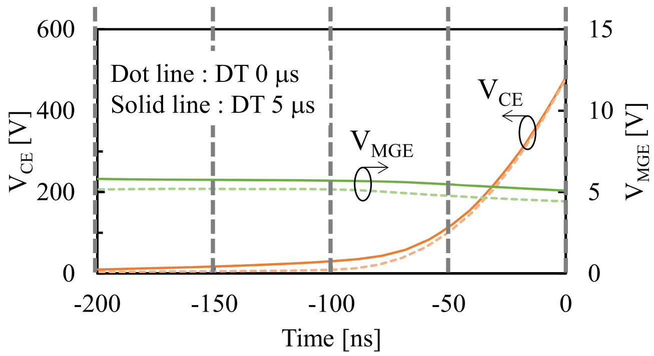
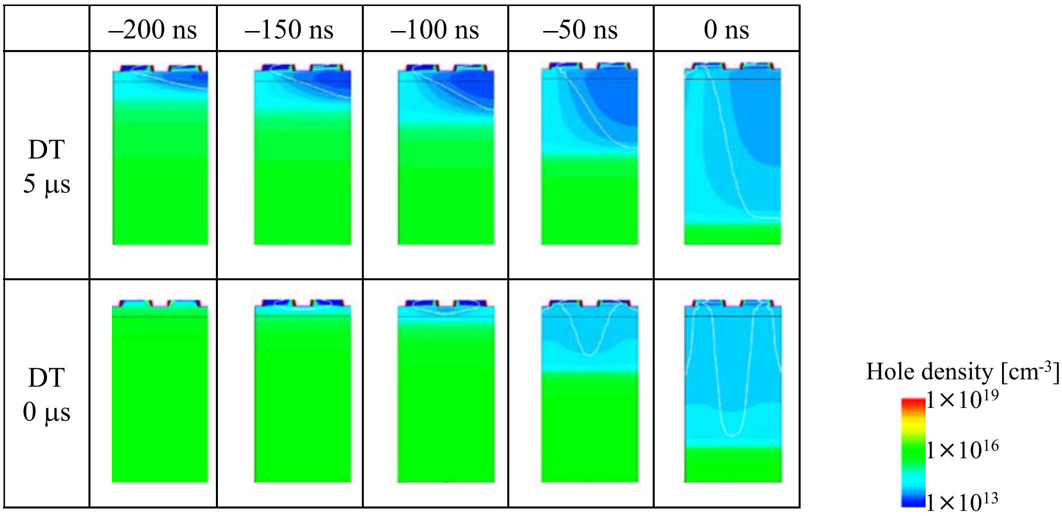
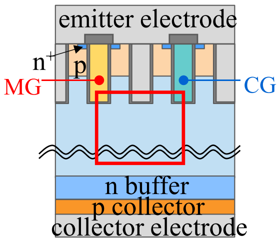


Fig. 10. (Color online) Simulated turn-off waveforms with type A.



(a)



(b)

Fig. 11. (Color online) Simulated hole density with type A (a) time change of hole density, (b) display area (red frame).

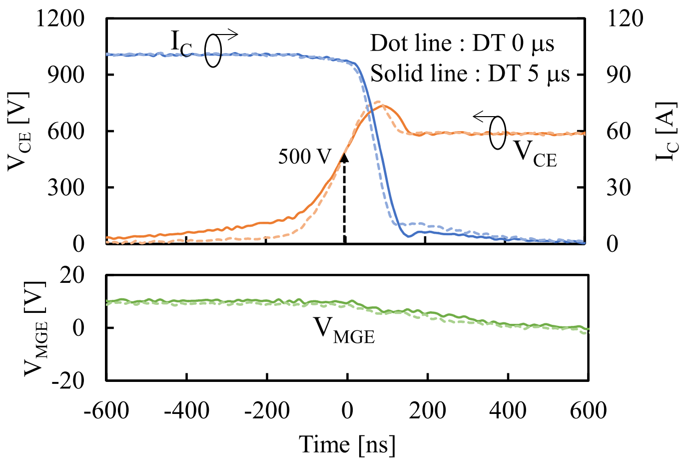


Fig. 12. (Color online) Measured turn-off waveforms at $R_G = 82\ \Omega$ with type A.

Figure 12 shows turn-off waveforms when $R_G = 82\ \Omega$. In the case of DT 5 μs, because change of V_{MGE} is slow towing to higher R_G, longer step-up of V_{CE} is observed than at R_G 33 Ω. This step-up of V_{CE} causes dV_{CE}/dt to decrease and turn-off loss to increase.

Figure 13 shows the measured R_G dependences of dV_{CE}/dt and dI_C/dt characteristics at DT 5 μs. Here, dI_C/dt is defined as the rate of decrease in I_C from 90% to 50%. As R_G decreases from 82 Ω, dV_{CE}/dt and dI_C/dt increase. dV_{CE}/dt increases until $R_G = 3.9\ \Omega$, though dI_C/dt reaches a maximum at 33 Ω. The region over which dV_{CE}/dt increases without increasing dI_C/dt is known as the "semi-controllable region".[31] The IGBT behaves not like expected from MOSFET because of a bipolar device. Hole injection occurs

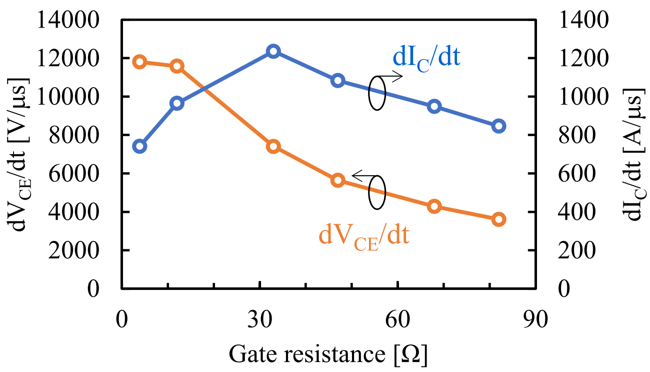


Fig. 13. (Color online) Measured behavior of dI_C/dt and dV_{CE}/dt in turn-off at DT = 5 μs with type A.

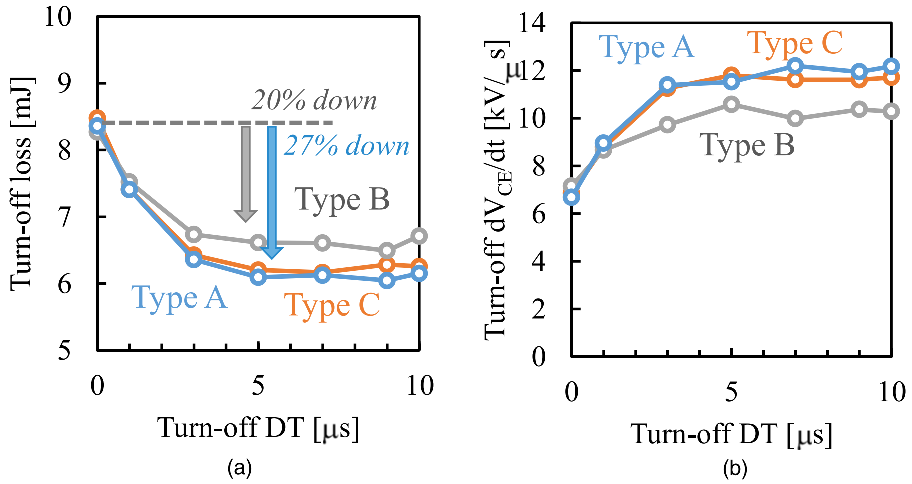


Fig. 14. (Color online) Measured DT dependence of turn-off losses with type A, B and C.

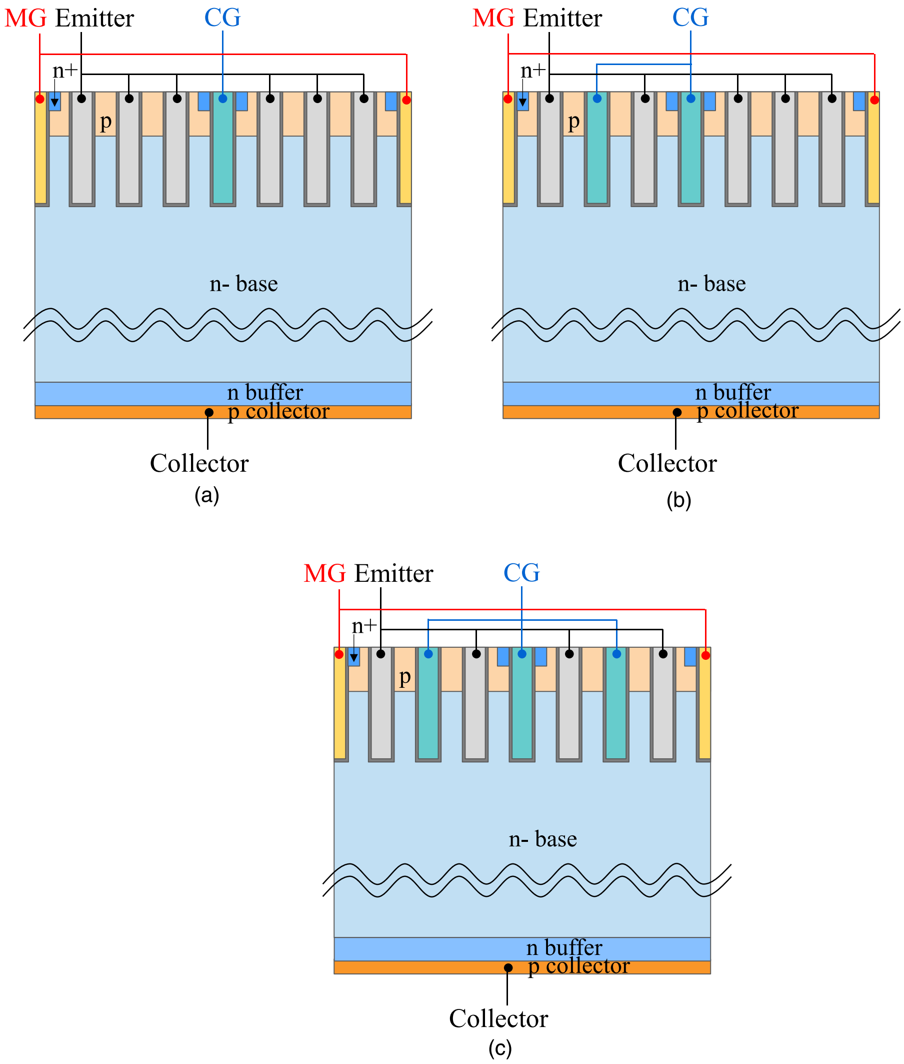


Fig. 15. (Color online) Simulated structures as Type B variations (a) Type B, (b) Type B′, (c) Type B″.

after electrons reach the collector electrode and hole current continuously flows for a while after electron injection stops due to the influence of the slow carrier mobility. As described above, the value of dV_{CE}/dt increases, peaking at about 7000 V μs^{-1} when DT is 0 μs and increases above 12 000 V μs^{-1} at DT 5 μs as R_G decreases, as shown in Fig. 5. We found that dV_{CE}/dt increases of the DG IGBT occur in this semi-controllable region. Further, surge voltage caused by the product of parasitic inductance and dI_C/dt is also suppressed to low levels, despite the high dV_{CE}/dt.

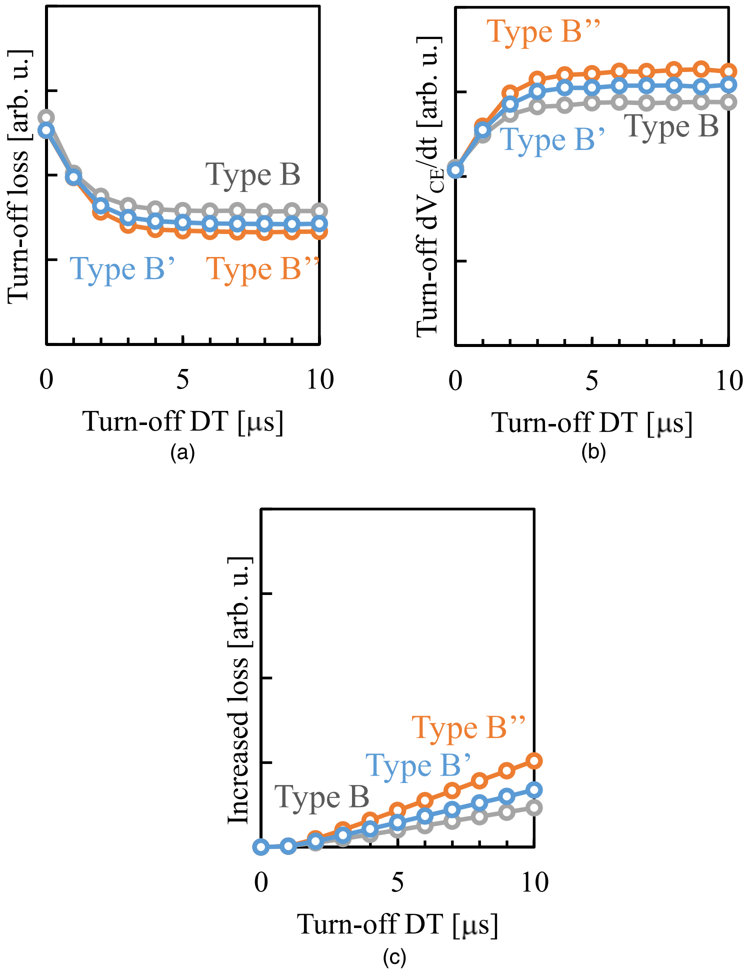


Fig. 16. (Color online) Simulated DT dependence of turn-off losses with type B variations (a) turn-off loss, (b) Turn-off dV_{CE}/dt, (c) Increased loss.

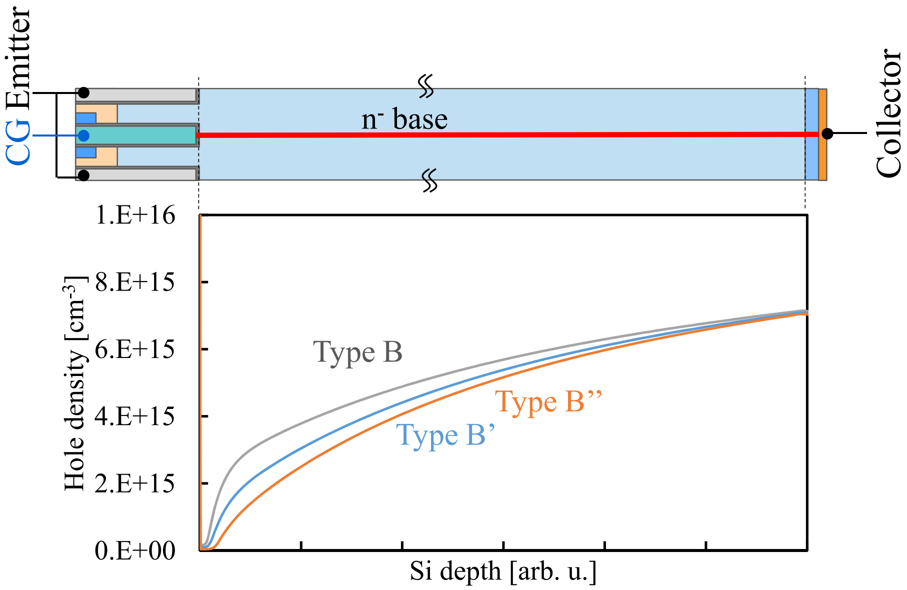


Fig. 17. (Color online) Simulated hole density just before Period 3.

3.2. Comparison between three structures

We performed turn-off measurements using the fabricated DG IGBTs shown in Fig. 1. Figure 14 shows the measured relations between DT and turn-off losses and the relations between DT and turn-off dV_{CE}/dt at R_G 3.9 Ω with type A, type B and type C structures. Type B is the structure having three dummy trenches [Fig. 1(b)]. Type C has the CG without formation of n$^+$ emitter layer [Fig. 1(c)]. With type B, dV_{CE}/dt can increase to about 10 kV μs^{-1} at DT 5 μs. This value is lower than with type A. The reduction ratio of turn-off loss when using the DG drive to that in the case of using a conventional drive is 20% with type B.

We performed TCAD simulations to confirm the relation between the effects of turn-off loss reduction using the DG drive and the number of CGs. The structures used in TCAD simulations are shown in Fig. 15. Type B, type B′ and type B″ have one, two and three CGs in a unit cell, respectively. Figure. 16 shows the simulated relations between DT and turn-off losses and the relations between DT and turn-off dV_{CE}/dt at R_G 3.9 Ω with the structures shown in Fig. 15. Turn-off losses are lower in the case of a structure having a larger number of CGs as shown in Fig. 16(a). These results are caused by higher dV_{CE}/dt as shown in Fig. 16(b).

Figure 17 shows simulated hole density just before Period 3 with the structures shown in Fig. 15. The stored carriers decrease near the emitter side surface of n^- base layer is observed and carriers decrease is more remarkable with a structure having a larger number of CGs. This is because more holes drain with a structure having a larger number of CGs. However, carrier decrease near the emitter side causes V_{CE} to increase at Period 2 and conduction loss to increase. This increased conduction loss is shown in Fig. 16(c).

With type C, dV_{CE}/dt can increase to about 12 000 V μs^{-1} at DT 5 μs as shown in Fig. 14(b). This value is nearly equal to the value of type A. These results suggest that DG drive can cause dV_{CE}/dt to increase and reduce turn-off loss regardless of whether the structure has n^+ emitter layer or not at the side of CG trench.

4. Conclusions

We analyzed the dependence of dV_{CE}/dt on turn-off characteristics in a 1200 V DG IGBT. When dV_{CE}/dt is less than the maximum dV_{CE}/dt of a conventional gate drive, using a DG drive increased turn-off loss. The DG drive allowed dV_{CE}/dt of IGBT to increase beyond the maximum dV_{CE}/dt of the conventional gate drive. Increases in dV_{CE}/dt by the DG IGBT occur in the semi-controllable region, whereas increases in dI_C/dt are limited.

We found that turn-off losses are lower in the case of a structure having a larger number of CGs and that DG drive can cause dV_{CE}/dt to increase and reduce turn-off loss regardless of whether the structure has n^+ emitter layer or not at the side of CG trench.

Acknowledgments

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