

3.3 kV all SiC MOSFET module with Schottky barrier diode embedded SiC MOSFET

Hiroshi Kono,¹ Tomohiro Iguchi,¹ Tatsuya Hirakawa,¹ Hiroyuki Irifune,¹ Takahiro Kawano,¹ Masaru Furukawa,¹ Kenya Sano,¹ Masakazu Yamaguchi,¹ Hisashi Suzuki,¹ and Georges Tchouangue²

¹ Toshiba Electronic Devices & Storage Corporation, Japan

² Toshiba Electronics Europe GmbH, Germany

Corresponding author: Hiroshi Kono, hiroshi.kono@toshiba.co.jp

Abstract

A 3.3-kV class third-generation silicon carbide (SiC) metal-oxide-semiconductor field-effect transistor (MOSFET) with an optimized cell structure consisting of a Schottky barrier diode (SBD) embedded in a SiC MOSFET is developed. The developed SiC MOSFET not only suppresses bipolar operation but also achieves 19% lower on-resistance compared with conventional SiC MOSFETs. We also develop a low-inductance package named iXPLV, whose stray inductance is reduced by 40% compared with conventional modules. We measure the switching losses of the developed MOSFET assembled in iXPLV and compare it with the switching loss of a silicon (Si) insulated gate bipolar transistor (IGBT) assembled in a conventional module. The switching loss of the developed module is 60% lower than the conventional Si IGBT with Si PiN diode and 43% lower than the Si IGBT with SiC SBD. We also estimate the effect of these loss reductions on the cooling unit volume, and the developed module is found to achieve a heatsink volume reduction of 40% compared with the module with a Si IGBT with Si PiN diode and 59% compared with the module with a Si IGBT with SiC SBD.

1 Introduction

Silicon carbide (SiC) metal-oxide-semiconductor field effect transistors (MOSFETs) are regarded as a next-generation power switching device for high power and high blocking voltage applications. Degradation of on-resistance of SiC MOSFETs caused by bipolar operation has been an issue for SiC MOSFETs.[1,2] Although several studies have reported reducing the characteristic degradation rate,[3] a fundamental solution for this issue is needed for high-power modules in order to achieve high reliability. Schottky barrier diode (SBD)-embedded MOSFETs can suppress the bipolar operation of the body diode of a MOSFET.[4,5] Toshiba Electronic Devices & Storage Corporation has developed an SBD-embedded MOSFET [5] as a second-generation SiC MOSFET and has started the production of 1.2-kV class SBD-embedded MOSFETs.

In high-voltage and high-power modules, there is demand for even lower power dissipation and higher temperature operation. We therefore developed a new third-generation SiC MOSFET to improve the power loss and the reverse current capacity. A low-loss 3.3-kV class SiC MOSFET

was achieved by optimizing the ratio of SBDs to MOSFETs and optimizing the cell structure.

To take advantage of the performance of SiC chips, modules need to be able to handle high speed and high-temperature operation. For high-speed operation, it is important to reduce the overall stray inductance of the package. We have developed a low-stray-inductance package named iXPLV. For high reliability, we have developed a technology for achieving high temperature operation.

In this paper, we present the characteristics of our third-generation SiC MOSFET assembled in a module and compare it with Si IGBTs.

2 SBD-embedded SiC MOSFET device

Figure 1 shows a schematic cross-sectional diagram of the fabricated 3.3-kV class SBD-embedded SiC MOSFET that is based on a planar gate structure. In addition to optimizing the SBD ratio as reported in our previous study,[5] overall cell structure optimization was also carried out. Figure 2 shows a comparison of I_d - V_d characteristics between the conventional and developed SBD-embedded MOSFETs. The gate voltage and the measurement temperature were

20V/0V and room temperature, respectively. Whereas the specific on-resistance of the conventional MOSFET is $15.5 \text{ m}\Omega\text{cm}^2$, that of the developed MOSFET is $12.4 \text{ m}\Omega\text{cm}^2$. The specific on-resistances have been reduced by 19% while maintaining the same breakdown voltages. The threshold voltage of the device is 3.9 V at 150°C and 3.5 V even at 175°C , which is sufficiently high even at a high temperature. This is an advantageous feature for suppressing undesired parasitic turn-on.

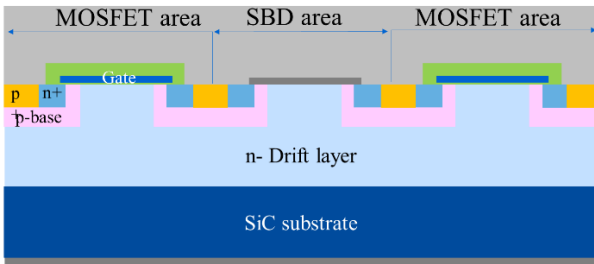
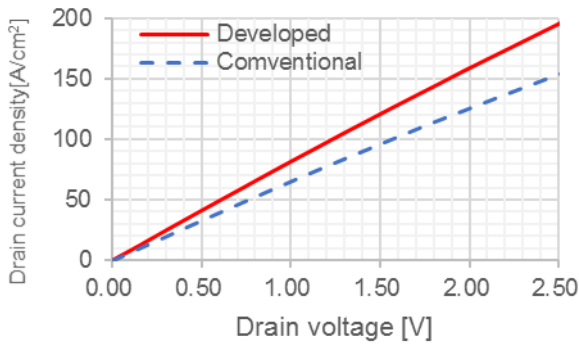
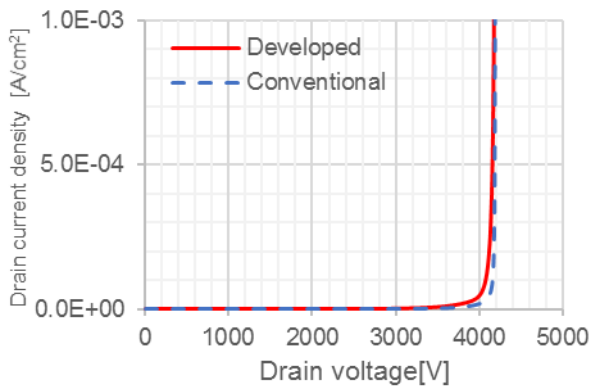


Fig. 1: Schematic cross-sectional diagram of the fabricated SBD-embedded SiC MOSFET.



(a) On state characteristics at room temperature



(b) Off state characteristics at room temperature

Fig. 2: I_d - V_d characteristics of the conventional and developed SBD-embedded SiC MOSFETs when $V_g = 20\text{V}/0\text{V}$ at room temperature.

Figure 3 shows the reverse current characteristics of the conventional and developed MOSFETs when $V_g = -5 \text{ V}$ and the temperature is 175°C . A MOSFET without SBD is also shown for reference. Although the MOSFET without SBD starts bipolar operation at about 2.3 V, the developed device does not start bipolar operation until the current is more than 250 A/cm^2 , even at 175°C .

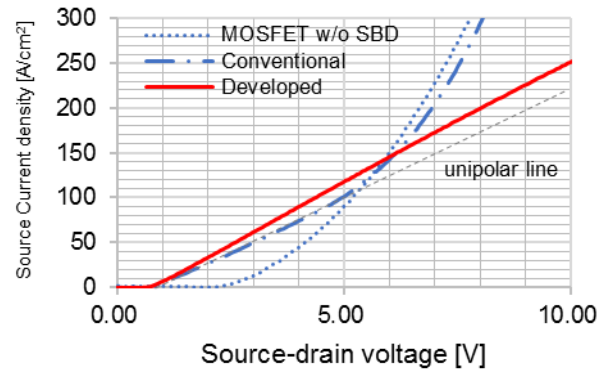


Fig. 3: I_{sd} - V_{sd} characteristics of the MOSFET without SBD, the conventional and the developed SBD-embedded SiC MOSFETs when $V_g = -5 \text{ V}$ at 175°C .

3 Low inductance package iXPLV

In order to reduce the size of a power converter, it is important to reduce the energy consumption and package size of the power module. We have developed a new package platform named iXPLV (Figure 4). The footprint of the iXPLV package is $140 \times 100 \text{ mm}$, which is 23% lower than that of the conventional package ($140 \times 130 \text{ mm}$).

The parasitic inductance inside the module has been reduced by 40% from 20 nH to 12 nH by optimizing the chip layout, wire bonding, Cu pattern on direct bonding copper, terminal shape, and layout.

Figure 5 shows a schematic diagram of the power terminal conductor layout. By placing the P and N terminals close to each other, the mutual inductance is increased and the total inductance between the P and N terminals is reduced.

Figure 6 shows a comparison of the stray inductance between conventional and developed packages; the stray inductance of the iXPLV package is 40% lower than that of the conventional package.

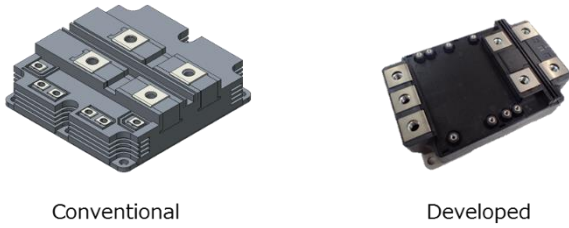


Fig. 4: 3.3-kV, 800-A, 2-in-1 all SiC module (iXPLV) and conventional 3.3-kV 800-A module.

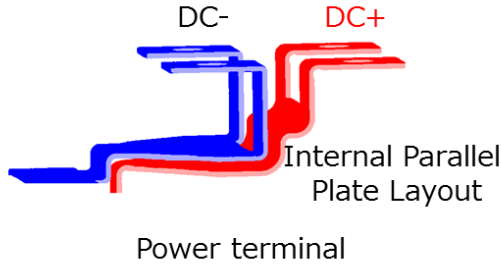


Fig. 5: Internal Cu plate layout for reducing total inductance of the package.

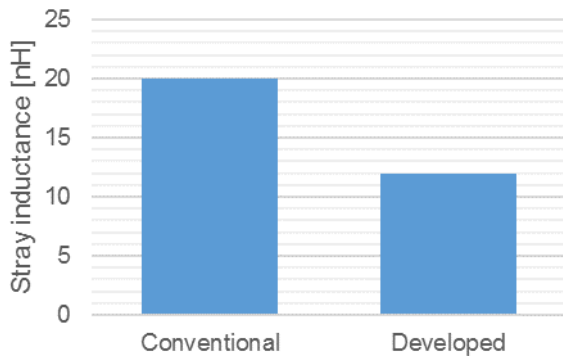


Fig. 6: Comparison of package stray inductance.

In order to improve the power density of the module, it is also important to ensure reliability. We employ a new die bonding technique using Ag-sintering technology to reduce the thermal resistance and improve the power cycling capability.

Figure 7 shows a comparison of cumulative structure functions between the Ag-sintered module and the soldered module. Arrows indicate the thermal resistance of the die-bonding area. The thermal resistance of the Ag-sintered layer is half that of the soldered layer.

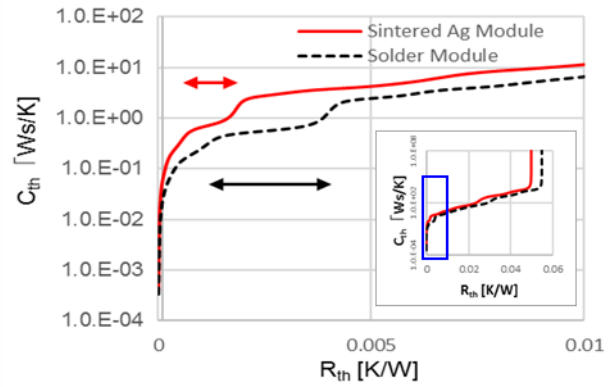


Fig. 7: Comparison of cumulative structure functions between the soldered and Ag-sintered modules.

Figure 8 shows a comparison of the power cycling test between the soldered module and the Ag-sintered module. The input power was set such that T_{vjmax} , ΔT , and t_{on} were $150^{\circ}C$, $90^{\circ}C$, and 2 s, respectively, in the soldered module, and the same input power was applied in both tests. The vertical axis shows the rate of change of V_{ds} . The results are normalized with respect to the lifetime of the solder module, which was defined as the point where the rate of change exceeds 1.05. The lifetime of the Ag-sintered module was two times longer than that of the soldered module. These experimental results demonstrate that the developed module has higher performance and reliability than do conventional modules.

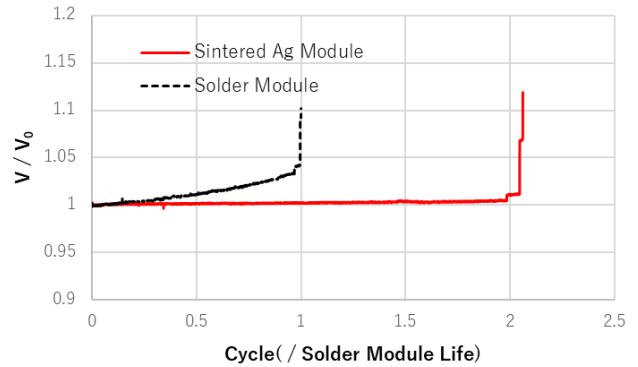


Fig. 8: Comparison of power cycle test between the soldered and Ag-sintered modules.

4 Comparison of device characteristics

Figures 9 and 10 show the forward and reverse characteristics of the iXPLV package with the rated current of 800 A. It can be seen that the developed device does not exhibit any bipolar operation up to

1600 A at 175 °C. The optimized SBD-embedded SiC MOSFET also exhibits low forward voltage drop (V_{dson}) compared with previously reported devices [4,6,7] at room temperature, 150 °C, and 175 °C.

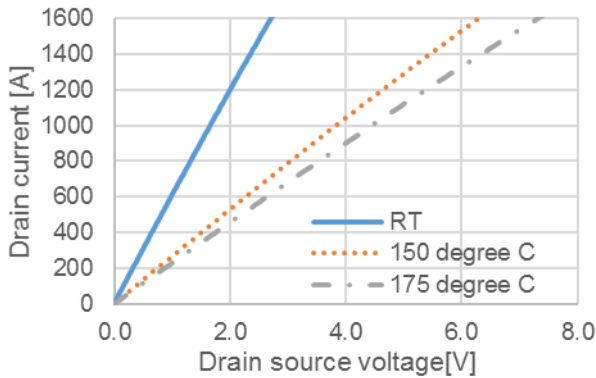


Fig. 9: I_d - V_d characteristics of the conventional and developed SBD-embedded SiC MOSFETs when $V_g = 20$ V.

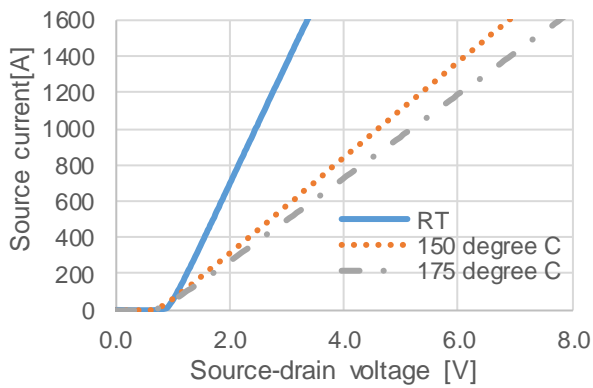


Fig. 10: I_{sd} - V_{sd} characteristics of the conventional and developed SBD-embedded SiC MOSFETs when $V_g = -6$ V.

The temperature dependence of the conduction loss is shown in Fig.11. The conduction loss of the developed SiC MOSFET is less than half that of the IGBT at room temperature. Incidentally, the temperature dependence of the SiC MOSFET is larger than that of the Si IGBT. Although high-temperature operation of more than 150°C is not effective for loss reduction, the conduction loss of the SiC MOSFET is lower than that of the Si IGBT below 150°C.

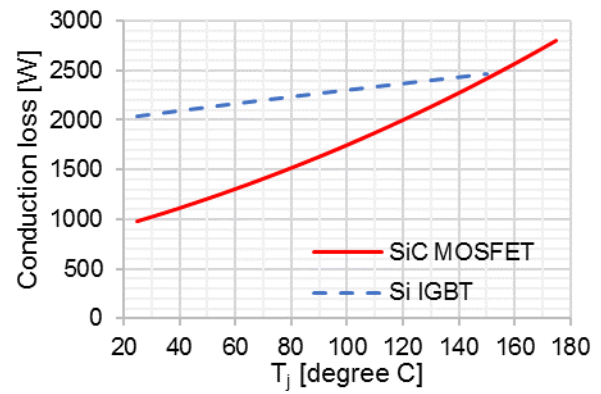


Fig. 11: Temperature dependence of conduction losses between the Si IGBT module and the developed SiC MOSFET module.

Figure 12 shows a comparison of the switching losses between the Si IGBT with Si FRD, the Si IGBT with SiC SBD and the fabricated SiC MOSFET. The Si IGBTs were assembled in the conventional package of which the rated current and a footprint size are 1500 A and 190 × 140 mm, respectively. The switching conditions were set to $V_d = 1800$ V, $I_d = 800$ A, $I_c = 1500$ A, and $T = 150^\circ\text{C}$. The switching currents were normalized with respect to I_d and I_c . The gate voltages were set to +15/-15V for the Si-IGBT and +20/-6V for the SiC-MOSFET. The turn-off loss was calculated by integrating the energy loss between the time when the gate voltage drops below 0.9 V_g and the time when the current drops below 0.02 I_c or 0.02 I_d . The turn-on loss was calculated by integrating the energy loss between the time when the gate voltage exceeds 0.1 V_g and the time when the current falls below 0.02 V_d or 0.02 V_c .

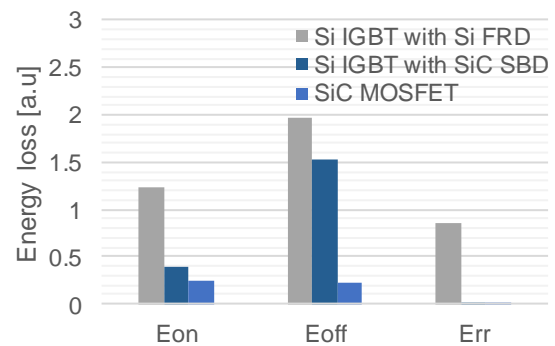


Fig. 12: Comparison of energy losses between the Si IGBT modules and the developed SiC MOSFET module.

The turn-on, turn-off, and recovery losses of the SiC MOSFET module were reduced by 80%, 89%, and 98%, respectively, compared with those of the

Si IGBT with Si FRD module. The turn-on and turn-off energies of the SiC MOSFET module were reduced by 47% and 85%, respectively, compared with those of the Si IGBT with SBD module.

The SiC SBD reduces E_{rr} and E_{on} by eliminating the reverse recovery current. The E_{rr} of the SBD-embedded MOSFET is also negligibly small owing to suppression of bipolar operation even at high temperature.

Figures 13 and 14 respectively show the turn-on and turn-off switching waveforms of the Si-IGBT with SiC SBD and SiC MOSFET. The turn-on losses of the SiC MOSFET modules are slightly reduced owing to the reduced voltage-drop time during turn-on switching. The turn-off losses of the SiC MOSFET modules can also be reduced by a fifth by increasing the switching speed and decreasing the tail current.

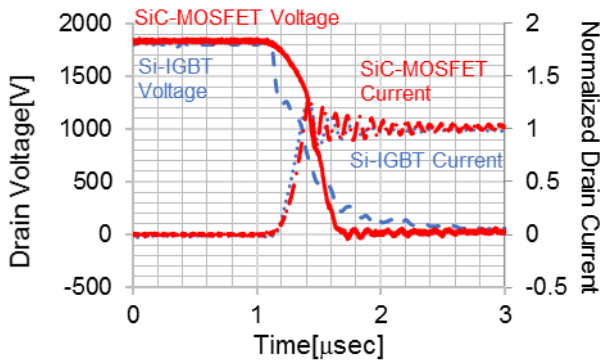


Fig. 13: Comparison of turn-on switching waveforms between the Si IGBT with SiC SBD module and the developed SiC MOSFET module at 150°C. Currents are normalized with respect to the corresponding rated current.

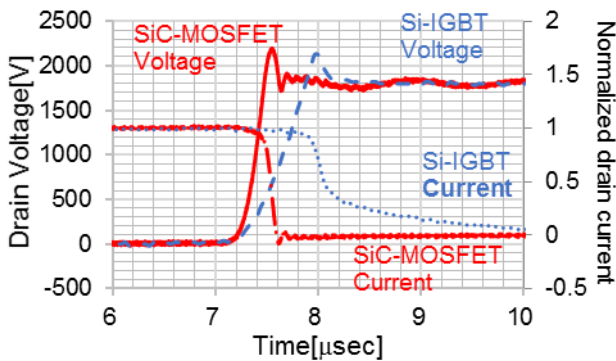


Fig. 14: Comparison of turn-off switching waveforms between the Si IGBT with SiC SBD module and the developed SiC MOSFET module at 150°C. Currents are normalized with respect to the corresponding rated current.

The power consumption of inverters using the conventional Si-IGBT module and the developed SiC module were calculated and compared. In the inverter loss calculation, we assumed the case where Si-IGBTs are used on the high and low sides and where two iXPLVs are connected in parallel.

Figure 15 shows the calculation results for the power dissipation of the inverter. The calculation was carried out under conditions of $V_{ds} = 1500$ V, $I_d = 1024$ A, $\cos\phi = 0.85$, $f_c = 1$ kHz, and $T_j = 150^\circ\text{C}$. The SiC MOSFET module reduced the inverter loss by 60% compared with the Si IGBT with Si PiN module and 43% compared with the Si IGBT with SiC SBD module. The conduction loss of the SiC MOSFET was slightly lower than the Si IGBT as shown in Fig. 12. The reduction in the turn-off switching loss is the main difference in the power dissipation between the Si IGBT with SiC SBD module and SiC MOSFET module.

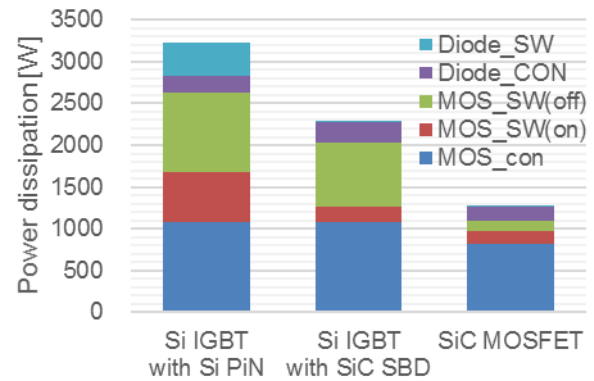


Fig. 15: Comparison of inverter power dissipation between the Si IGBT module and the developed SiC MOSFET module.

We also estimated the impact of the developed SiC MOSFET module on reducing cooler volume. For this, we use the cooling system performance index (CSPI).[8] CSPI [W/K liter] is written as

$$CSPI = 1 / \{R_{th(s-a)} V_{CS}\}$$

where $R_{th(s-a)}$ is thermal resistance between the heatsink and ambient and V_{CS} is the volume of the heatsink. We assume a common cooling system and a CSPI value of 5. We used thermal resistances of $R_{th(j-c)} = 8$ K/kW, $R_{th(c-s)} = 6$ K/kW for the conventional package and $R_{th(j-c)} = 32$ K/kW, $R_{th(c-s)} = 2.3$ K/kW for the iXPLV. The operating conditions of the inverter are the same as in Fig. 15. The calculated cooling system volumes at $T_j = 150^\circ\text{C}$ and $T_a = 40^\circ\text{C}$ are shown in Fig. 16. From

these results, the volume of the cooling system for the developed SiC MOSFET module is reduced by 59% compared with the Si IGBT with the Si FRD module and by 40% compared with the Si IGBT with the SiC SBD module.

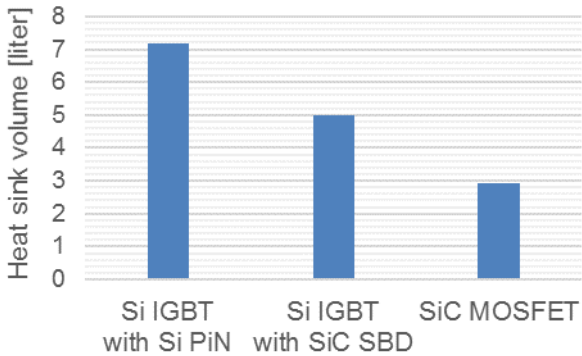


Fig. 16: Heatsink volume of the inverter with Si IGBT module and the developed SiC MOSFET module when CSPI is assumed to be 5.

5 Conclusion

We developed a third-generation SiC MOSFET that solved the reliability issue of body diode operation and achieved a 20% conduction loss reduction compared with the conventional structure. We also developed a new package named iXPLV that improves the power cycle lifetime by two times compared with conventional solder bonding by using a Ag-sintered layer. We compared the developed SiC MOSFET assembled in iXPLV package with the Si-IGBT with Si FRD and the Si-IGBT with SiC SBD, and found that, the developed SiC MOSFET module reduced the energy loss by 60% and 43%, respectively. We also estimated the impact of the developed module in terms of reducing the volume of the cooling system. It was shown that the volume of the heatsink can be reduced by 60% compared with the Si IGBT with Si FRD and 40% compared with the Si IGBT with SiC SBD, respectively. The combination of the third-generation SiC MOSFET and iXPLV package can thus contribute to reducing the volume of power units.

6 References:

- [1] A. Agarwal, H. Fatima, S. Haney, and S. H. Ryu, I, "A New Degradation Mechanism in High-Voltage SiC Power MOSFETs", *IEEE Electron Device Lett.* 28, 587 (2007).
- [2] K. Konishi, S. Yamamoto, S. Nakata, Y. Nakamura, Y. Nakanishi, T. Tanaka, Y. Mitani, N. Tomita, Y. Toyoda, and S. Yamakawa, "Stacking fault expansion from basal plane dislocations converted into threading edge dislocations in 4H-SiC epilayers under high current stress", *Journal of Applied Physics*, vol. 114, p. 014504, (2013).
- [3] T. Tawara, T. Miyazawa, M. Ryo, M. Miyazato, T. Fujimoto, K. Takenaka, S. Matsunaga, M. Miyajima, A. Otsuki, Y. Yonezawa, T. Kato, H. Okumura, T. Kimoto, and H. Tsuchida, "Short minority carrier lifetimes in highly nitrogen-doped 4H-SiC epilayers for suppression of the stacking fault formation in PiN diodes", *Journal of Applied Physics*, vol. 120, p. 115101, (2016).
- [4] K. Kawahara, S. Hino, K. Sadamatsu, S. Tomohisa, and S. Yamakawa, "Impact of embedding Schottky barrier diodes into 3.3kV and 6.5kV SiC MOSFETs", *Materials Science Forum*, vol. 924, p. 727, (2018).
- [5] M. Furukawa, H. Kono, K. Sano, M. Yamaguchi, H. Suzuki, T. Misao and G. Tchouangue, "Improved reliability of 1.2kV SiC MOSFET by preventing the intrinsic body diode operation", *Proceedings of PCIM2020*, pp.1-5, (2020).
- [6] Y. Sekino, T. Tsuji, T. Shiigi, R. Usui, M Utsumi, S. Iwamoto, Y. Kusunoki, M. Takei, Y. Kobayashi, Y. Onishi, and H. Kimura, "3.3kV All SiC Module with 1st Generation Trench Gate SiC MOSFETs for Traction Inverters", *Proceedings of PCIM2020*, pp. 98-103, (2020).
- [7] T. Murakami, K. Sadamatsu, M. Imaizumi, E. Suekawa, and S. Hino, "Comparative study of electrical characteristics between conventional and SBD-embedded MOSFETs for next generation 3.3kV SiC modules", *Proceedings of PCIM2020*, pp. 864-868, (2020).
- [8] U. Drogenik, G. Laimer and J. W. Kolar, "Theoretical Converter Power Density Limits for Forced Convection Cooling", *Proceedings of PCIM2005*, pp. 608-619, (2005).

* Company names, product names, and service names may be trademarks of their respective companies.