H. Kono et al., "Improved reliability of a 2200 V SiC MOSFET module with an epoxy-encapsulated insulated metal substrate", 2024 Power Conversion and Intelligent Motion (PCIM) Europe, Nürnberg, Germany, 2024, pp. 2017-2022. Doi: 10.30420/566262283

Improved reliability of a 2200 V SiC MOSFET module with an epoxy-encapsulated insulated metal substrate

Hiroshi Kono[1], Shun Takeda[1], Eitaro Miyake[1], Tomohiro Iguchi[2], Teruyuki Ohashi[2], Georges Tchouangue[3] and Kazuya Kodani[4].

1 Toshiba Electronic Devices & Storage Corporation, 2 Toshiba corporation, 3 Toshiba Electronics Europe GmbH, 4 Toshiba Infrastructure Systems & Solutions Corporation.

Corresponding author: Hiroshi Kono, hiroshi.kono@toshiba.co.jp

Abstract

The impact of combining epoxy-potting encapsulation with an insulated metal substrate (IMS) on the performance and reliability of SiC MOSFET modules was investigated. Static and dynamic characteristics, thermal resistance, and power cycle tolerance were measured, and a high-temperature bias test and a high-temperature humidity test were carried out. An IMS module with epoxy-potting encapsulation was compared with a conventional ceramic insulated substrate with silicone-gel encapsulation. The IMS module was found to have a higher thermal cycling tolerance, which allowed for a more flexible copper pattern layout. The optimized copper pattern layout enabled reduced conduction loss in the IMS module. In addition, the IMS module exhibited improved power cycling tolerance compared with the conventional ceramic insulated substrate. This improved performance and reliability are expected to contribute to the realization of higher-density power units.

1 Introduction

Silicon carbide power devices offer lower power loss and higher power density compared with silicon due to their superior material properties. Our group has previously developed 3.3 kV class SiC metal-oxide-semiconductor field effect transistors (MOSFETs) and 2.2 kV class SiC MOSFETs modules and showed that these modules make it possible to reduce the volume of the cooling system compared with silicon insulated gate bipolar transistors (Si-IGBTs) [1,2]. As discussed in these studies, thermal management is a key factor in further reducing the volume and weight of power conversion units. For example, power units with higher power densities are subject to higher thermal cycling stress, which reduces the life of the power unit. Therefore, it is important to reduce losses, and thermal resistance and to improve thermal cycling life in order to increase the power density of the unit.

Traditionally, ceramic substrates have been used for power modules owing to their excellent insulation and thermal properties. With the recent development of resin insulation materials, insulated metal substrates are also being considered as promising candidates for power module insulation materials. Insulating resin has a linear expansion coefficient similar to that of copper, and thus maintains thermal cycling reliability even as substrate size increases. Epoxy-potting encapsulations can be used for insulating resin substrates and can improve power cycle tolerance compared with conventional silicone-gel encapsulations. However, since the thermal conductivity of insulating resin is lower than that of ceramic substrates, thus increasing the thermal resistance of the device, the overall thermal design is an important factor for improving reliability.

In this study, we fabricated modules with reduced thermal resistance by optimizing the chip layout and investigated the impact on characteristics and reliability. Modules were fabricated using a 2.2 kV Schottky barrier diode (SBD)-embedded SiC-MOSFET chip [2], and 2.2 kV modules using ceramic substrates and standard gel-encapsulated packages [2] were used for reference.

2 SBD-embedded SiC MOSFET device

Degradation of on-resistance caused by bipolar operation has been a problem for SiC MOSFETs [3,4]. SBD-embedded MOSFETs are an essential solution to this problem because they are able to

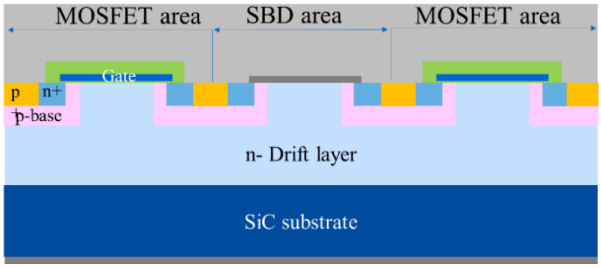


Fig. 1: Schematic cross-section of the fabricated SBD-embedded SiC MOSFET.

Fig. 3: 2200 V, 250A, 2in1 all SiC IMS module with an epoxy-potting encapsulation.

suppress the bipolar operation of the body diode of a MOSFET [5,6]. Figure 1 shows a schematic cross-section of the fabricated 2.2 kV class SBD-embedded SiC MOSFET that is based on a planar gate structure.

Figure 2 shows the reverse current characteristics of the developed MOSFETs when Vg = −5 V and the temperature is 150°C. The SBD-embedded SiC MOSFET does not start bipolar operation until the current exceeds 450 A, even at 150°C.

3 Insulated metal substrate module

In order to reduce the size of a power converter, it is important to reduce the power consumption and package size of the power module. As mentioned above, IMS can achieve sufficient reliability even if with increased substrate size and copper pattern thickness which help to achieve a low resistance package. In this study, to take advantage of these features and overcome the low thermal conductivity, the thermal resistance of the module was reduced by optimizing the chip layout. This was accomplished by suppressing the thermal interference between the chips. Figure 3 shows the fabricated 2.2 kV, 250 A, 2-in-1 all SiC IMS module with an epoxy-potting encapsulation.

Figure 4 shows a comparison of the thermal resistances estimated from the structure function between the IMS module and the conventional ceramic module. The thermal resistance of the IMS module was 16% lower than that of the conventional package.

Figure 5 shows a comparison of the power cycling test between the IMS module and the ceramic module. The input power was set such that T_{vjmax}, ΔT, and t_{on} were 150°C, 80°C, and 2 s, respectively. The vertical axis shows the rate of change of V_{sd}. Results are normalized with respect to the lifetime of the conventional ceramic module, which was defined as the point at which the rate of change exceeds 1.05. The lifetime of the IMS module was six times longer than that of the

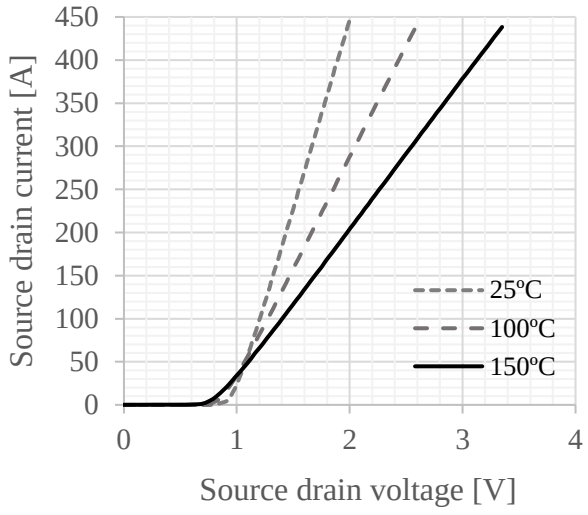


Fig. 2: I_{sd}-V_{sd} characteristics of the SBD-embedded SiC MOSFET when V_g = −5 V at 150 °C.

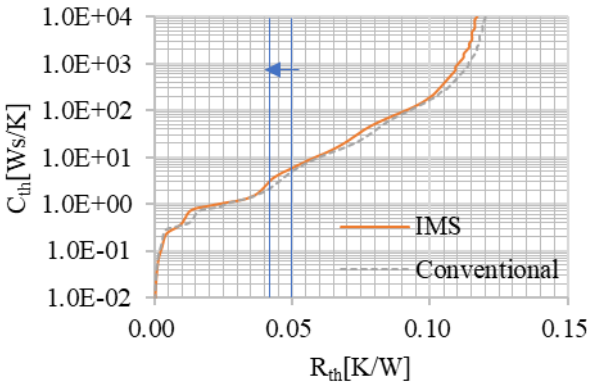


Fig. 4: Comparison of structure functions between the conventional and IMS modules.

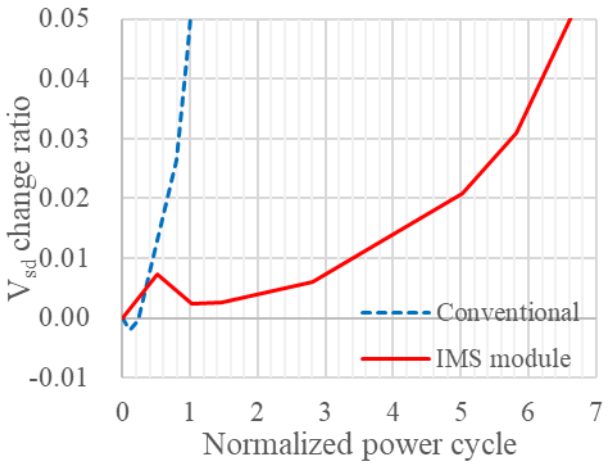


Fig. 5: Comparison of power cycling tolerance between the conventional and IMS modules. Tests were caried out with T_{jmax} = 150°C, d_{tj} = 80°C, and t_{on} = 2 s.

ceramic module. These experimental results demonstrate that the developed module had higher performance and reliability than did the conventional modules.

Figures 6 and 7 show scanning electron microscope (SEM) images of the bonding wires at the end of the power cycling test. Whereas the ceramic module wire separated at the interface between the bonding wire and the surface metal, the IMS module wire cracked vertically. It is thought that the epoxy-encapsulation prevented wire lift-off and improved the lifetime.

The thermal resistance was calculated from the power cycling test results as shown in Fig. 8. This result shows that the developed IMS module had lower thermal resistance than did the conventional

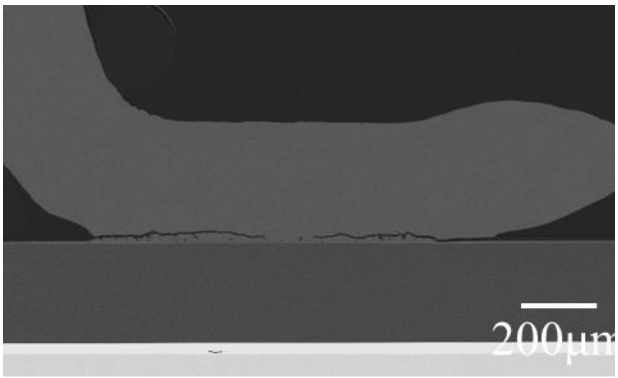


Fig. 6: SEM image of the bonding wire at the end of the power cycling test for the ceramic module.

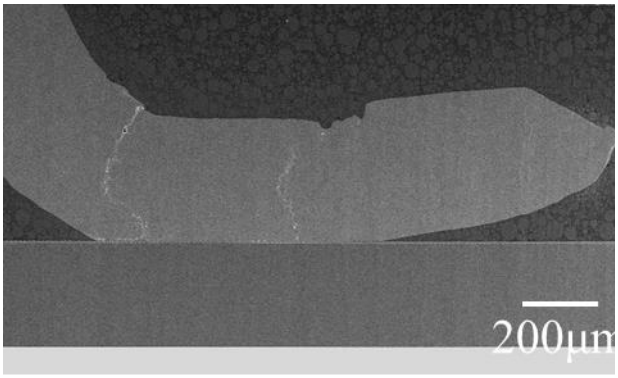


Fig. 7: SEM image of the bonding wire at the end of the power cycling test for the IMS module.

module, which matches the results evaluated by the structure function.

In addition to thermal reliability, we also investigated electrical reliability. Although there

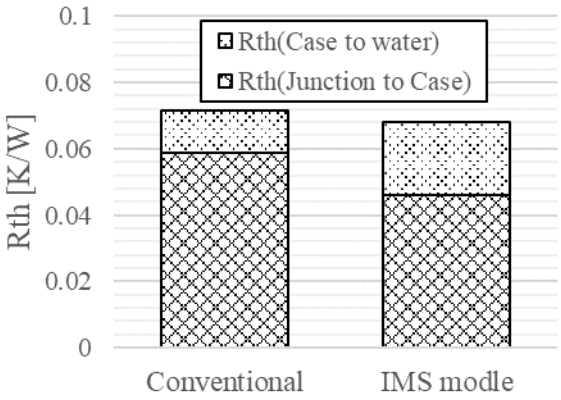


Fig. 8: Comparison of thermal resistivity evaluated by a power cycling test between the conventional and IMS modules.

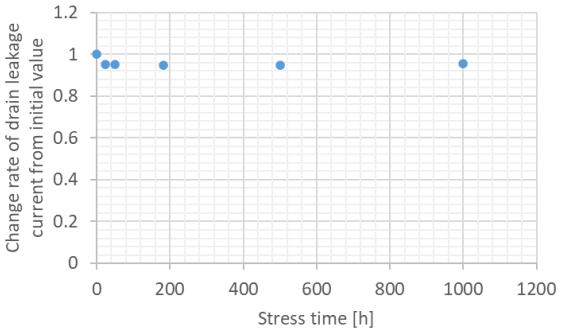


Fig. 9: Time dependence of leakage current evaluated by a high-temperature drain vias stress test (V_d = 2200 V, V_g = −10 V, 150°C).

was a concern that the moisture resistance of the resin-insulated substrate would be lower than that of the ceramic substrate, no failures occurred during a 1000 h high-temperature humidity test conducted under conditions of 85°C, 85% humidity, and 1760 V. In addition, as shown in Fig. 9, no degradation was observed in the high temperature drain bias stress test where V_d = 2200 V, V_g = −10 V, and the temperature was 150°C. These results indicate that the developed epoxy-potting encapsulated IMS had low thermal resistance and high reliability.

4 Comparison of device characteristics

Figures 10 and 11 show comparisons of the I_d-V_d characteristics and on-resistance between the conventional and IMS modules. The resistances were measured at the main terminals. The copper pattern can be made thicker on the IMS, thereby the package loss was reduced.

Figures 12 shows the turn-on and turn-off switching waveforms of the conventional module and IMS module. Figures 13 shows the comparison of the switching loss. No obvious difference in switching losses was observed.

The power consumption of inverters using the conventional Si-IGBT module and the developed SiC module were calculated and compared. In the inverter loss calculation, we assumed the case of Si-IGBTs are in a T-type three-level inverter and SiC-MOSFETs in a two-level inverter [1, 7].

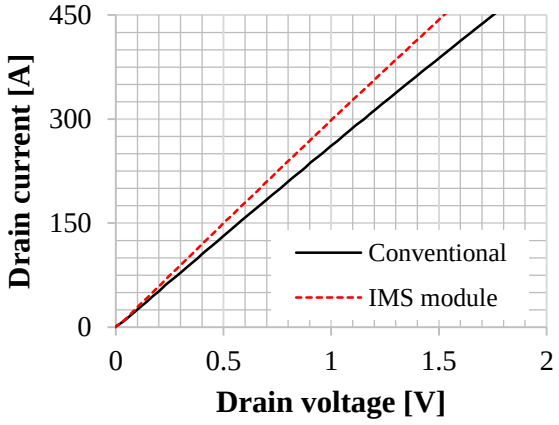


Fig. 10: I_d-V_d characteristics of the conventional and IMS modules when V_g = 20 V.

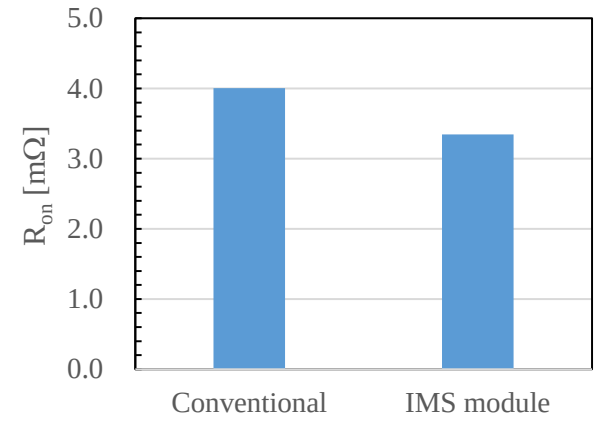
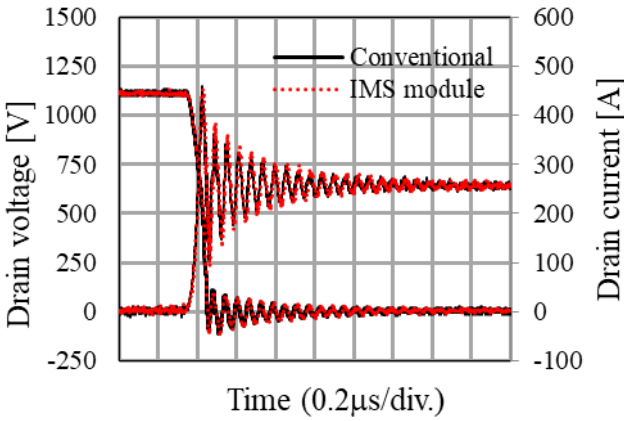
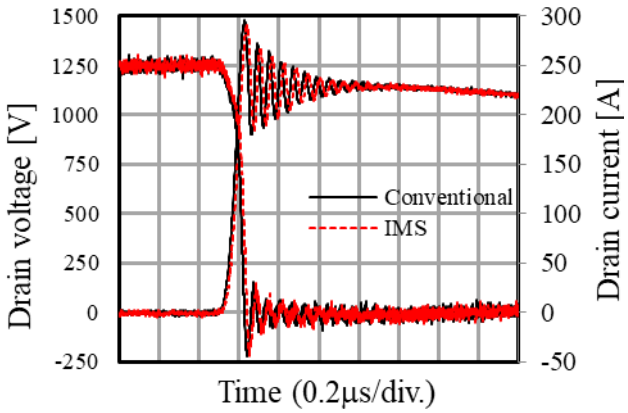


Fig. 11: Comparison of on-resistance between the conventional and IMS modules.



(a) Turn-on



(b) turn-off

Fig. 12: Comparison of the switching waveforms between the IMS module and the conventional module at 150°C. Test condition: V_{ds}=1100V, I_d = 250 A, V_{gs} = −6 /+20 V, R_{gon} = 0.5 Ω, R_{goff} =3 Ω.

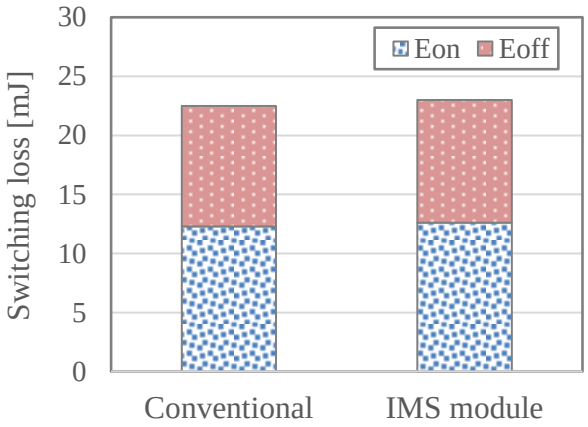


Fig. 13: Comparison of switching losses between conventional and IMS modules.

Figure 14 shows the calculation results for the power dissipation of an inverter arm. The calculation was carried out under conditions of V_{ds} = 1200 V, I_d = 200 A, cosϕ = 1, f_c = 10 kHz, and T_j = 150°C for SiC MOSFET. For Si-IGBTs, the calculation was carried out under the conditions of V_{ce} =600 V, Id = 200 A, cos = 1, fc = 5 kHz, and Tj = 150°C. The inverter loss was 27% lower in the SiC MOSFET module compared with the Si-IGBT module.

We also estimated the impact of the developed SiC MOSFET module on reducing cooler volume. For this, we used the cooling system performance index (CSPI) [W/K L] [8], which is calculated as

$$\mathrm{CSPI} = {}^{1}\Big/_{\{R_{th(s-a)}V_{CS}\}}$$

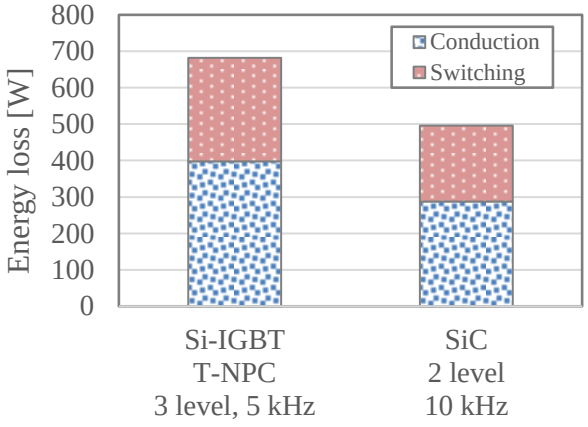


Fig. 14: Comparison of an inverter arm power dissipation between the Si IGBT modules and the developed SiC MOSFET modules.

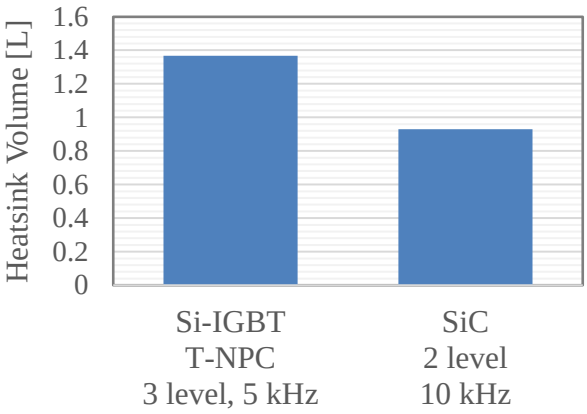


Fig. 15: Heatsink volume of the inverter with Si IGBT module and the developed SiC MOSFET module when CSPI is assumed to be 5.

where $R_{th(s-a)}$ is the thermal resistance between the heatsink and ambient and V_{cs} is the volume of the heatsink. We assumed a common cooling system and a CSPI value of 5. The operating conditions of the inverter were the same as in Fig. 14. The calculated cooling system volumes at T_j = 150°C and T_a = 40°C are shown in Fig. 16. These results show that the volume of the cooling system for the developed SiC MOSFET module was 32% lower than that of the Si IGBT module.

In high-load applications, the operating conditions ΔT_j and T_{jmax} can be suppressed to ensure the power cycle life of the module. Assuming that lowering ΔT_j by 20°C improves the power cycle endurance by a factor of about 3, the developed module allows ΔT_j to be increased by 20°C. The improved power cycle tolerance allows a reduction

	Conventional	IMS module
Current [A]	100	133
Number of modules	4	3
Loss per module [W]	66.1	92.5
Total loss [W]	264.2	277.6
ΔT_j [°C]	50	69.6

Table 1 Comparison of temperature rise when the number of modules in parallel is reduced.

in the number of modules connected in parallel, whereas conventional modules need to be arranged in parallel to ensure reliability by reducing the current per module. Table 1 shows this comparison. The temperature rose by 50°C with 4 modules in parallel and an output current of 100 A and by 69.6°C when the number of modules in parallel was 3 and the current was increased to 133 A.

5 Conclusion

We have developed an IMS module SiC MOSFET that has lower conduction and thermal resistance and six-times higher power cycle life compared with conventional ceramic modules. The developed SiC MOSFET module exhibited a 27% reduction in power dissipation compared with Si-IGBTs. The impact of the developed module on volume reduction of the cooling system was also evaluated. The results showed that the volume of the heat sink can be reduced by 32%. It was also demonstrated that improvement in power cycle endurance contributed to reducing the number of modules in parallel. Therefore, the combination of third-generation SiC MOSFETs and IMS modules can contribute to reducing the volume of power units.

6 References:

[1] H. Kono, T. Iguchi, T. Hirakawa, H. Irifune, T. Kawano, M. Furukawa, K. Sano, M. Yamaguchi, H. Suzuki, and G. Tchouangue, "3.3 kV All SiC MOSFET Module with Schottky Barrier Diode Embedded SiC MOSFET", Proceedings of PCIM Europe 2021, pp. 914-919, (2021).

[2] T. Ogata, H. Kono, H. Irifune, S. Fujii, T. Tanaka and G. Tchouangue, "A Novel 2200 V Schottky Barrier Diode-Embedded SiC MOSFET Module", Proceedings of PCIM Europe 2023, pp. 1-6 (2023).

[3] A. Agarwal, H. Fatima, S. Haney, and S. H. Ryu, I, "A New Degradation Mechanism in High-Voltage SiC Power MOSFETs", IEEE Electron Device Lett. 28, 587, (2007).

[4] K. Konishi, S. Yamamoto, S. Nakata, Y. Nakamura, Y. Nakanishi, T. Tanaka, Y. Mitani, N. Tomita, Y. Toyoda, and S. Yamakawa, "Stacking fault expansion from basal plane dislocations converted into threading edge dislocations in 4H-SiC epilayers under high current stress", Journal of Applied Physics, vol. 114, p. 014504, (2013).

[5] K. Kawahara, S. Hino, K. Sadamatsu, S. Tomohisa, and S. Yamakawa, "Impact of embedding Schottky barrier diodes into 3.3kV and 6.5kV SiC MOSFETs", Materials Science Forum, vol. 924, p. 727, (2018).

[6] M. Furukawa, H. Kono, K. Sano, M. Yamaguchi, H. Suzuki, T. Misao and G. Tchouangue, "Improved reliability of 1.2kV SIC MOSFET by preventing the intrinsic body diode operation", Proceedings of PCIM Europe 2020, pp.1-5, (2020).

[7] I. Staudt, "3L NPC & TNPC Topology. Semikron Application Note: An11001 SEMIKRON" in, 2015.

[8] U. Drofenik, G. Laimer and J. W. Kolar, "Theoretical Converter Power Density Limits for Forced Convection Cooling", Proceedings of PCIM2005, pp. 608-619, (2005).